

# NSS40302PDR2G

## Complementary 40 V, 6.0 A, Low $V_{CE(sat)}$ Transistor

ON Semiconductor's e<sup>2</sup>PowerEdge family of low  $V_{CE(sat)}$  transistors are surface mount devices featuring ultra low saturation voltage ( $V_{CE(sat)}$ ) and high current gain capability. These are designed for use in low voltage, high speed switching applications where affordable efficient energy control is important.

Typical applications are low voltage motor controls in mass storage products such as disc drives and tape drives. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows e<sup>2</sup>PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

### Features

- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

Rating		Symbol	Max	Unit
Collector-Emitter Voltage	NPN PNP	$V_{CEO}$	40 -40	Vdc
Collector-Base Voltage	NPN PNP	$V_{CBO}$	40 -40	Vdc
Emitter-Base Voltage	NPN PNP	$V_{EBO}$	6.0 -7.0	Vdc
Collector Current – Continuous	NPN PNP	$I_C$	3.0 -3.0	A
Collector Current – Peak	NPN PNP	$I_{CM}$	6.0 -6.0	A
Electrostatic Discharge		ESD	HBM Class 3B MM Class C	

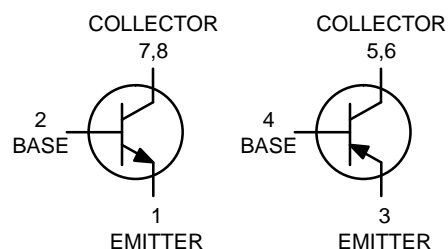
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



ON Semiconductor®

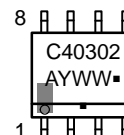
[www.onsemi.com](http://www.onsemi.com)

**40 VOLTS, 6.0 AMPS  
COMPLEMENTARY LOW  
 $V_{CE(sat)}$  TRANSISTOR  
EQUIVALENT  $R_{DS(on)}$  80 m $\Omega$**



**SOIC-8  
CASE 751  
STYLE 16**

### DEVICE MARKING



C40302 = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
NSS40302PDR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
NSV40302PDR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NSS40302PDR2G

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
----------------	--------	-----	------

### SINGLE HEATED

Total Device Dissipation (Note 1) $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	576	mW
		4.6	mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	217	$^\circ\text{C/W}$
Total Device Dissipation (Note 2) $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	676	mW
		5.4	mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	185	$^\circ\text{C/W}$

### DUAL HEATED (Note 3)

Total Device Dissipation (Note 1) $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	653	mW
		5.2	mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	191	$^\circ\text{C/W}$
Total Device Dissipation (Note 2) $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	783	mW
		6.3	mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	160	$^\circ\text{C/W}$
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

1. FR-4 @ 10 mm<sup>2</sup>, 1 oz. copper traces, still air.
2. FR-4 @ 100 mm<sup>2</sup>, 1 oz. copper traces, still air.
3. Dual heated values assume total power is the sum of two equally powered devices.

# NSS40302PDR2G

## NPN ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

### OFF CHARACTERISTICS

Collector–Emitter Breakdown Voltage (I <sub>C</sub> = 10 mA, I <sub>B</sub> = 0)	V <sub>(BR)CEO</sub>	40	–	–	Vdc
Collector–Base Breakdown Voltage (I <sub>C</sub> = 0.1 mA, I <sub>E</sub> = 0)	V <sub>(BR)CBO</sub>	40	–	–	Vdc
Emitter–Base Breakdown Voltage (I <sub>E</sub> = 0.1 mA, I <sub>C</sub> = 0)	V <sub>(BR)EBO</sub>	6.0	–	–	Vdc
Collector Cutoff Current (V <sub>CB</sub> = 40 Vdc, I <sub>E</sub> = 0)	I <sub>CBO</sub>	–	–	0.1	μAdc
Emitter Cutoff Current (V <sub>EB</sub> = 6.0 Vdc)	I <sub>EBO</sub>	–	–	0.1	μAdc

### ON CHARACTERISTICS

DC Current Gain (Note 5) (I <sub>C</sub> = 10 mA, V <sub>CE</sub> = 2.0 V) (I <sub>C</sub> = 500 mA, V <sub>CE</sub> = 2.0 V) (I <sub>C</sub> = 1.0 A, V <sub>CE</sub> = 2.0 V) (I <sub>C</sub> = 2.0 A, V <sub>CE</sub> = 2.0 V)	h <sub>FE</sub>	200 200 180 180	400 350 340 320	– – – –	
Collector–Emitter Saturation Voltage (Note 5) (I <sub>C</sub> = 0.1 A, I <sub>B</sub> = 0.010 A) (I <sub>C</sub> = 1.0 A, I <sub>B</sub> = 0.100 A) (I <sub>C</sub> = 1.0 A, I <sub>B</sub> = 0.010 A) (I <sub>C</sub> = 2.0 A, I <sub>B</sub> = 0.200 A)	V <sub>CE(sat)</sub>	– – – –	0.008 0.044 0.080 0.082	0.011 0.060 0.115 0.115	V
Base–Emitter Saturation Voltage (Note 5) (I <sub>C</sub> = 1.0 A, I <sub>B</sub> = 0.01 A)	V <sub>BE(sat)</sub>	–	0.780	0.900	V
Base–Emitter Turn–on Voltage (Note 5) (I <sub>C</sub> = 0.1 A, V <sub>CE</sub> = 2.0 V)	V <sub>BE(on)</sub>	–	0.650	0.750	V
Cutoff Frequency (I <sub>C</sub> = 100 mA, V <sub>CE</sub> = 5.0 V, f = 100 MHz)	f <sub>T</sub>	100	–	–	MHz
Input Capacitance (V <sub>EB</sub> = 0.5 V, f = 1.0 MHz)	C <sub>ibo</sub>	–	320	450	pF
Output Capacitance (V <sub>CB</sub> = 3.0 V, f = 1.0 MHz)	C <sub>obo</sub>	–	40	50	pF

### SWITCHING CHARACTERISTICS

Delay (V <sub>CC</sub> = 30 V, I <sub>C</sub> = 750 mA, I <sub>B1</sub> = 15 mA)	t <sub>d</sub>	–	–	100	ns
Rise (V <sub>CC</sub> = 30 V, I <sub>C</sub> = 750 mA, I <sub>B1</sub> = 15 mA)	t <sub>r</sub>	–	–	100	ns
Storage (V <sub>CC</sub> = 30 V, I <sub>C</sub> = 750 mA, I <sub>B1</sub> = 15 mA)	t <sub>s</sub>	–	–	780	ns
Fall (V <sub>CC</sub> = 30 V, I <sub>C</sub> = 750 mA, I <sub>B1</sub> = 15 mA)	t <sub>f</sub>	–	–	110	ns

4. Pulsed Condition: Pulse Width = 300 μsec, Duty Cycle ≤ 2%.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# NSS40302PDR2G

## PNP ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

### OFF CHARACTERISTICS

Collector–Emitter Breakdown Voltage ( $I_C = -10\text{ mA}$ , $I_B = 0$ )	$V_{(BR)CEO}$	-40	–	–	Vdc
Collector–Base Breakdown Voltage ( $I_C = -0.1\text{ mA}$ , $I_E = 0$ )	$V_{(BR)CBO}$	-40	–	–	Vdc
Emitter–Base Breakdown Voltage ( $I_E = -0.1\text{ mA}$ , $I_C = 0$ )	$V_{(BR)EBO}$	-7.0	–	–	Vdc
Collector Cutoff Current ( $V_{CB} = -40\text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	–	–	-0.1	$\mu\text{A}$ dc
Emitter Cutoff Current ( $V_{EB} = -6.0\text{ Vdc}$ )	$I_{EBO}$	–	–	-0.1	$\mu\text{A}$ dc

### ON CHARACTERISTICS

DC Current Gain (Note 5) ( $I_C = -10\text{ mA}$ , $V_{CE} = -2.0\text{ V}$ ) ( $I_C = -500\text{ mA}$ , $V_{CE} = -2.0\text{ V}$ ) ( $I_C = -1.0\text{ A}$ , $V_{CE} = -2.0\text{ V}$ ) ( $I_C = -2.0\text{ A}$ , $V_{CE} = -2.0\text{ V}$ )	$h_{FE}$	250 220 180 150	380 340 300 230	– – – –	
Collector–Emitter Saturation Voltage (Note 5) ( $I_C = -0.1\text{ A}$ , $I_B = -0.010\text{ A}$ ) ( $I_C = -1.0\text{ A}$ , $I_B = -0.100\text{ A}$ ) ( $I_C = -1.0\text{ A}$ , $I_B = -0.010\text{ A}$ ) ( $I_C = -2.0\text{ A}$ , $I_B = -0.200\text{ A}$ )	$V_{CE(sat)}$	– – – –	-0.013 -0.075 -0.130 -0.135	-0.017 -0.095 -0.170 -0.170	V
Base–Emitter Saturation Voltage (Note 5) ( $I_C = -1.0\text{ A}$ , $I_B = -0.01\text{ A}$ )	$V_{BE(sat)}$	–	-0.780	-0.900	V
Base–Emitter Turn–on Voltage (Note 5) ( $I_C = -0.1\text{ A}$ , $V_{CE} = -2.0\text{ V}$ )	$V_{BE(on)}$	–	-0.660	-0.750	V
Cutoff Frequency ( $I_C = -100\text{ mA}$ , $V_{CE} = -5.0\text{ V}$ , $f = 100\text{ MHz}$ )	$f_T$	100	–	–	MHz
Input Capacitance ( $V_{EB} = -0.5\text{ V}$ , $f = 1.0\text{ MHz}$ )	$C_{ibo}$	–	250	300	pF
Output Capacitance ( $V_{CB} = -3.0\text{ V}$ , $f = 1.0\text{ MHz}$ )	$C_{obo}$	–	50	65	pF

### SWITCHING CHARACTERISTICS

Delay ( $V_{CC} = -30\text{ V}$ , $I_C = -750\text{ mA}$ , $I_{B1} = -15\text{ mA}$ )	$t_d$	–	–	60	ns
Rise ( $V_{CC} = -30\text{ V}$ , $I_C = -750\text{ mA}$ , $I_{B1} = -15\text{ mA}$ )	$t_r$	–	–	120	ns
Storage ( $V_{CC} = -30\text{ V}$ , $I_C = -750\text{ mA}$ , $I_{B1} = -15\text{ mA}$ )	$t_s$	–	–	400	ns
Fall ( $V_{CC} = -30\text{ V}$ , $I_C = -750\text{ mA}$ , $I_{B1} = -15\text{ mA}$ )	$t_f$	–	–	130	ns

5. Pulsed Condition: Pulse Width = 300  $\mu\text{sec}$ , Duty Cycle  $\leq 2\%$ .

NPN TYPICAL CHARACTERISTICS

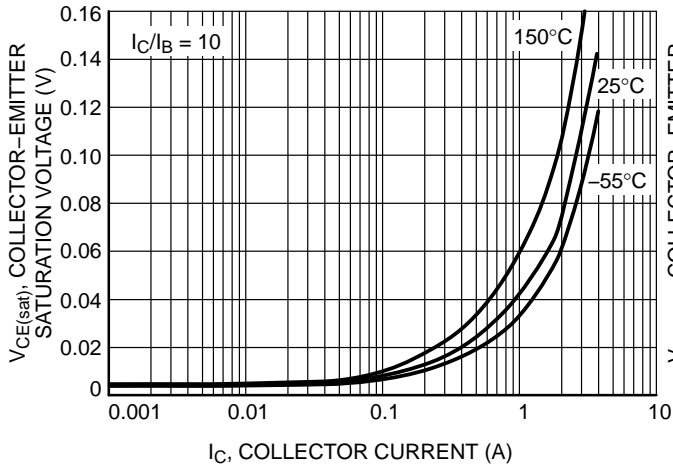


Figure 1. Collector Emitter Saturation Voltage vs. Collector Current

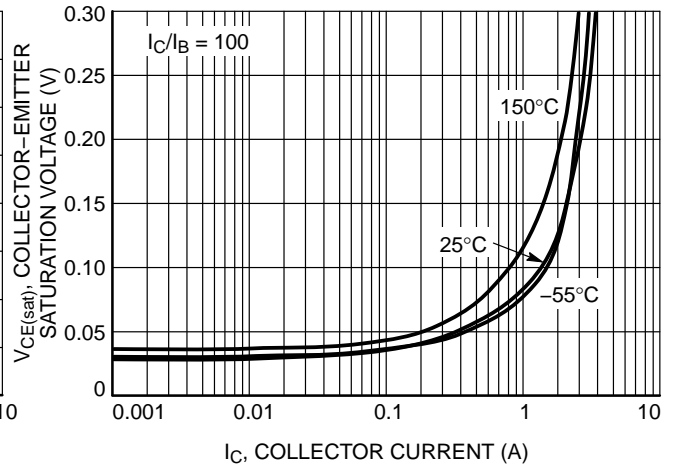


Figure 2. Collector Emitter Saturation Voltage vs. Collector Current

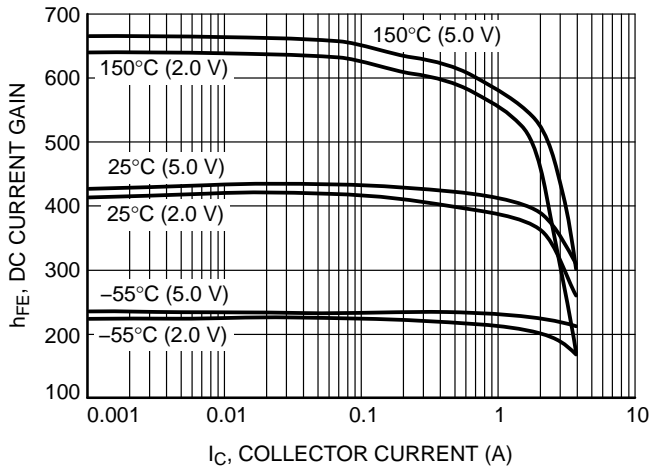


Figure 3. DC Current Gain vs. Collector Current

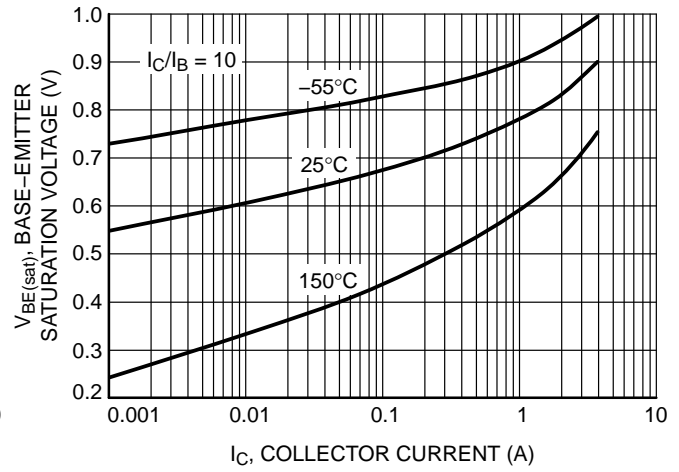


Figure 4. Base Emitter Saturation Voltage vs. Collector Current

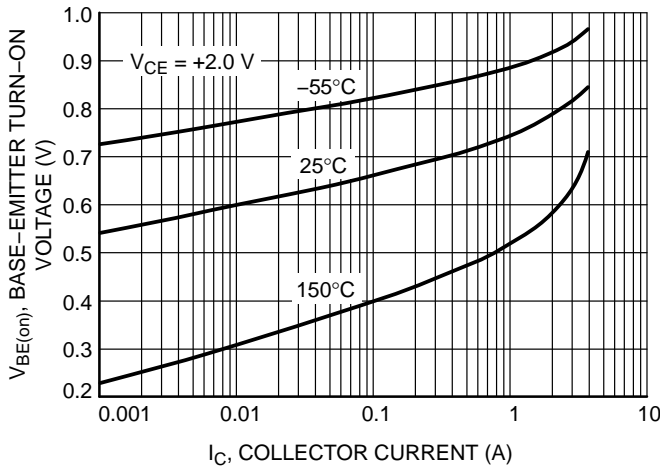


Figure 5. Base Emitter Turn-On Voltage vs. Collector Current

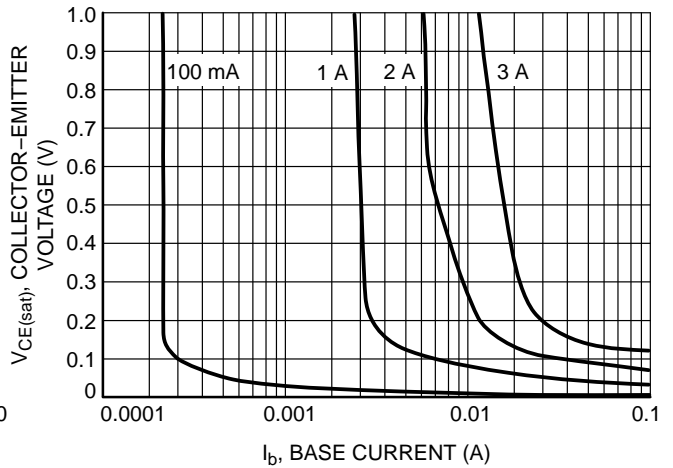


Figure 6. Saturation Region

NPN TYPICAL CHARACTERISTICS

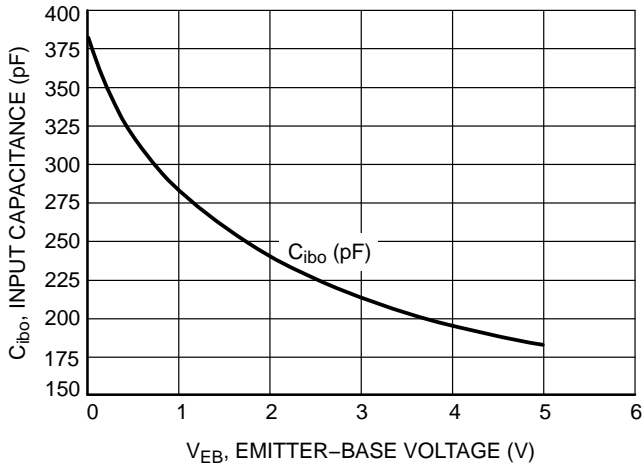


Figure 7. Input Capacitance

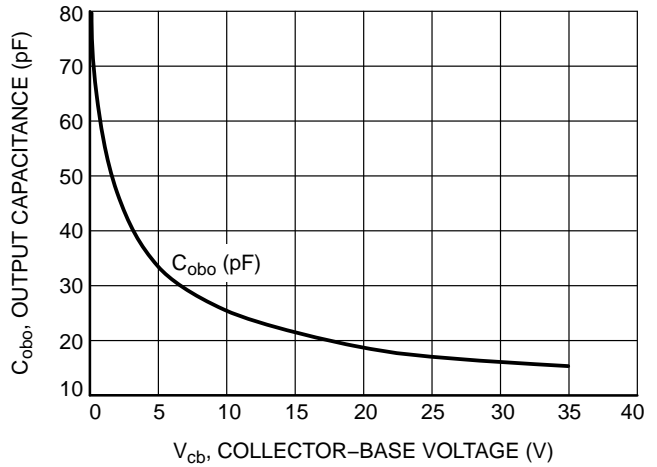


Figure 8. Output Capacitance

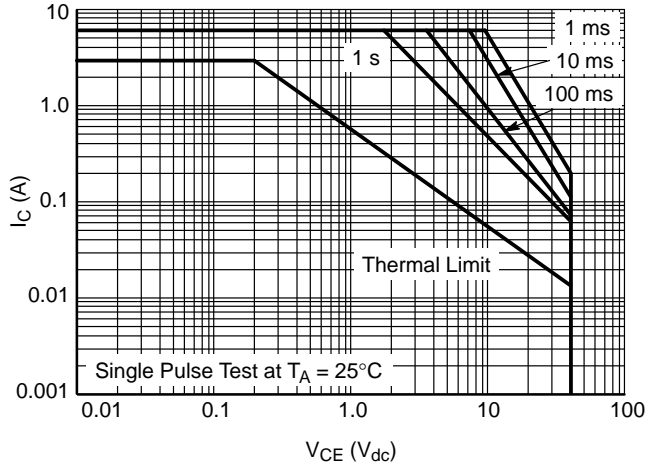


Figure 9. Safe Operating Area

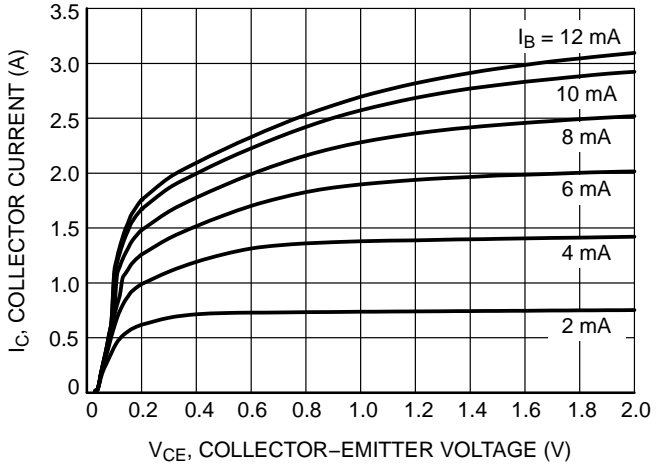


Figure 10. Collector Current as a Function of Collector Emitter Voltage

PNP TYPICAL CHARACTERISTICS

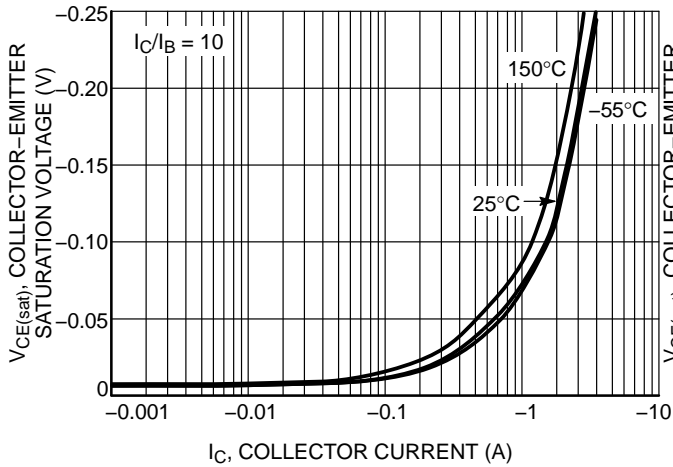


Figure 11. Collector Emitter Saturation Voltage vs. Collector Current

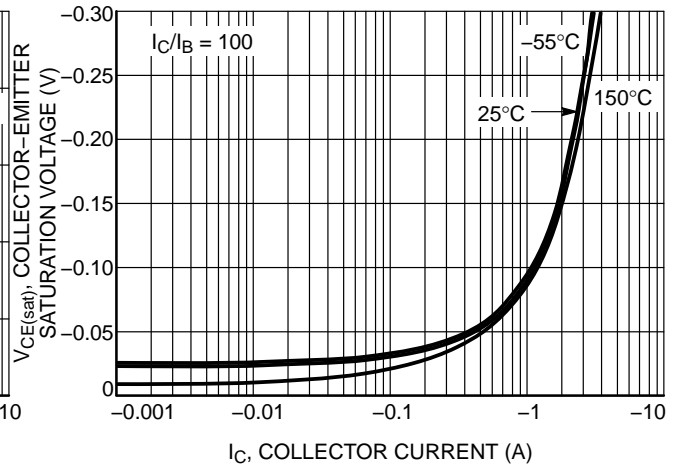


Figure 12. Collector Emitter Saturation Voltage vs. Collector Current

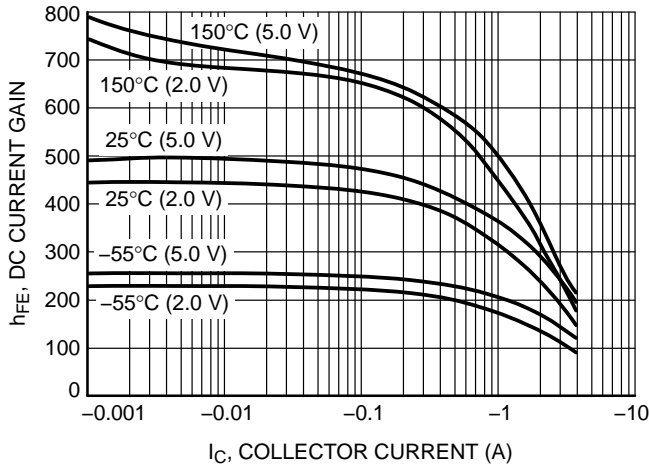


Figure 13. DC Current Gain vs. Collector Current

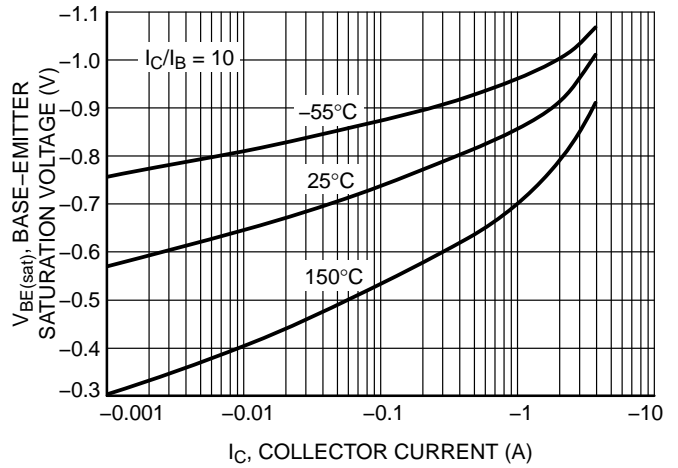


Figure 14. Base Emitter Saturation Voltage vs. Collector Current

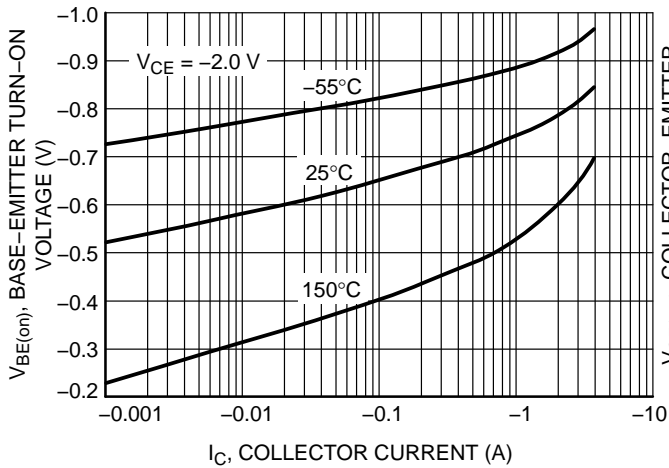


Figure 15. Base Emitter Turn-On Voltage vs. Collector Current

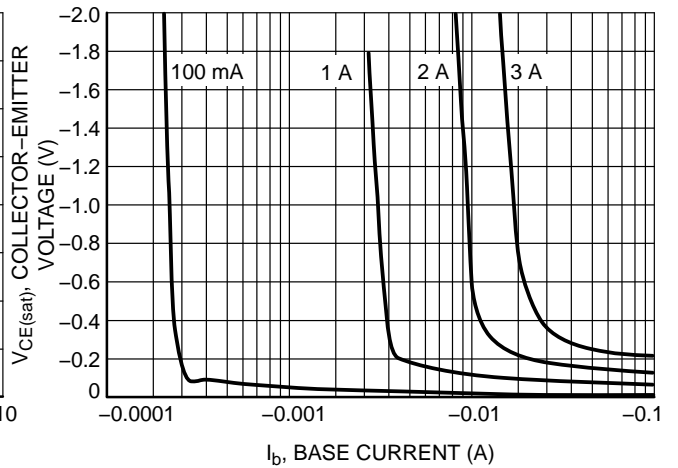


Figure 16. Saturation Region

PNP TYPICAL CHARACTERISTICS

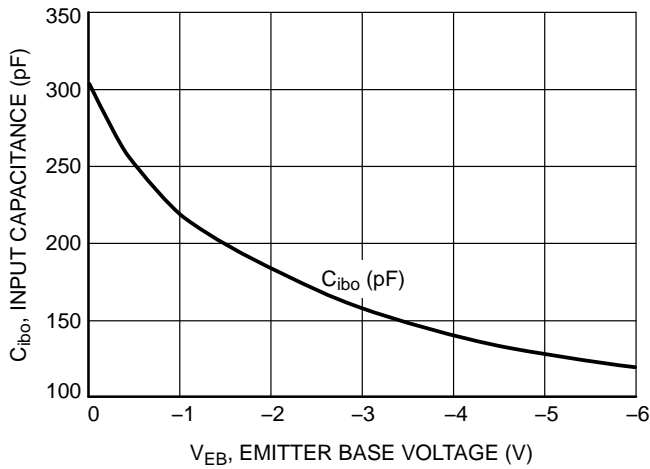


Figure 17. Input Capacitance

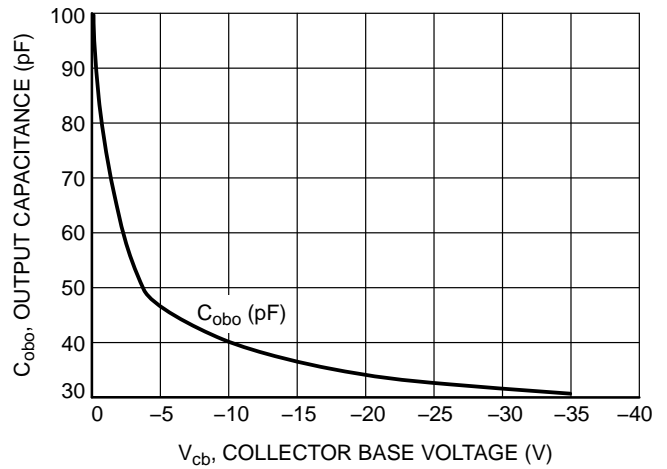


Figure 18. Output Capacitance

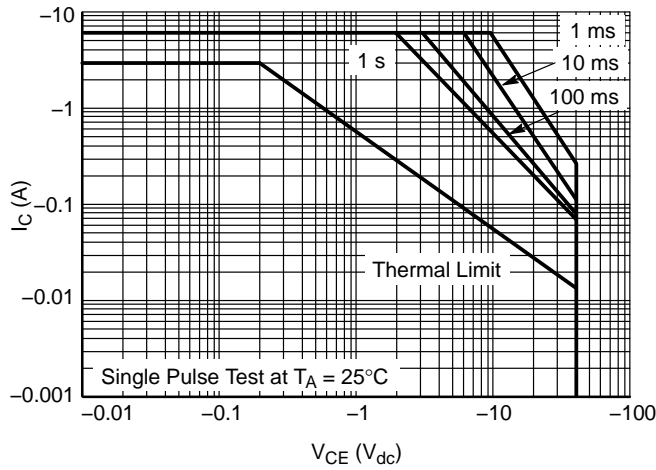


Figure 19. Safe Operating Area

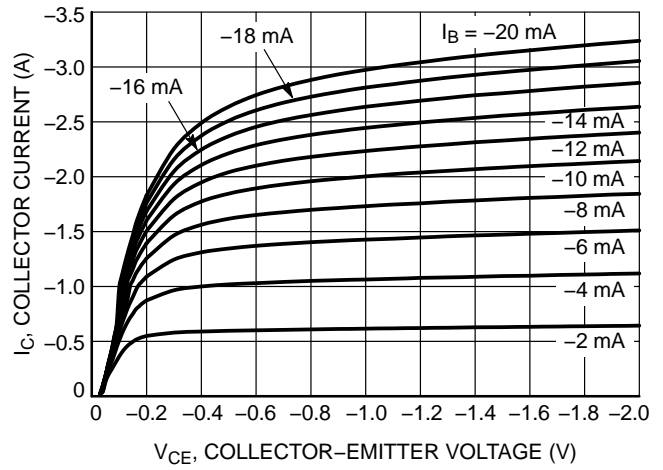
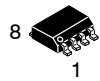


Figure 20. Output Characteristics



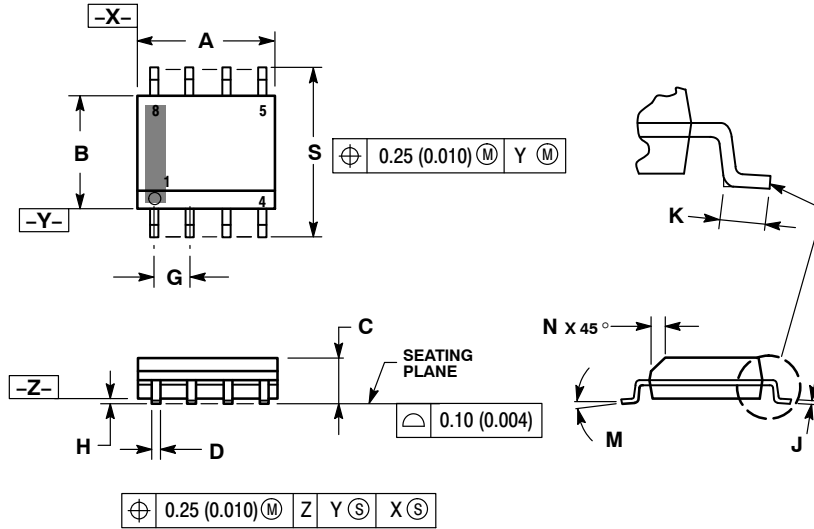
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

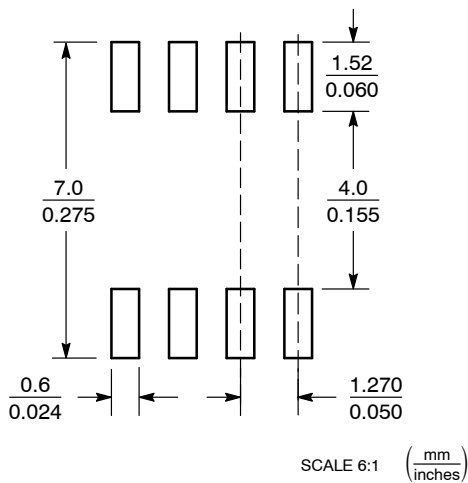
DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

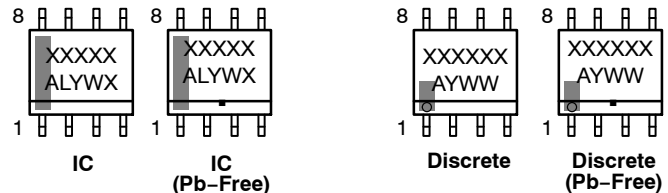
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

## SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM\*



XXXXX = Specific Device Code  
 A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 W = Work Week  
 ■ = Pb-Free Package

XXXXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

## STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

onsemi and ONsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |   |  |  |  |
|---|--|--|--|
| <p>STYLE 1:<br/>         PIN 1. EMITTER<br/>         2. COLLECTOR<br/>         3. COLLECTOR<br/>         4. EMITTER<br/>         5. EMITTER<br/>         6. BASE<br/>         7. BASE<br/>         8. EMITTER</p>   | <p>STYLE 2:<br/>         PIN 1. COLLECTOR, DIE, #1<br/>         2. COLLECTOR, #1<br/>         3. COLLECTOR, #2<br/>         4. COLLECTOR, #2<br/>         5. BASE, #2<br/>         6. EMITTER, #2<br/>         7. BASE, #1<br/>         8. EMITTER, #1</p>               | <p>STYLE 3:<br/>         PIN 1. DRAIN, DIE #1<br/>         2. DRAIN, #1<br/>         3. DRAIN, #2<br/>         4. DRAIN, #2<br/>         5. GATE, #2<br/>         6. SOURCE, #2<br/>         7. GATE, #1<br/>         8. SOURCE, #1</p>                            | <p>STYLE 4:<br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. ANODE<br/>         4. ANODE<br/>         5. ANODE<br/>         6. ANODE<br/>         7. ANODE<br/>         8. COMMON CATHODE</p>   |
| <p>STYLE 5:<br/>         PIN 1. DRAIN<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. DRAIN<br/>         5. GATE<br/>         6. GATE<br/>         7. SOURCE<br/>         8. SOURCE</p>   | <p>STYLE 6:<br/>         PIN 1. SOURCE<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. SOURCE<br/>         5. SOURCE<br/>         6. GATE<br/>         7. GATE<br/>         8. SOURCE</p>  | <p>STYLE 7:<br/>         PIN 1. INPUT<br/>         2. EXTERNAL BYPASS<br/>         3. THIRD STAGE SOURCE<br/>         4. GROUND<br/>         5. DRAIN<br/>         6. GATE 3<br/>         7. SECOND STAGE Vd<br/>         8. FIRST STAGE Vd</p>                    | <p>STYLE 8:<br/>         PIN 1. COLLECTOR, DIE #1<br/>         2. BASE, #1<br/>         3. BASE, #2<br/>         4. COLLECTOR, #2<br/>         5. COLLECTOR, #2<br/>         6. EMITTER, #2<br/>         7. EMITTER, #1<br/>         8. COLLECTOR, #1</p>                              |
| <p>STYLE 9:<br/>         PIN 1. EMITTER, COMMON<br/>         2. COLLECTOR, DIE #1<br/>         3. COLLECTOR, DIE #2<br/>         4. EMITTER, COMMON<br/>         5. EMITTER, COMMON<br/>         6. BASE, DIE #2<br/>         7. BASE, DIE #1<br/>         8. EMITTER, COMMON</p> | <p>STYLE 10:<br/>         PIN 1. GROUND<br/>         2. BIAS 1<br/>         3. OUTPUT<br/>         4. GROUND<br/>         5. GROUND<br/>         6. BIAS 2<br/>         7. INPUT<br/>         8. GROUND</p>  | <p>STYLE 11:<br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. DRAIN 2<br/>         7. DRAIN 1<br/>         8. DRAIN 1</p>   | <p>STYLE 12:<br/>         PIN 1. SOURCE<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p>STYLE 13:<br/>         PIN 1. N.C.<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>  | <p>STYLE 14:<br/>         PIN 1. N-SOURCE<br/>         2. N-GATE<br/>         3. P-SOURCE<br/>         4. P-GATE<br/>         5. P-DRAIN<br/>         6. P-DRAIN<br/>         7. N-DRAIN<br/>         8. N-DRAIN</p>   | <p>STYLE 15:<br/>         PIN 1. ANODE 1<br/>         2. ANODE 1<br/>         3. ANODE 1<br/>         4. ANODE 1<br/>         5. CATHODE, COMMON<br/>         6. CATHODE, COMMON<br/>         7. CATHODE, COMMON<br/>         8. CATHODE, COMMON</p>               | <p>STYLE 16:<br/>         PIN 1. EMITTER, DIE #1<br/>         2. BASE, DIE #1<br/>         3. EMITTER, DIE #2<br/>         4. BASE, DIE #2<br/>         5. COLLECTOR, DIE #2<br/>         6. COLLECTOR, DIE #2<br/>         7. COLLECTOR, DIE #1<br/>         8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:<br/>         PIN 1. VCC<br/>         2. V2OUT<br/>         3. V1OUT<br/>         4. TXE<br/>         5. RXE<br/>         6. VEE<br/>         7. GND<br/>         8. ACC</p>  | <p>STYLE 18:<br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. CATHODE<br/>         8. CATHODE</p>   | <p>STYLE 19:<br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. MIRROR 2<br/>         7. DRAIN 1<br/>         8. MIRROR 1</p>   | <p>STYLE 20:<br/>         PIN 1. SOURCE (N)<br/>         2. GATE (N)<br/>         3. SOURCE (P)<br/>         4. GATE (P)<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p>STYLE 21:<br/>         PIN 1. CATHODE 1<br/>         2. CATHODE 2<br/>         3. CATHODE 3<br/>         4. CATHODE 4<br/>         5. CATHODE 5<br/>         6. COMMON ANODE<br/>         7. COMMON ANODE<br/>         8. CATHODE 6</p>  | <p>STYLE 22:<br/>         PIN 1. I/O LINE 1<br/>         2. COMMON CATHODE/VCC<br/>         3. COMMON CATHODE/VCC<br/>         4. I/O LINE 3<br/>         5. COMMON ANODE/GND<br/>         6. I/O LINE 4<br/>         7. I/O LINE 5<br/>         8. COMMON ANODE/GND</p> | <p>STYLE 23:<br/>         PIN 1. LINE 1 IN<br/>         2. COMMON ANODE/GND<br/>         3. COMMON ANODE/GND<br/>         4. LINE 2 IN<br/>         5. LINE 2 OUT<br/>         6. COMMON ANODE/GND<br/>         7. COMMON ANODE/GND<br/>         8. LINE 1 OUT</p> | <p>STYLE 24:<br/>         PIN 1. BASE<br/>         2. EMITTER<br/>         3. COLLECTOR/ANODE<br/>         4. COLLECTOR/ANODE<br/>         5. CATHODE<br/>         6. CATHODE<br/>         7. COLLECTOR/ANODE<br/>         8. COLLECTOR/ANODE</p>                                      |
| <p>STYLE 25:<br/>         PIN 1. VIN<br/>         2. N/C<br/>         3. REXT<br/>         4. GND<br/>         5. IOUT<br/>         6. IOUT<br/>         7. IOUT<br/>         8. IOUT</p>   | <p>STYLE 26:<br/>         PIN 1. GND<br/>         2. dv/dt<br/>         3. ENABLE<br/>         4. ILIMIT<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. VCC</p>  | <p>STYLE 27:<br/>         PIN 1. ILIMIT<br/>         2. OVLO<br/>         3. UVLO<br/>         4. INPUT+<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. DRAIN</p>  | <p>STYLE 28:<br/>         PIN 1. SW_TO_GND<br/>         2. DASIC_OFF<br/>         3. DASIC_SW_DET<br/>         4. GND<br/>         5. V_MON<br/>         6. VBULK<br/>         7. VBULK<br/>         8. VIN</p>  |
| <p>STYLE 29:<br/>         PIN 1. BASE, DIE #1<br/>         2. EMITTER, #1<br/>         3. BASE, #2<br/>         4. EMITTER, #2<br/>         5. COLLECTOR, #2<br/>         6. COLLECTOR, #2<br/>         7. COLLECTOR, #1<br/>         8. COLLECTOR, #1</p>                        | <p>STYLE 30:<br/>         PIN 1. DRAIN 1<br/>         2. DRAIN 1<br/>         3. GATE 2<br/>         4. SOURCE 2<br/>         5. SOURCE 1/DRAIN 2<br/>         6. SOURCE 1/DRAIN 2<br/>         7. SOURCE 1/DRAIN 2<br/>         8. GATE 1</p>                           |  |  |

<b>DOCUMENT NUMBER:</b>	<b>98ASB42564B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SOIC-8 NB</b>	<b>PAGE 2 OF 2</b>

**onsemi** and **ONSEMI** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

---

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)