

NSP4201MR6

ESD and Surge Protection Device

Low Clamping Voltage Surge Protection Diode Array

The NSP4201MR6 surge protector is designed to protect high speed data lines from ESD, EFT, and lightning surges.

Features

- Protection for the Following IEC Standards:
IEC 61000-4-2 (ESD) ± 30 kV (Contact)
IEC 61000-4-5 (Lightning) 25 A (8/20 μ s)
- Low Clamping Voltage
- Low Leakage
- UL Flammability Rating of 94 V-0
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- High Speed Communication Line Protection
- USB 1.1 and 2.0 Power and Data Line Protection
- Digital Video Interface (DVI)
- Monitors and Flat Panel Displays

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Power Dissipation 8/20 μ s @ $T_A = 25^\circ\text{C}$ (Note 1)	P_{pk}	500	W
Operating Junction Temperature Range	T_J	-40 to +125	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to +150	$^\circ\text{C}$
Lead Solder Temperature – Maximum (10 Seconds)	T_L	260	$^\circ\text{C}$
IEC 61000-4-2 Air (ESD) IEC 61000-4-2 Contact (ESD)	ESD	± 30 ± 30	kV
IEC 61000-4-4 (5/50 ns)	EFT	40	A

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

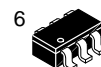
1. Non-repetitive current pulse per Figure 1 (Pin 5 to Pin 2)

See Application Note AND8308/D for further description of survivability specs.



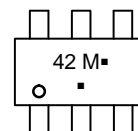
ON Semiconductor®

www.onsemi.com



6
1
TSOP-6
CASE 318G

MARKING DIAGRAM

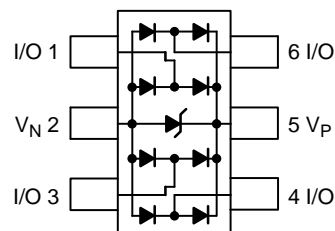


42 = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

PIN CONFIGURATION AND SCHEMATIC



ORDERING INFORMATION

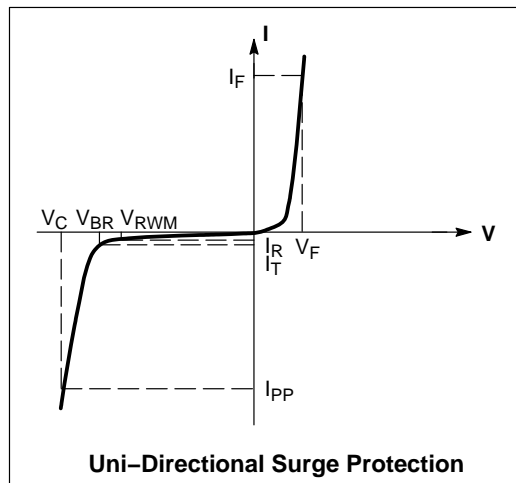
Device	Package	Shipping
NSP4201MR6T1G	TSOP-6 (Pb-Free)	3000 / Tape & Reel
SZNSP4201MR6T1G	TSOP-6 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F
P_{pk}	Peak Power Dissipation
C	Capacitance @ $V_R = 0$ and $f = 1.0$ MHz



*See Application Note AND8308/D for detailed explanations of datasheet parameters.

ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	(Note 2)			5.0	V
Breakdown Voltage	V_{BR}	$I_T=1$ mA, (Note 3)	6.0			V
Reverse Leakage Current	I_R	$V_{RWM} = 5$ V			1.0	μA
Clamping Voltage ($t_p = 8/20$ μs per Figure 1)	V_C	$I_{PP} = 1$ A, Any I/O to GND			8.5	V
		$I_{PP} = 5$ A, Any I/O to GND			9.0	
		$I_{PP} = 8$ A, Any I/O to GND			10	
		$I_{PP} = 25$ A, Any I/O to GND			12	
Junction Capacitance	C_J	$V_R = 0$ V, $f=1$ MHz between I/O Pins and GND		3.0	5.0	pF
Junction Capacitance	C_J	$V_R = 0$ V, $f=1$ MHz between I/O Pins		1.5	3.0	pF

- Surge protection devices are normally selected according to the working peak reverse voltage (V_{RWM}), which should be equal or greater than the DC or continuous peak operating voltage level.
- V_{BR} is measured at pulse test current I_T .

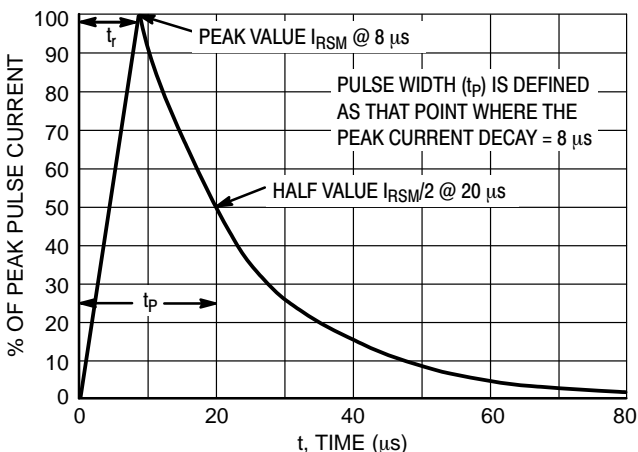


Figure 1. IEC61000-4-5 8/20 μs Pulse Waveform

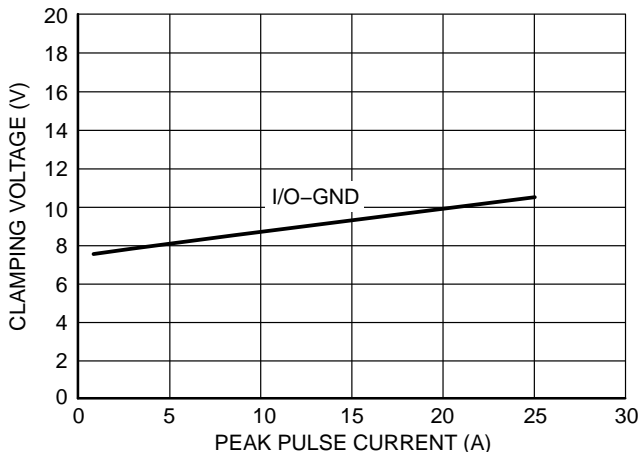


Figure 2. Clamping Voltage vs. Peak Pulse Current ($t_p = 8/20$ μs per Figure 1)

NSP4201MR6

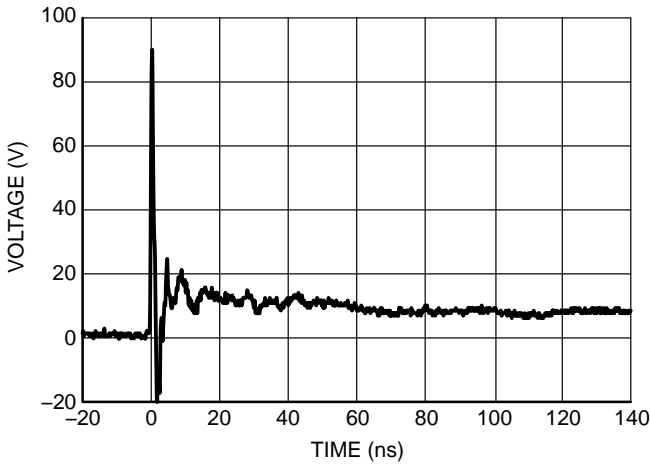


Figure 3. IEC61000-4-2 +8 kV Contact Clamping Voltage

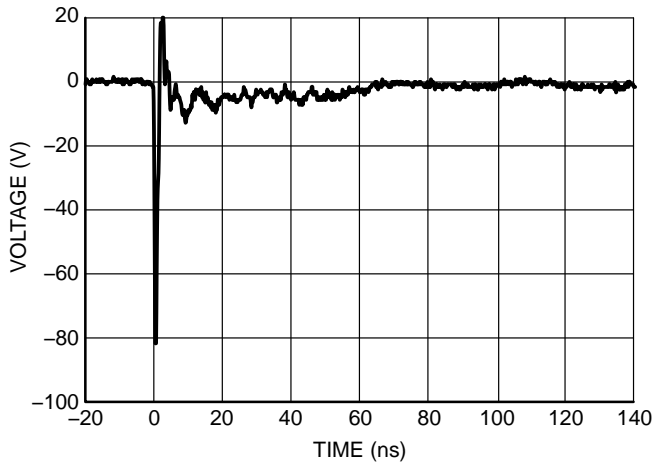


Figure 4. IEC61000-4-2 -8 kV Contact Clamping Voltage

IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

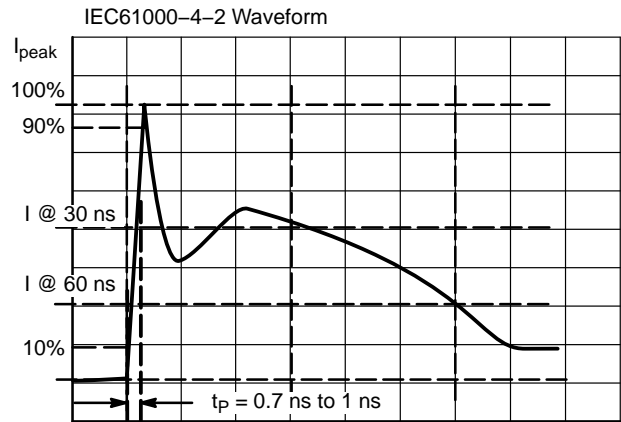


Figure 5. IEC61000-4-2 Spec

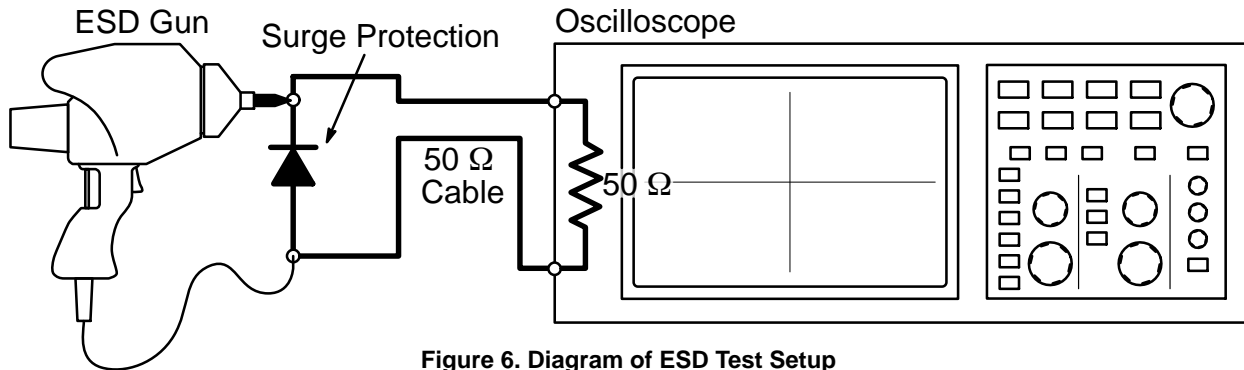


Figure 6. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

NSP4201MR6

TYPICAL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise noted)

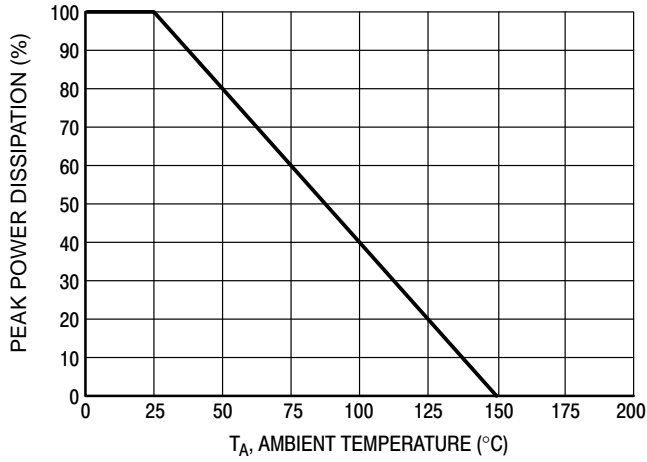


Figure 7. Pulse Derating Curve

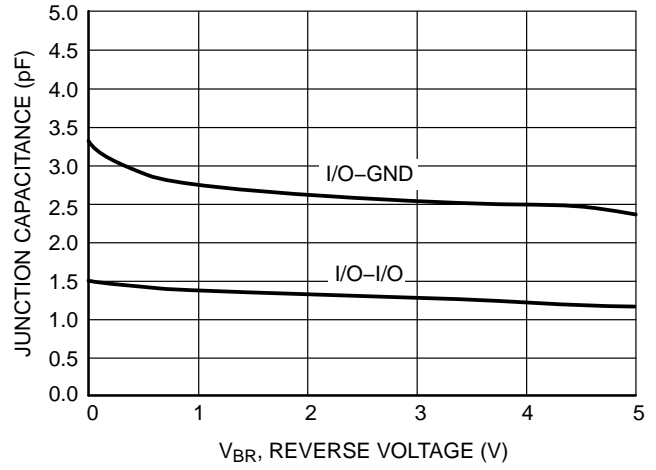


Figure 8. Junction Capacitance vs Reverse Voltage

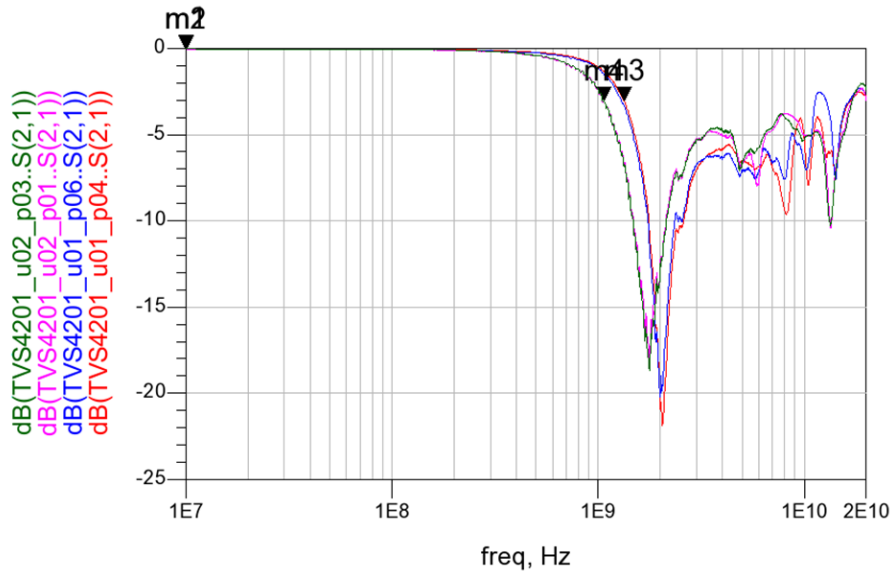


Figure 9. RF Insertion Loss

NSP4201MR6

TYPICAL APPLICATIONS

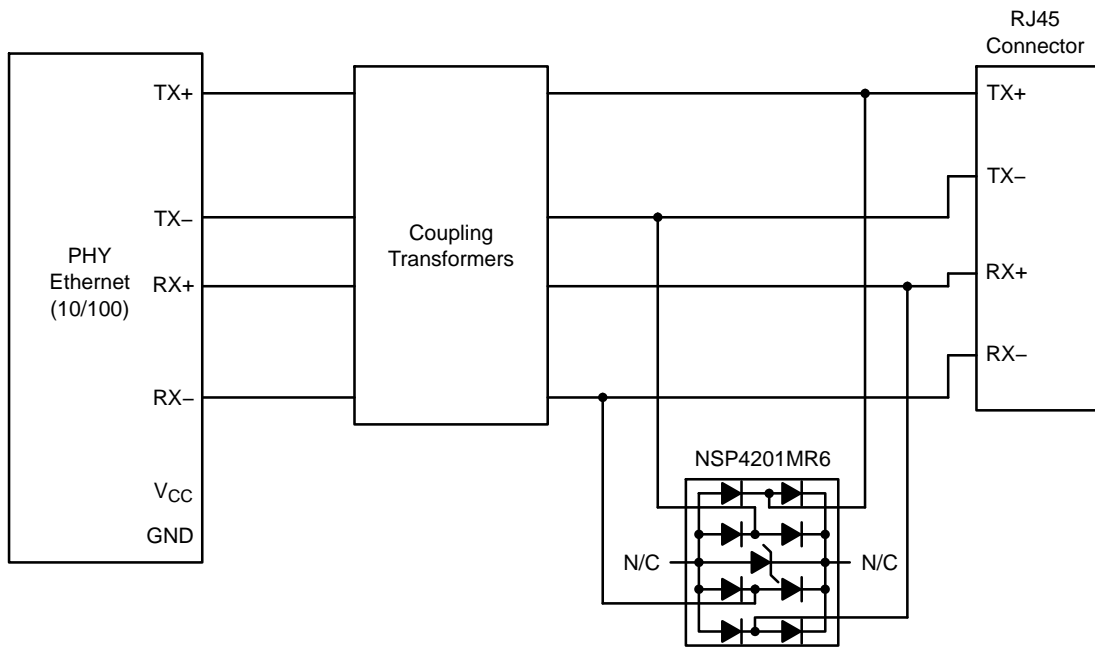


Figure 10. Protection for Ethernet 10/100 (Differential mode)

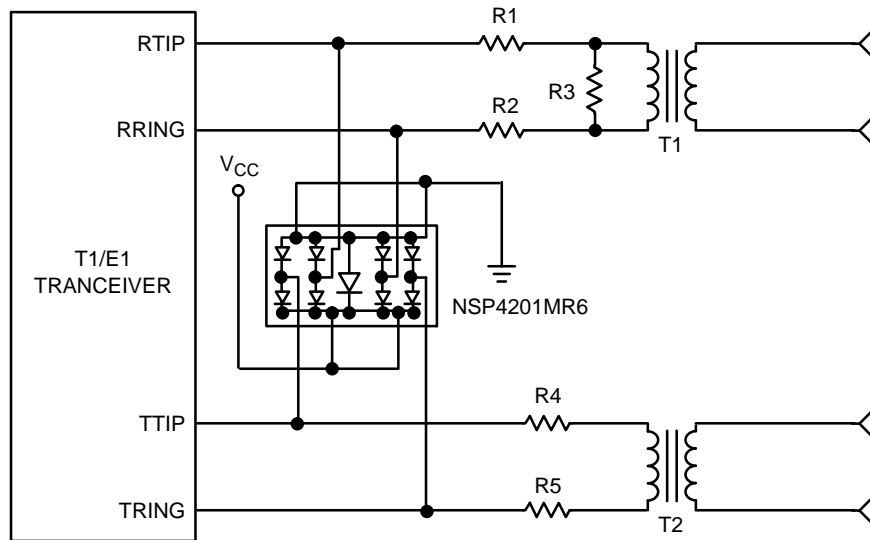


Figure 11. T1/E1 Interface Protection

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

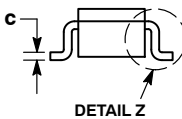
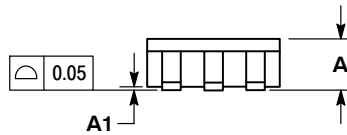
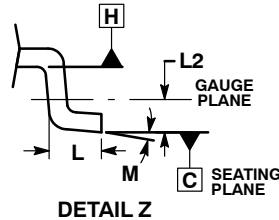
ON Semiconductor®



SCALE 2:1

TSOP-6 CASE 318G-02 ISSUE V

DATE 12 JUN 2012



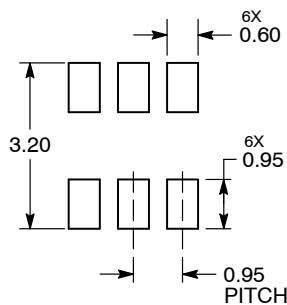
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	-	10°

- | | | | | | |
|--|--|---|---|---|--|
| <p>STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN</p> | <p>STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2</p> | <p>STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out</p> | <p>STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD</p> | <p>STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2</p> | <p>STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR</p> |
| <p>STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER</p> | <p>STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND</p> | <p>STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE</p> | <p>STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)-
4. D(IN)-
5. VBUS
6. D(IN)+</p> | <p>STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2</p> | <p>STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O</p> |
| <p>STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1</p> | <p>STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN</p> | <p>STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE</p> | <p>STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE</p> | <p>STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR</p> | |

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



- | | |
|--|---|
| <p>XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb-Free Package</p> | <p>XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package</p> |
|--|---|

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

DOCUMENT NUMBER:	98ASB14888C	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TSOP-6	PAGE 1 OF 1

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

ON Semiconductor Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:
Voice Mail: 1 800-282-9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative