

NLU1GT125

Non-Inverting 3-State Buffer, TTL Level LSTTL-Compatible Inputs

The NLU1GT125 MiniGate™ is an advanced CMOS high-speed non-inverting buffer in ultra-small footprint.

The NLU1GT125 requires the 3-state control input \overline{OE} to be set High to place the output in the high impedance state.

The device input is compatible with TTL-type input thresholds and the output has a full 5.0 V CMOS level output swing.

The NLU1GT125 input and output structures provide protection when voltages up to 7.0 V are applied, regardless of the supply voltage.

Features

- High Speed: $t_{PD} = 3.8 \text{ ns (Typ) @ } V_{CC} = 5.0 \text{ V}$
- Low Power Dissipation: $I_{CC} = 1 \mu\text{A (Max) at } T_A = 25^\circ\text{C}$
- TTL-Compatible Input: $V_{IL} = 0.8 \text{ V; } V_{IH} = 2.0 \text{ V}$
- CMOS-Compatible Output:
 $V_{OH} > 0.8 V_{CC}; V_{OL} < 0.1 V_{CC} @ \text{Load}$
- Power Down Protection Provided on inputs
- Balanced Propagation Delays
- Ultra-Small Packages
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These are Pb-Free Devices

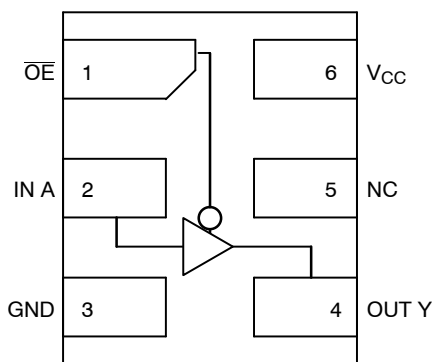


Figure 1. Pinout (Top View)



Figure 2. Logic Symbol

FUNCTION TABLE

| Input | | Output |
|-------|-----------------|--------|
| A | \overline{OE} | Y |
| L | L | L |
| H | L | H |
| X | H | Z |

PIN ASSIGNMENT

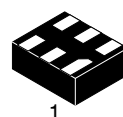
| | |
|---|-----------------|
| 1 | \overline{OE} |
| 2 | IN A |
| 3 | GND |
| 4 | OUT Y |
| 5 | NC |
| 6 | V_{CC} |



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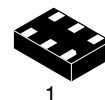
MARKING DIAGRAMS



UDFN6
1.2 x 1.0
CASE 517AA



UDFN6
1.0 x 1.0
CASE 517BX



UDFN6
1.45 x 1.0
CASE 517AQ



7 = Device Marking
M = Date Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

NLU1GT125

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---------------|--|----------------------|-------------|
| V_{CC} | DC Supply Voltage | -0.5 to +7.0 | V |
| V_{IN} | DC Input Voltage | -0.5 to +7.0 | V |
| V_{OUT} | DC Output Voltage | -0.5 to +7.0 | V |
| I_{IK} | DC Input Diode Current $V_{IN} < GND$ | -20 | mA |
| I_{OK} | DC Output Diode Current $V_{OUT} < GND$ | ± 20 | mA |
| I_O | DC Output Source/Sink Current | ± 12.5 | mA |
| I_{CC} | DC Supply Current Per Supply Pin | ± 25 | mA |
| I_{GND} | DC Ground Current per Ground Pin | ± 25 | mA |
| T_{STG} | Storage Temperature Range | -65 to +150 | $^{\circ}C$ |
| T_L | Lead Temperature, 1 mm from Case for 10 Seconds | 260 | $^{\circ}C$ |
| T_J | Junction Temperature Under Bias | 150 | $^{\circ}C$ |
| MSL | Moisture Sensitivity | Level 1 | |
| F_R | Flammability Rating Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in | |
| $I_{LATCHUP}$ | Latchup Performance Above V_{CC} and Below GND at 125 $^{\circ}C$ (Note 2) | ± 500 | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow.
2. Tested to EIA / JESD78.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---------------------|--|--------|-----------|-------------|
| V_{CC} | Positive DC Supply Voltage | 1.65 | 5.5 | V |
| V_{IN} | Digital Input Voltage | 0 | 5.5 | V |
| V_{OUT} | Output Voltage | 0 | 5.5 | V |
| T_A | Operating Free-Air Temperature | -55 | +125 | $^{\circ}C$ |
| $\Delta t/\Delta V$ | Input Transition Rise or Fall Rate $V_{CC} = 3.3 V \pm 0.3 V$ $V_{CC} = 5.0 V \pm 0.5 V$ | 0 0 | 100 20 | ns/V |

NLU1GT125

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | V _{CC} (V) | T _A = 25 °C | | | T _A = +85°C | | T _A = -55°C to +125°C | | Unit |
|--------------------|---------------------------|--|---------------------|------------------------|------------|--------------|------------------------|--------------|----------------------------------|--------------|------|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| V _{IH} | Low-Level Input Voltage | | 3.0 4.5 to 5.5 | 1.4 2.0 | | | 1.4 2.0 | | 1.4 2.0 | | V |
| V _{IL} | Low-Level Input Voltage | | 3.0 4.5 to 5.5 | | | 0.53 0.8 | | 0.53 0.8 | | 0.53 0.8 | V |
| V _{OH} | High-Level Output Voltage | V _{IN} = V _{IH} or V _{IL} I _{OH} = -50 μA | 3.0 4.5 | 2.9 4.4 | 3.0 4.5 | | 2.9 4.4 | | 2.9 4.4 | | V |
| | | V _{IN} = V _{IH} or V _{IL} I _{OH} = -4 mA I _{OH} = -8 mA | 3.0 4.5 | 2.58 3.94 | | | 2.48 3.80 | | 2.34 3.66 | | |
| V _{OL} | Low-Level Output Voltage | V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 μA | 3.0 4.5 | | 0 0 | 0.1 0.1 | | 0.1 0.1 | | 0.1 0.1 | V |
| | | V _{IN} = V _{IH} or V _{IL} I _{OL} = 4 mA I _{OL} = 8 mA | 3.0 4.5 | | | 0.36 0.36 | | 0.44 0.44 | | 0.52 0.52 | |
| I _{IN} | Input Leakage Current | 0 ≤ V _{IN} ≤ 5.5 V | 0 to 5.5 | | | ±0.1 | | ±1.0 | | ±1.0 | μA |
| I _{CC} | Quiescent Supply Current | 0 ≤ V _{IN} ≤ V _{CC} | 5.5 | | | 1.0 | | 20 | | 40 | μA |
| I _{CC(T)} | Quiescent Supply Current | V _{IN} = 3.4 V Other Input: V _{CC} or GND | 5.5 | | | 1.35 | | 1.50 | | 1.65 | mA |
| I _{OPD} | Output Leakage Current | V _{OUT} = 5.5 V | 0.0 | | | 0.5 | | 5.0 | | 10 | μA |
| I _{OZ} | 3-State Leakage Current | V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND | 0.0 | | | ±0.25 | | ±2.5 | | ±2.5 | μA |

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0 ns)

| Symbol | Parameter | V _{CC} (V) | Test Condition | T _A = 25 °C | | | T _A = +85°C | | T _A = -55°C to +125°C | | Unit |
|--|--|---------------------|--|------------------------|------------|-------------|------------------------|--------------|----------------------------------|--------------|------|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| t _{PLH} , t _{PHL} | Propagation Delay, A to Y (Figures 3 and 5) | 3.0 to 3.6 | C _L = 15 pF C _L = 50 pF | | 5.6 8.1 | 8.0 11.5 | 1.0 1.0 | 9.5 13.0 | | 12.0 16.0 | ns |
| | | 4.5 to 5.5 | C _L = 15 pF C _L = 50 pF | | 3.8 5.3 | 5.5 7.5 | 1.0 1.0 | 6.5 8.5 | | 8.5 10.5 | |
| t _{PZL} , t _{PZH} | Output Enable Time, \overline{OE} to Y (Figures 4 and 6) | 3.0 to 3.6 | C _L = 15 pF C _L = 50 pF | | 5.4 7.9 | 8.0 11.5 | 1.0 1.0 | 9.5 13.0 | | 11.5 15.0 | ns |
| | | 4.5 to 5.5 | C _L = 15 pF C _L = 50 pF | | 3.6 5.1 | 5.1 7.1 | 1.0 1.0 | 6.0 8.0 | | 7.5 9.5 | |
| t _{PLZ} , t _{PHZ} | Output Disable Time, \overline{OE} to Y (Figures 4 and 6) | 3.0 to 3.6 | C _L = 15 pF C _L = 50 pF | | 6.5 8.0 | 9.7 13.2 | 1.0 1.0 | 11.5 15.0 | | 14.5 18.5 | ns |
| | | 4.5 to 5.5 | C _L = 15 pF C _L = 50 pF | | 4.8 7.0 | 6.8 8.8 | 1.0 1.0 | 8.0 10.0 | | 10.0 12.0 | |
| C _{IN} | Input Capacitance | | | | 4 | 10 | | 10 | | 10.0 | pF |
| C _{OUT} | 3-State Output Capacitance (Output in High Impedance State) | | | | 6 | | | | | | pF |
| C _{PD} | Power Dissipation Capacitance (Note 3) | 5.0 | | | 14 | | | | | | pF |

3. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption: P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

NLU1GT125

SWITCHING WAVEFORMS

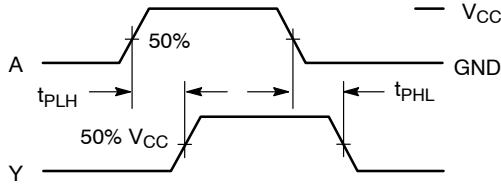


Figure 3. Switching Waveforms

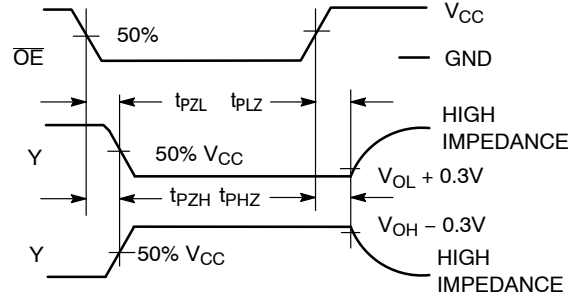


Figure 4.

MiniGate is a trademark of Semiconductor Components Industries, LLC (SCILLC).

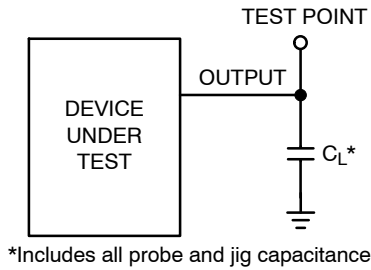


Figure 5. Test Circuit

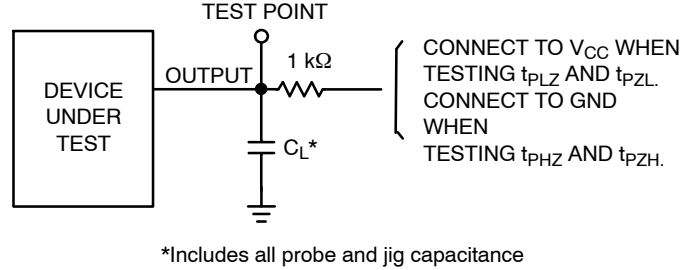


Figure 6. Test Circuit

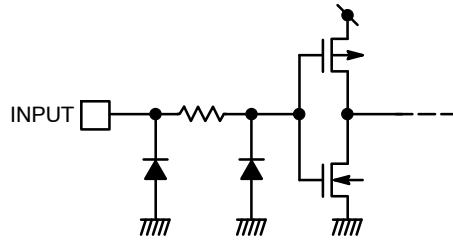


Figure 7. Input Equivalent Circuit

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|------------------------------------|-----------------------------------|-----------------------|
| NLU1GT125MUTCG | UDFN6, 1.2 x 1.0, 0.4P (Pb-Free) | 3000 / Tape & Reel |
| NLU1GT125AMUTCG, NLVU1GT125AMUTCG* | UDFN6, 1.45 x 1.0, 0.5P (Pb-Free) | 3000 / Tape & Reel |
| NLU1GT125CMUTCG | UDFN6, 1.0 x 1.0, 0.35P (Pb-Free) | 3000 / Tape & Reel |

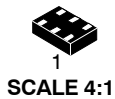
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

MECHANICAL CASE OUTLINE

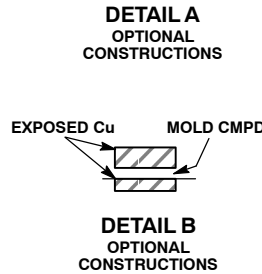
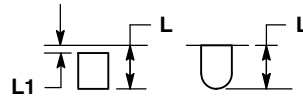
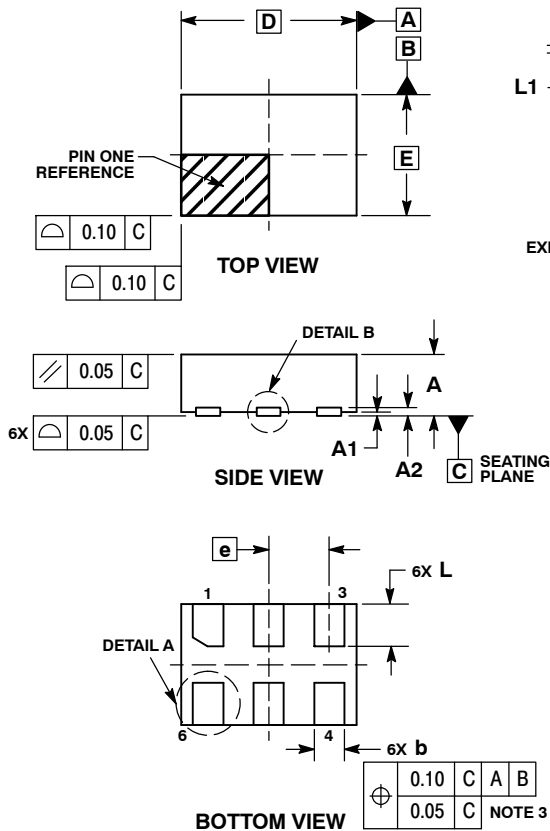
PACKAGE DIMENSIONS

ON Semiconductor®



UDFN6, 1.45x1.0, 0.5P
CASE 517AQ-01
ISSUE O

DATE 15 MAY 2008



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

| MILLIMETERS | | |
|-------------|------|------|
| DIM | MIN | MAX |
| A | 0.45 | 0.55 |
| A1 | 0.00 | 0.05 |
| A2 | 0.07 | REF |
| b | 0.20 | 0.30 |
| D | 1.45 | BSC |
| E | 1.00 | BSC |
| e | 0.50 | BSC |
| L | 0.30 | 0.40 |
| L1 | --- | 0.15 |

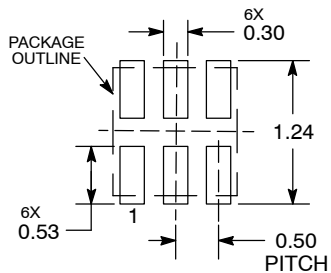
GENERIC MARKING DIAGRAM*



- X = Specific Device Code
- M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present.

MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
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| DESCRIPTION: | UDFN6, 1.45X1.0, 0.5P | PAGE 1 OF 2 |

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