NLSX4378A

4-Bit 24 Mb/s Dual-Supply Level Translator

The NLSX4378A is a 4−bit configurable dual−supply bidirectional auto sensing translator that does not require a directional control pin. The V_{CC} I/O and V_L I/O ports are designed to track two different power supply rails, V_{CC} and V_L respectively. The V_{CC} and V_L supply rails are configurable from 1.65 V to 5.5 V. This allows voltage logic signals on the V_L side to be translated into lower, higher or equal value voltage logic signals on the V_{CC} side, and vice−versa.

The NLSX4378A translator has open−drain outputs with integrated 10 kΩ pullup resistors on the I/O lines. The integrated pullup resistors are used to pullup the I/O lines to either V_L or V_{CC}. The NLSX4378A is an excellent match for open−drain applications such as the I^2C communication bus.

Features

- V_L can be Less than, Greater than or Equal to V_{CC}
- Wide V_{CC} Operating Range: 1.65 V to 5.5 V
  Wide V_L Operating Range: 1.65 V to 5.5 V
- High−Speed with 24 Mb/s Guaranteed Date Rate
- Low Bit−to−Bit Skew
- Enable Input is Overvoltage Tolerant (OVT) to 5.5 V
- Nonpreferential Powerup Sequencing
- Integrated 10 kΩ Pullup Resistors
- ESD Protection: >7 kV HBM for all pins
- Small Space Saving Package − 2.02 x 1.54 mm µBump12
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- I^2C, SMBus, PMBus
- Low Voltage ASIC Level Translation
- Mobile Phones, PDAs, Cameras

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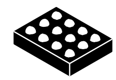


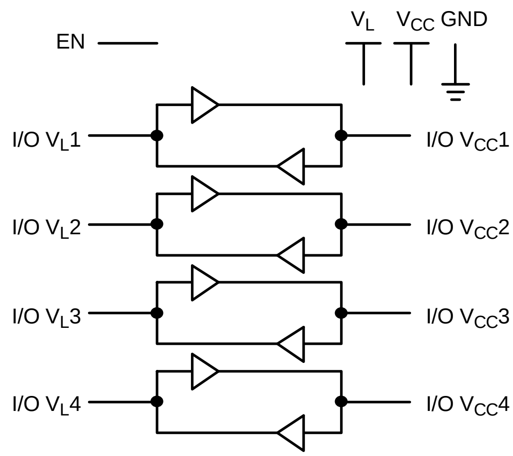
µBump12
FC SUFFIX
CASE 499AU

MARKING DIAGRAM

S4378AB
AYWW
▪

A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

LOGIC DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

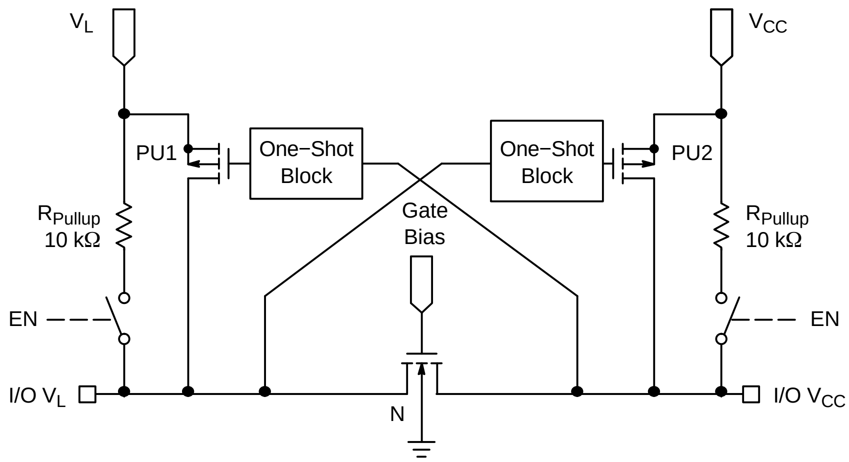


Figure 1. Block Diagram (1 I/O Line)

PIN ASSIGNMENT

Pins	Description
V_{CC}	V_{CC} Input Voltage
V_L	V_L Input Voltage
GND	Ground
EN	Output Enable
I/O V_{CC}n	V_{CC} I/O Port, Referenced to V_{CC}
I/O V_Ln	V_L I/O Port, Referenced to V_L

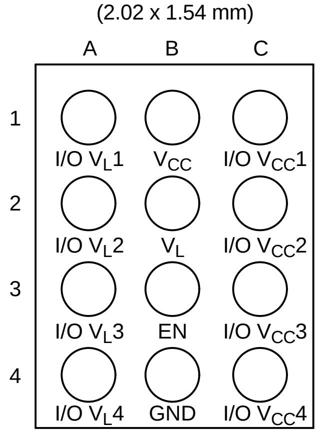
FUNCTION TABLE

EN	Operating Mode
L	Hi−Z
H	I/O Buses Connected

PIN LOCATION

Pin	Pin Name
A1	I/O V_L1
A2	I/O V_L2
A3	I/O V_L3
A4	I/O VL4
B1	V_{CC}
B2	V_L
B3	EN
B4	GND
C1	I/O V_{CC}1
C2	I/O V_{CC}2
C3	I/O V_{CC}3
C4	I/O V_{CC}4

µBump12
(2.02 x 1.54 mm)



(Bottom View)

MAXIMUM RATINGS

Symbol	Parameter	Condition	Value	Unit
V_{CC}	DC Supply Voltage		−0.3 to +7.0	V
V_L	DC Supply Voltage		−0.3 to +7.0	V
I/O V_{CC}	V_{CC}−Referenced DC Input/Output Voltage		−0.3 to (V_{CC} + 0.3)	V
I/O V_L	V_L−Referenced DC Input/Output Voltage		−0.3 to (V_L + 0.3)	V
V_{EN}	Enable Control Pin DC Input Voltage		−0.3 to +7.0	V
I_{I/O_SC}	Short−Circuit Duration (I/O V_L and I/O V_{CC} to GND)	Continuous	40	mA
T_{STG}	Storage Temperature		−65 to +150	°C
I_{LU}	Latch−up Current		100	mA
ESD Rating	Human Body Model Charged Device Model		7000 2000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	1.65	5.5	V
V_L	DC Supply Voltage	1.65	5.5	V
V_{EN}	Enable Control Pin Voltage	GND	5.5	V
V_{IO}	I/O Pin Voltage	GND	V_{CC} or V_L	V
T_A	Operating Temperature Range	−55	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 1.65 V to 5.5 V and V_L = 1.65 V to 5.5 V, unless otherwise specified)

Symbol	Parameter	Test Conditions	−40°C to +85°C Min	−40°C to +85°C Typ (Notes 1, 2)	−40°C to +85°C Max	−55°C to +125°C Min	−55°C to +125°C Max	Unit
V_{IHC}	I/O V_{CC} Input HIGH Voltage		V_{CC} − 0.4	–	–	V_{CC} − 0.4	–	V
V_{ILC}	I/O V_{CC} Input LOW Voltage		–	–	0.15	–	0.15	V
V_{IHL}	I/O V_L Input HIGH Voltage		V_L − 0.4	–	–	V_L − 0.4	–	V
V_{ILL}	I/O V_L Input LOW Voltage		–	–	0.15	–	0.15	V
V_{IH}	Control Pin Input HIGH Voltage		0.65 * V_L	–	–	0.65 * V_L	–	V
V_{IL}	Control Pin Input LOW Voltage		–	–	0.35 * V_L	–	0.35 * V_L	V
V_{OHC}	I/O V_{CC} Output HIGH Voltage	I/O V_{CC} Source Current = 20 μA	0.8 * V_{CC}	–	–	0.8 * V_{CC}	–	V
V_{OLC}	I/O V_{CC} Output LOW Voltage	I/O V_{CC} Sink Current = 1.0 mA, I/O_V_L ≤ 0.15 V	–	–	0.4	–	0.4	V
V_{OHL}	I/O V_L Output HIGH Voltage	I/O V_L Source Current = 20 μA	0.8 * V_L	–	–	0.8 * V_L	–	V
V_{OLL}	I/O V_L Output LOW Voltage	I/O V_L Sink Current = 1.0 mA, I/O_V_{CC} ≤ 0.15 V	–	–	0.4	–	0.4	V
I_{QVCC}	V_{CC} Supply Current	I/O V_{CC} and I/O V_L Unconnected, V_{EN} = V_L	–	0.5	2.0	–	3.0	μA
I_{QVL}	V_L Supply Current	I/O V_{CC} and I/O V_L Unconnected, V_{EN} = V_L	–	0.3	1.0	–	3.0	μA
I_{TS-VCC}	V_{CC} Tristate Output Mode Supply Current	I/O V_{CC} and I/O V_L Unconnected, V_{EN} = GND	–	0.1	1.0	–	1.5	μA
I_{TS-VL}	V_L Tristate Output Mode Supply Current	I/O V_{CC} and I/O V_L Unconnected, V_{EN} = GND	–	0.1	1.0	–	1.5	μA
I_{OZ}	I/O Tristate Output Mode Leakage Current	T_A = +25°C	–	0.1	1.0	–	1.0	μA
R_{PU}	Pullup Resistor I/O V_L and V_{CC}	T_A = +25°C	–	10	–	–	–	kΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Typical values are for V_{CC} = +2.8 V, V_L = +1.8 V and T_A = +25°C.
2. All units are production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

TIMING CHARACTERISTICS − RAIL−TO−RAIL DRIVING CONFIGURATIONS

(I/O test circuit of Figures 2 and 3, C_{LOAD} = 15 pF, driver output impedance ≤ 50 Ω, R_{LOAD} = 1 MΩ)

Symbol	Parameter	Test Conditions	−40°C to +85°C (Note 3) Min	Typ	Max	−55°C to +125°C (Note 3) Min	Max	Unit
V_L = 1.65 V, V_{CC} = 5.5 V								
t_{RVCC}	I/O V_{CC} Risetime				15		15	ns
t_{FVCC}	I/O V_{CC} Falltime				30		30	ns
t_{RVL}	I/O V_L Risetime				30		30	ns
t_{FVL}	I/O V_L Falltime				10		10	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L)				20		20	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC})				20		20	ns
t_{SKEW}	Channel−to−Channel Skew				5		5	nS
MDR	Maximum Data Rate		24			24		Mb/s
V_L = 1.8 V, V_{CC} = 2.8 V								
t_{RVCC}	I/O V_{CC} Risetime				15		15	ns
t_{FVCC}	I/O V_{CC} Falltime				15		15	ns
t_{RVL}	I/O V_L Risetime				25		25	ns
t_{FVL}	I/O V_L Falltime				10		10	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L)				15		15	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC})				15		15	ns
t_{SKEW}	Channel−to−Channel Skew				5		5	nS
MDR	Maximum Data Rate		24			24		Mb/s
V_L = 2.5 V, V_{CC} = 3.6 V								
t_{RVCC}	I/O V_{CC} Risetime				15		15	ns
t_{FVCC}	I/O V_{CC} Falltime				10		10	ns
t_{RVL}	I/O V_L Risetime				15		15	ns
t_{FVL}	I/O V_L Falltime				10		10	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L)				15		15	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC})				15		15	ns
t_{SKEW}	Channel−to−Channel Skew				5		5	nS
MDR	Maximum Data Rate		24			24		Mb/s
V_L = 2.8 V, V_{CC} = 1.8 V								
t_{RVCC}	I/O V_{CC} Risetime				25		25	ns
t_{FVCC}	I/O V_{CC} Falltime				10		10	ns
t_{RVL}	I/O V_L Risetime				15		15	ns
t_{FVL}	I/O V_L Falltime				15		15	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L)				15		15	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC})				15		15	ns
t_{SKEW}	Channel−to−Channel Skew				5		5	nS
MDR	Maximum Data Rate		24			24		Mb/s

3. Limits over the operating temperature range are guaranteed by design.

TIMING CHARACTERISTICS − RAIL−TO−RAIL DRIVING CONFIGURATIONS

(I/O test circuit of Figures 2 and 3, C_{LOAD} = 15 pF, driver output impedance ≤ 50 Ω, R_{LOAD} = 1 MΩ)

Symbol	Parameter	Test Conditions	−40°C to +85°C (Note 3)			−55°C to +125°C (Note 3)		Unit
			Min	Typ	Max	Min	Max	
V_L = 3.6 V, V_{CC} = 2.5 V								
t_{RVCC}	I/O V_{CC} Risetime				15		15	ns
t_{FVCC}	I/O V_{CC} Falltime				10		10	ns
t_{RVL}	I/O V_L Risetime				15		15	ns
t_{FVL}	I/O V_L Falltime				10		10	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L)				15		15	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC})				15		15	ns
t_{SKEW}	Channel−to−Channel Skew				5		5	nS
MDR	Maximum Data Rate		24			24		Mb/s
V_L = 5.5 V, V_{CC} = 1.65 V								
t_{RVCC}	I/O V_{CC} Risetime				30		30	ns
t_{FVCC}	I/O V_{CC} Falltime				10		10	ns
t_{RVL}	I/O V_L Risetime				15		15	ns
t_{FVL}	I/O V_L Falltime				30		30	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L)				20		20	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC})				20		20	ns
t_{SKEW}	Channel−to−Channel Skew				5		5	nS
MDR	Maximum Data Rate		24			24		Mb/s

3. Limits over the operating temperature range are guaranteed by design.

TIMING CHARACTERISTICS − OPEN DRAIN DRIVING CONFIGURATIONS

(I/O test circuit of Figures 4 and 5, C_{LOAD} = 15 pF, driver output impedance ≤ 50 Ω, R_{LOAD} = 1 MΩ)

Symbol	Parameter	Test Conditions	−40°C to +85°C (Note 4)			−55°C to +125°C (Note 4)		Unit
			Min	Typ	Max	Min	Max	
+1.65 ≤ V_L, V_{CC} ≤ +5.5 V								
t_{RVCC}	I/O V_{CC} Risetime				400		400	ns
t_{FVCC}	I/O V_{CC} Falltime				50		50	ns
t_{RVL}	I/O V_L Risetime				400		400	ns
t_{FVL}	I/O V_L Falltime				60		60	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L)				1000		1000	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC})				1000		1000	ns
t_{SKEW}	Channel−to−Channel Skew				50		50	nS
MDR	Maximum Data Rate		2			2		Mb/s

4. Limits over the operating temperature range are guaranteed by design.

TEST SETUPS

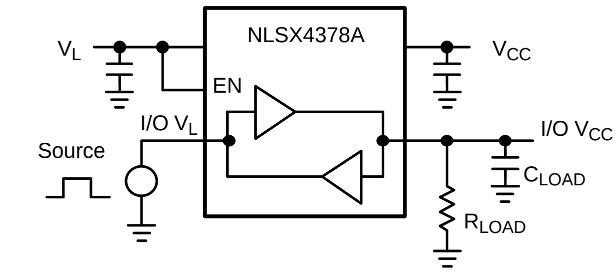


Figure 2. Rail−to−Rail Driving I/O V_L

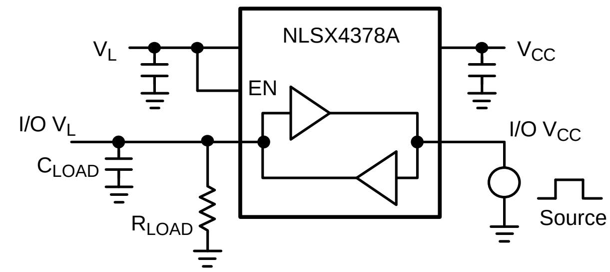


Figure 3. Rail−to−Rail Driving I/O V_{CC}

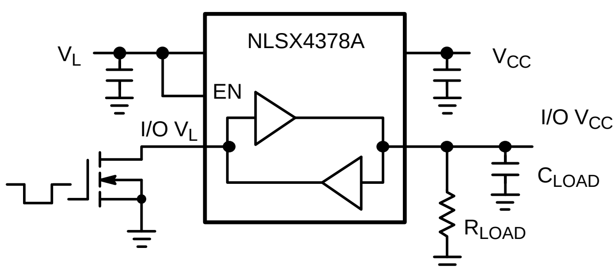


Figure 4. Open−Drain Driving I/O V_L

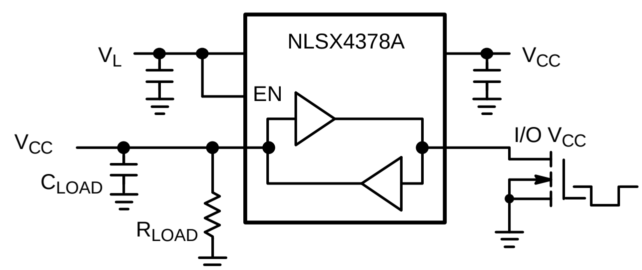


Figure 5. Open−Drain Driving I/O V_{CC}

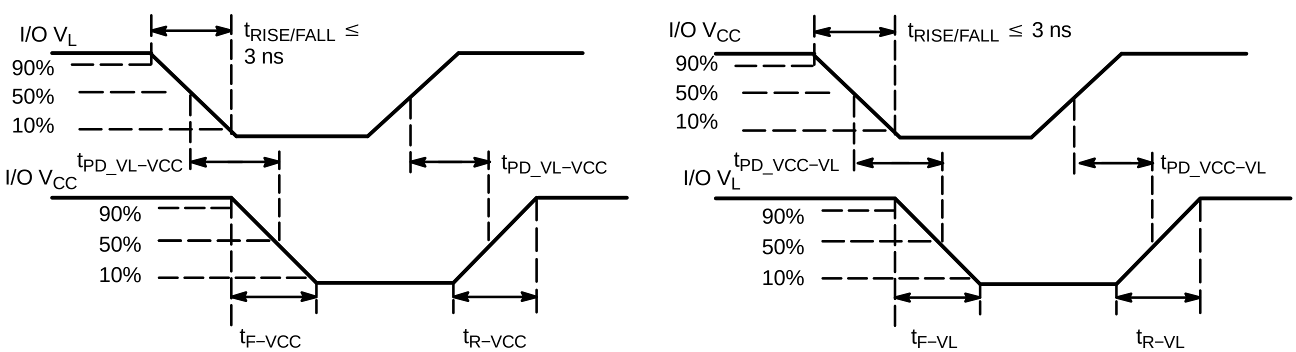


Figure 6. Definition of Timing Specification Parameters

APPLICATIONS INFORMATION

Level Translator Architecture

The NLSX4378A auto sense translator provides bi−directional voltage level shifting to transfer data in multiple supply voltage systems. This device has two supply voltages, V_L and V_{CC}, which set the logic levels on the input and output sides of the translator. When used to transfer data from the V_L to the V_{CC} ports, input signals referenced to the V_L supply are translated to output signals with a logic level matched to V_{CC}. In a similar manner, the V_{CC} to V_L translation shifts input signals with a logic level compatible to V_{CC} to an output signal matched to V_L.

The NLSX4378A consists of four bi−directional channels that independently determine the direction of the data flow without requiring a directional pin. The one−shot circuits are used to detect the rising input signals. In addition, the one shots decrease the rise time of the output signal for low−to−high transitions.

Each input/output pin has an internal 10 kΩ pull−up resistor. The magnitude of the pull−up resistors can be reduced by connecting external resistors in parallel to the internal 10 kΩ resistors.

Input Driver Requirements

The rise (t_R) and fall (t_F) timing parameters of the open drain outputs depend on the magnitude of the pull−up resistors. In addition, the propagation times (t_{PD}), skew (t_{SKEW}) and maximum data rate depend on the impedance of the device that is connected to the translator. The timing parameters listed in the data sheet assume that the output impedance of the drivers connected to the translator is less than 50 Ω.

Enable Input (EN)

The NLSX4378A has an Enable pin (EN) that provides tri−state operation at the I/O pins. Driving the Enable pin to a low logic level minimizes the power consumption of the device and drives the I/O V_{CC} and I/O V_L pins to a high impedance state. Normal translation operation occurs when the EN pin is equal to a logic high signal. The EN pin is referenced to the V_L supply and has Overvoltage Tolerant (OVT) protection.

Power Supply Guidelines

During normal operation, supply voltage V_L can be greater than, less than or equal to V_{CC}. The sequencing of the power supplies will not damage the device during the power up operation.

For optimal performance, 0.01 μF to 0.1 μF decoupling capacitors should be used on the V_L and V_{CC} power supply pins. Ceramic capacitors are a good design choice to filter and bypass any noise signals on the voltage lines to the ground plane of the PCB. The noise immunity will be maximized by placing the capacitors as close as possible to the supply and ground pins, along with minimizing the PCB connection traces.

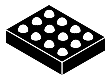
ORDERING INFORMATION

Device	Package	Shipping†
NLSX4378ABFCT1G	μBump12 (Backside Laminate Coating) (Pb−Free)	3000 / Tape & Reel

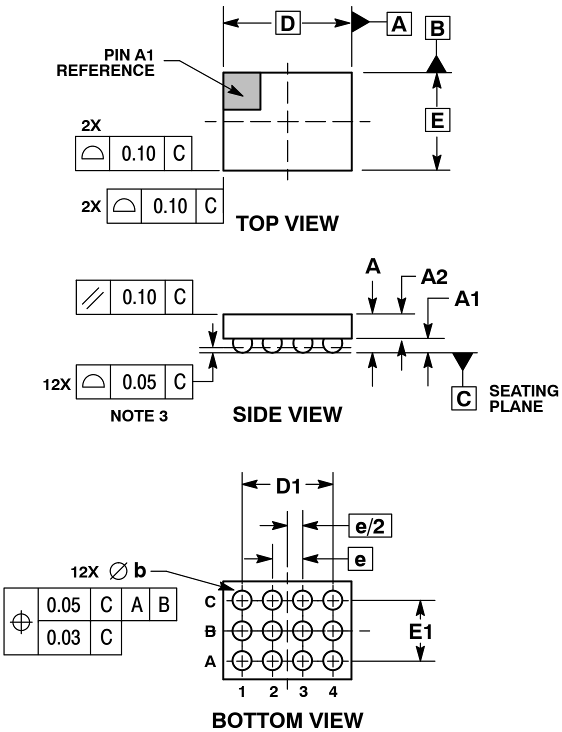
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

12 PIN FLIP−CHIP, 2.02x1.54, 0.5P
CASE 499AU−01
ISSUE O

DATE 19 MAR 2007



SCALE 4:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.66
A1	0.21	0.27
A2	0.33	0.39
b	0.29	0.34
D	2.02 BSC	
D1	1.50 BSC	
E	1.54 BSC	
E1	1.00 BSC	
e	0.50 BSC	

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DESCRIPTION:	**12 PIN FLIP−CHIP, 2.02 X 1.54, 0.5P**	**PAGE 1 OF 1**

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