

# 2-Bit 20 Mb/s Dual-Supply Level Translator

## NLSX0102

The NLSX0102 is a 2-bit configurable dual-supply bidirectional auto sensing translator that does not require a directional control pin. The I/O  $V_{CC}$  and I/O  $V_L$  ports are designed to track two different power supply rails,  $V_{CC}$  and  $V_L$  respectively. Both the  $V_{CC}$  and  $V_L$  supply rails are configurable from 1.65 V to 5.5 V. This allows voltage logic signals on the  $V_L$  side to be translated into voltage logic signals on the  $V_{CC}$  side, and vice-versa.

The NLSX0102 translator has integrated 10 k $\Omega$  pull-up resistors on the I/O lines. The integrated pull-up resistors are used to pull-up the I/O lines to either  $V_L$  or  $V_{CC}$ . The NLSX0102 is an excellent match for open-drain applications such as the I<sup>2</sup>C communication bus.

### Features

- Wide  $V_{CC}$  Operating Range:  $V_L$  to 5.5 V  
Wide  $V_L$  Operating Range: 1.65 V to 5.5 V
- High-Speed with 24 Mb/s Guaranteed Data Rate
- Low Bit-to-Bit Skew
- Enable Input and I/O Pins are  
Overvoltage Tolerant (OVT) to 5.5 V
- Non-preferential Power-up Sequencing
- Integrated 10 k $\Omega$  Pull-up Resistors
- Small Space Saving Package  
– 1.9 mm x 0.9 mm x 0.5 mm Flipchip8
- This is a Pb-Free Device

### Typical Applications

- I<sup>2</sup>C, SMBus
- Low Voltage ASIC Level Translation
- Mobile Phones, PDAs, Cameras

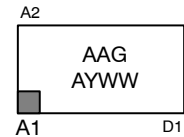
### Important Information

- ESD Protection for All Pins  
– Human Body Model (HBM) > 7000 V

### MARKING DIAGRAM

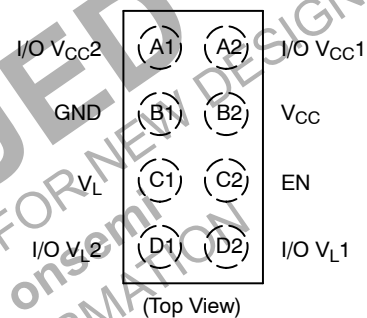


FLIP-CHIP 8  
CASE 499BF

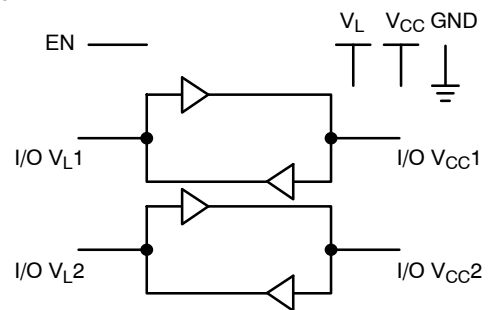


AAG = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week

### PIN ASSIGNMENTS



### LOGIC DIAGRAM



### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

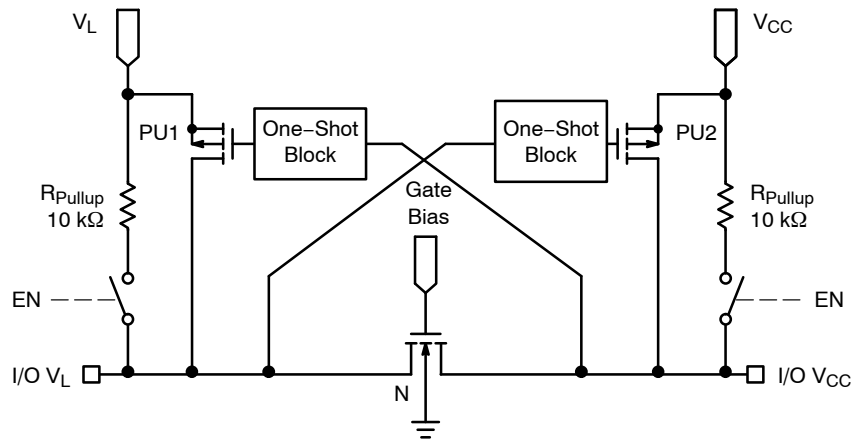


Figure 1. Block Diagram (1 I/O Line)

## PIN ASSIGNMENT

Pins	Description
$V_{CC}$	$V_{CC}$ Supply Voltage
$V_L$	$V_L$ Supply Voltage
GND	Ground
EN	Output Enable, referenced to $V_L$
I/O $V_{CCn}$	I/O Port, referenced to $V_{CC}$
I/O $V_{Ln}$	I/O Port, referenced to $V_L$

## FUNCTION TABLE

EN	Operating Mode
L	Hi-Z
H	I/O Buses Connected

## MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
$V_{CC}$	High-side DC Supply Voltage	-0.5 to +7.0		V
$V_L$	Low-side DC Supply Voltage	-0.5 to +7.0		V
I/O $V_{CC}$	$V_{CC}$ -referenced DC Input / Output Voltage	-0.5 to +7.0		V
I/O $V_L$	$V_L$ -referenced DC Input / Output Voltage	-0.5 to +7.0		V
$V_{EN}$	Enable Control Pin DC Input Voltage	-0.5 to +7.0		V
$I_{I/O\_SC}$	Short-Circuit Duration (I/O $V_L$ and I/O $V_{CC}$ to GND)	±50	Continuous	mA
$I_{I/O\_K}$	Input / Output Clamping Current (I/O $V_L$ and I/O $V_{CC}$ )	-50	$V_{I/O} < 0$	mA
$T_{STG}$	Storage Temperature	-65 to +150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	High-side Positive DC Supply Voltage	$V_L$	5.5	V
$V_L$	Low-side Positive DC Supply Voltage	1.65	5.5	V
$V_{EN}$	Enable Control Pin Voltage	GND	5.5	V
$V_{IO}$	I/O Pin Voltage	GND	5.5	V
$\Delta t/\Delta V$	Input Transition Rise and Fall Rate I/O $V_L$ and I/O $V_{CC}$ Ports, Push-Pull Driving		10	ns/V
	Control Input		10	
$T_A$	Operating Temperature Range	-40	+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# NLSX0102

## DC ELECTRICAL CHARACTERISTICS ( $T_A = -40$ to $+85$ °C, unless otherwise specified)

Symbol	Parameter	Test Conditions (Note 1)	$V_L$	$V_{CC}$	-40 °C to +85 °C			Unit
					Min	Typ (Notes 1, 2)	Max	
$V_{IHC}$	I/O $V_{CC}$ Input HIGH Voltage		1.65 to 5.5	$V_L$ to 5.5	$V_{CC} - 0.4$		–	V
$V_{ILC}$	I/O $V_{CC}$ Input LOW Voltage		1.65 to 5.5	$V_L$ to 5.5			0.15	V
$V_{IHL}$	I/O $V_L$ Input HIGH Voltage		1.65 to 5.5	$V_L$ to 5.5	$V_L - 0.4$		–	V
$V_{ILL}$	I/O $V_L$ Input LOW Voltage		1.65 to 5.5	$V_L$ to 5.5			0.15	V
$V_{IH}$	Control Pin Input HIGH Voltage		1.65 to 5.5	$V_L$ to 5.5	$0.75 * V_L$		–	V
$V_{IL}$	Control Pin Input LOW Voltage		1.65 to 5.5	$V_L$ to 5.5			$0.25 * V_L$	V
$V_{OHC}$	I/O $V_{CC}$ Output HIGH Voltage	I/O $V_{CC}$ source current = $-20 \mu A$	1.65 to 5.5	$V_L$ to 5.5	$2/3 * V_{CC}$		–	V
$V_{OLC}$	I/O $V_{CC}$ Output LOW Voltage	I/O $V_{CC}$ sink current = 1 mA	1.65 to 5.5	$V_L$ to 5.5			0.4	V
$V_{OHL}$	I/O $V_L$ Output HIGH Voltage	I/O $V_L$ source current = $-20 \mu A$	1.65 to 5.5	$V_L$ to 5.5	$2/3 * V_L$		–	V
$V_{OLL}$	I/O $V_L$ Output LOW Voltage	I/O $V_L$ sink current = 1 mA	1.65 to 5.5	$V_L$ to 5.5			0.4	V
$I_{QVL}$	$V_L$ Supply Current Supply Current	I/O $V_{CC}$ and I/O $V_L$ unconnected, $V_{EN} = V_L$	1.65 to 5.5	$V_L$ to 5.5			2.4	$\mu A$
			5.5	0			2.4	
$I_{QVCC}$	$V_L$ Supply Current Supply Current	I/O $V_{CC}$ and I/O $V_L$ unconnected, $V_{EN} = V_L$	1.65 to 5.5	$V_L$ to 5.5			2.4	$\mu A$
			0	5.5			2.4	
$I_{TS-VCC}$	$V_{CC}$ Tri-state Output Mode	I/O $V_{CC}$ and I/O $V_L$ unconnected, $V_{EN} = GND$	1.65 to 5.5	$V_L$ to 5.5			1.0	$\mu A$
$I_{TS-VL}$	$V_L$ Tri-state Output Mode Supply Current	I/O $V_{CC}$ and I/O $V_L$ unconnected, $V_{EN} = GND$	1.65 to 5.5	$V_L$ to 5.5			1.0	$\mu A$
$I_I$	Enable Pin Input Leakage Current		1.65 to 5.5	$V_L$ to 5.5			1.0	$\mu A$
$I_{OZ}$	I/O Tri-state Output Mode Leakage Current		1.65 to 5.5	$V_L$ to 5.5			1.0	$\mu A$
$R_{PU}$	Pull-Up Resistors I/O $V_L$ and $V_C$					10		k $\Omega$

1. Typical values are for  $V_{CC} = +3.3$  V,  $V_L = +1.8$  V and  $T_A = +25$  °C.

2. All units are production tested at  $T_A = +25$  °C. Limits over the operating temperature range are guaranteed by design.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**Timing Characteristics – Rail-to-Rail Driving Configuration**

(I/O test circuits of Figures 2, 3 and 7,  $C_{LOAD} = 15 \text{ pF}$ , driver output impedance  $\leq 50 \Omega$ ,  $R_{LOAD} = 1 \text{ M}\Omega$ , unless otherwise specified)

Symbol	Parameter	Conditions	-40°C to +85°C						Unit
			V <sub>CC</sub> = 2.3 to 2.7 V		V <sub>CC</sub> = 3.0 to 3.6 V		V <sub>CC</sub> = 4.5 to 5.5 V		
			Min	Max	Min	Max	Min	Max	

**$V_L = 1.65 \text{ to } 1.95 \text{ V}$**

$t_{RVL}$	I/O $V_L$ Rise Time	Figure 8	0.6	17.0	2.3	14.0	0.8	12.9	nS
$t_{RVCC}$	I/O $V_{CC}$ Rise Time	Figure 8	4.0	10.8	2.2	9.1	2.7	7.6	nS
$t_{FVL}$	I/O $V_L$ Fall Time	Figure 8	2.0	9.7	1.9	8.1	1.7	13.3	nS
$t_{FVCC}$	I/O $V_{CC}$ Fall Time	Figure 8	2.9	13.8	2.8	16.2	2.8	16.2	nS
$t_{PHL-VL-VCC}$	Propagation Delay (Driving I/O $V_L$ , $V_L$ to $V_{CC}$ )	Figure 2		7.2		7.1		10.0	nS
$t_{PLH-VL-VCC}$				6.5		7.1		7.4	
$t_{PHL-VCC-VL}$	Propagation Delay (Driving I/O $V_{CC}$ , $V_{CC}$ to $V_L$ )	Figure 3		6.0		5.3		6.7	nS
$t_{PLH-VCC-VL}$				8.0		7.6		7.1	
$t_{EN}$	Enable Time	Figure 7		50		40		35	nS
$t_{DIS}$	Disable Time	Figure 7		390		365		710	nS
$t_{PPSKEW}$	Part-to-Part Skew			0.7		0.7		0.7	nS
MDR	Maximum Data Rate		21		22		24		Mbps

**$V_L = 2.3 \text{ to } 2.7 \text{ V}$**

$t_{RVL}$	I/O $V_L$ Rise Time	Figure 8	2.8	8.6	2.6	8.1	1.8	10.3	nS
$t_{RVCC}$	I/O $V_{CC}$ Rise Time	Figure 8	3.2	9.2	2.9	8.8	1.9	7.7	nS
$t_{FVL}$	I/O $V_L$ Fall Time	Figure 8	1.9	8.3	1.9	7.8	1.8	7.4	nS
$t_{FVCC}$	I/O $V_{CC}$ Fall Time	Figure 8	2.2	8.3	2.4	8.0	2.6	10.0	nS
$t_{PHL-VL-VCC}$	Propagation Delay (Driving I/O $V_L$ , $V_L$ to $V_{CC}$ )	Figure 2		4.8		5.2		6.5	nS
$t_{PLH-VL-VCC}$				5.4		5.3		6.0	
$t_{PHL-VCC-VL}$	Propagation Delay (Driving I/O $V_{CC}$ , $V_{CC}$ to $V_L$ )	Figure 3		5.0		3.9		5.4	nS
$t_{PLH-VCC-VL}$				5.5		5.0		5.5	
$t_{EN}$	Enable Time	Figure 7		100		40		35	nS
$t_{DIS}$	Disable Time	Figure 7		320		305		430	nS
$t_{PPSKEW}$	Part-to-Part Skew			0.7		0.7		0.7	nS
MDR	Maximum Data Rate		20		22		24		Mbps

**Timing Characteristics – Rail-to-Rail Driving Configuration**(I/O test circuits of Figures 2, 3 and 7,  $C_{LOAD} = 15\text{ pF}$ , driver output impedance  $\leq 50\ \Omega$ ,  $R_{LOAD} = 1\text{ M}\Omega$ , unless otherwise specified)

Symbol	Parameter	Conditions	-40°C to +85°C						Unit
			V <sub>CC</sub> = 2.3 to 2.7 V		V <sub>CC</sub> = 3.0 to 3.6 V		V <sub>CC</sub> = 4.5 to 5.5 V		
			Min	Max	Min	Max	Min	Max	
V <sub>L</sub> = 3.0 to 3.6 V									
t <sub>RVL</sub>	I/O V <sub>L</sub> Rise Time	Figure 8			2.3	6.5	1.9	8.0	nS
t <sub>RVCC</sub>	I/O V <sub>CC</sub> Rise Time	Figure 8			2.5	6.5	2.1	7.4	nS
t <sub>FVL</sub>	I/O V <sub>L</sub> Fall Time	Figure 8			1.3	7.2	1.6	11.0	nS
t <sub>FVCC</sub>	I/O V <sub>CC</sub> Fall Time	Figure 8			1.7	8.0	1.3	9.3	nS
t <sub>PHL-VL-VCC</sub>	Propagation Delay (Driving I/O V <sub>L</sub> , V <sub>L</sub> to V <sub>CC</sub> )	Figure 2				3.9		4.6	nS
t <sub>PLH-VL-VCC</sub>						3.8		3.8	
t <sub>PHL-VCC-VL</sub>	Propagation Delay (Driving I/O V <sub>CC</sub> , V <sub>CC</sub> to V <sub>L</sub> )	Figure 3				3.8		4.6	nS
t <sub>PLH-VCC-VL</sub>						4.3		5.8	
t <sub>EN</sub>	Enable Time	Figure 7				80		35	nS
t <sub>DIS</sub>	Disable Time	Figure 7				260		385	nS
t <sub>PPSKEW</sub>	Part-to-Part Skew					0.7		0.7	nS
MDR	Maximum Data Rate				23		24		Mbps

**Timing Characteristics – Open Drain Driving Configuration**(I/O test circuits of Figures 4, 5 and 7,  $C_{LOAD} = 15\text{ pF}$ , driver output impedance  $\leq 50\ \Omega$ ,  $R_{LOAD} = 1\text{ M}\Omega$ , unless otherwise specified)

Symbol	Parameter	Conditions	-40°C to +85°C						Unit
			V <sub>CC</sub> = 2.3 to 2.7 V		V <sub>CC</sub> = 3.0 to 3.6 V		V <sub>CC</sub> = 4.5 to 5.5 V		
			Min	Max	Min	Max	Min	Max	
V <sub>L</sub> = 1.65 to 1.95 V									
t <sub>RVL</sub>	I/O V <sub>L</sub> Rise Time	Figure 8	38	340	30	245	22.0	134	nS
t <sub>RVCC</sub>	I/O V <sub>CC</sub> Rise Time	Figure 8	34	330	23	218	10.0	120	nS
t <sub>FVL</sub>	I/O V <sub>L</sub> Fall Time	Figure 8	4.4	11.1	4.3	12.0	4.2	14.2	nS
t <sub>FVCC</sub>	I/O V <sub>CC</sub> Fall Time	Figure 8	6.9	11	7.5	16.2	7.0	16.2	nS
t <sub>PHLVL-VCC</sub>	Propagation Delay (Driving I/O V <sub>L</sub> , V <sub>L</sub> to V <sub>CC</sub> )	Figure 2	2.3	27	2.4	20.0	2.6	23.0	nS
t <sub>PLHVL-VCC</sub>			45	260	36.0	208	27.0	208	
t <sub>PHLVCC-VL</sub>	Propagation Delay (Driving I/O V <sub>CC</sub> , V <sub>CC</sub> to V <sub>L</sub> )	Figure 3	1.9	22	1.1	22.0	1.2	22.0	nS
t <sub>PLHVCC-VL</sub>			45.0	200	36	150	27.0	112	
t <sub>EN</sub>	Enable Time	Figure 7		80		70		35	nS
t <sub>DIS</sub>	Disable Time	Figure 7		250		277		290	nS
t <sub>PPSKEW</sub>	Part-to-Part Skew			0.7		0.7		0.7	nS
MDR	Maximum Data Rate		2		2		2		Mbps

**Timing Characteristics – Open Drain Driving Configuration**

(I/O test circuits of Figures 4, 5 and 7,  $C_{LOAD} = 15 \text{ pF}$ , driver output impedance  $\leq 50 \Omega$ ,  $R_{LOAD} = 1 \text{ M}\Omega$ , unless otherwise specified)

Symbol	Parameter	Conditions	–40°C to +85°C						Unit
			V <sub>CC</sub> = 2.3 to 2.7 V		V <sub>CC</sub> = 3.0 to 3.6 V		V <sub>CC</sub> = 4.5 to 5.5 V		
			Min	Max	Min	Max	Min	Max	

**$V_L = 2.3 \text{ to } 2.7 \text{ V}$**

$t_{RVL}$	I/O $V_L$ Rise Time	Figure 8	34	400	28.0	300	24.0	208	nS
$t_{RVCC}$	I/O $V_{CC}$ Rise Time	Figure 8	35.0	352	24.0	280	12.0	180	nS
$t_{FVL}$	I/O $V_L$ Fall Time	Figure 8	4.4	6.9	4.3	6.2	4.2	7.8	nS
$t_{FVCC}$	I/O $V_{CC}$ Fall Time	Figure 8	4.3	8.8	4.9	9.4	5.4	10.4	nS
$t_{PHVL-VCC}$	Propagation Delay (Driving I/O $V_L$ , $V_L$ to $V_{CC}$ )	Figure 2	1.7	14.0	2.0	14.0	2.1	14.0	nS
$t_{PLHV-VCC}$			43.0	250	36.0	210	27.0	210	
$t_{PHLVCC-VL}$	Propagation Delay (Driving I/O $V_{CC}$ , $V_{CC}$ to $V_L$ )	Figure 3	1.8	13.0	2.6	13.0	1.2	13.0	nS
$t_{PLHVCC-VL}$			44.0	225	37.0	180	27.0	144	
$t_{EN}$	Enable Time	Figure 7		50		40		35	nS
$t_{DIS}$	Disable Time	Figure 7		265		230		215	nS
$t_{PPSKEW}$	Part-to-Part Skew			0.7		0.7		0.7	nS
MDR	Maximum Data Rate		2		2		2		Mbps

**$V_L = 3.0 \text{ to } 3.6 \text{ V}$**

$t_{RVL}$	I/O $V_L$ Rise Time	Figure 8			25.0	400	19.0	278	nS
$t_{RVCC}$	I/O $V_{CC}$ Rise Time	Figure 8			26.0	375	14.0	247	nS
$t_{FVL}$	I/O $V_L$ Fall Time	Figure 8			2.8	6.1	2.6	5.7	nS
$t_{FVCC}$	I/O $V_{CC}$ Fall Time	Figure 8			2.6	7.6	3.1	8.3	nS
$t_{PHVL-VCC}$	Propagation Delay (Driving I/O $V_L$ , $V_L$ to $V_{CC}$ )	Figure 2			1.3	10.0	1.4	8.0	nS
$t_{PLHV-VCC}$					36.0	255	28.0	243	
$t_{PHLVCC-VL}$	Propagation Delay (Driving I/O $V_{CC}$ , $V_{CC}$ to $V_L$ )	Figure 3			1.0	124	1.0	97.0	nS
$t_{PLHVCC-VL}$					3.0	185	3.0	136	
$t_{EN}$	Enable Time	Figure 7				40		35	nS
$t_{DIS}$	Disable Time	Figure 7				250		205	nS
$t_{PPSKEW}$	Part-to-Part Skew					0.7		0.7	nS
MDR	Maximum Data Rate				2		2		Mbps

TEST SETUPS

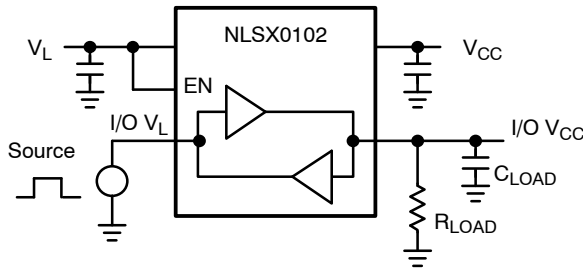


Figure 2. Rail-to-Rail Driving I/O  $V_L$

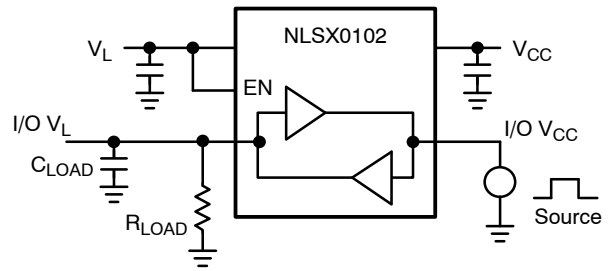


Figure 3. Rail-to-Rail Driving I/O  $V_{CC}$

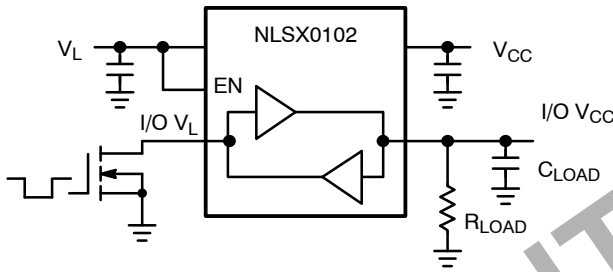


Figure 4. Open-Drain Driving I/O  $V_L$

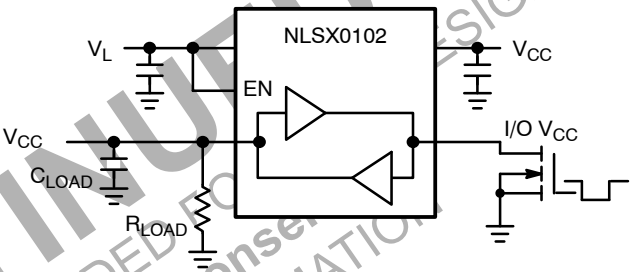


Figure 5. Open-Drain Driving I/O  $V_{CC}$

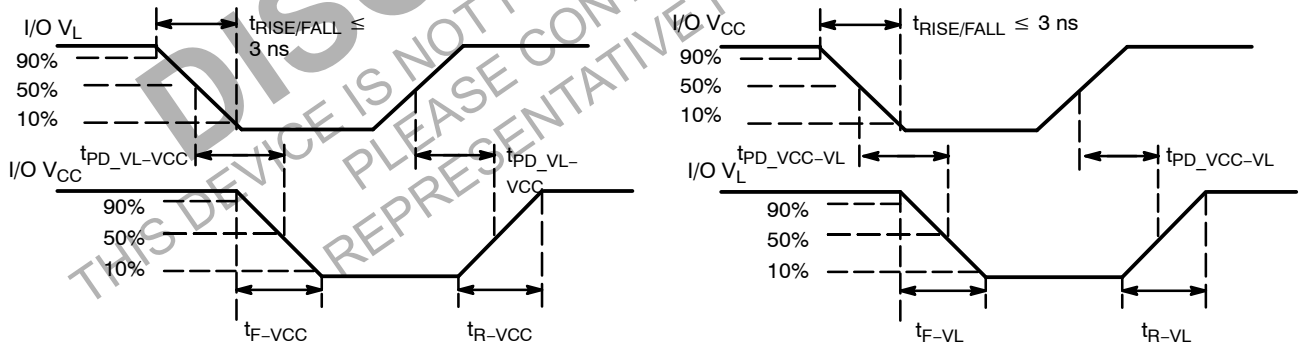
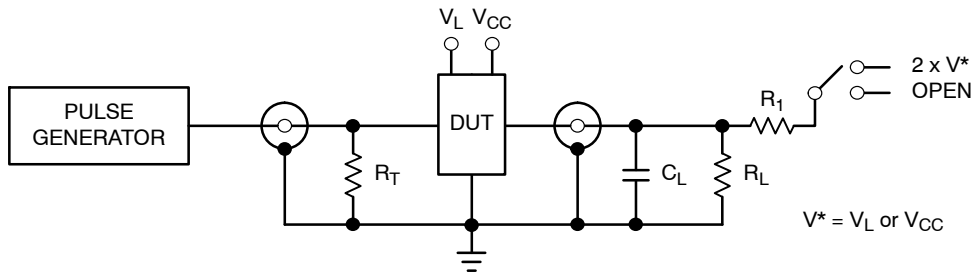


Figure 6. Definition of Timing Specification Parameters



Test	Switch
$t_{PZH}, t_{PHZ}$	Open
$t_{PZL}, t_{PLZ}$	$2 \times V^*$

$C_L = 15 \text{ pF}$  or equivalent (Includes jig and probe capacitance)  
 $R_L = R_1 = 50 \text{ k}\Omega$  or equivalent  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50 \Omega$ )  
 $V^* = V_L$  or  $V_{CC}$  for I/O\_VL or I/O\_VCC measurements, respectively.

Figure 7. Test Circuit for Enable/Disable Time Measurement

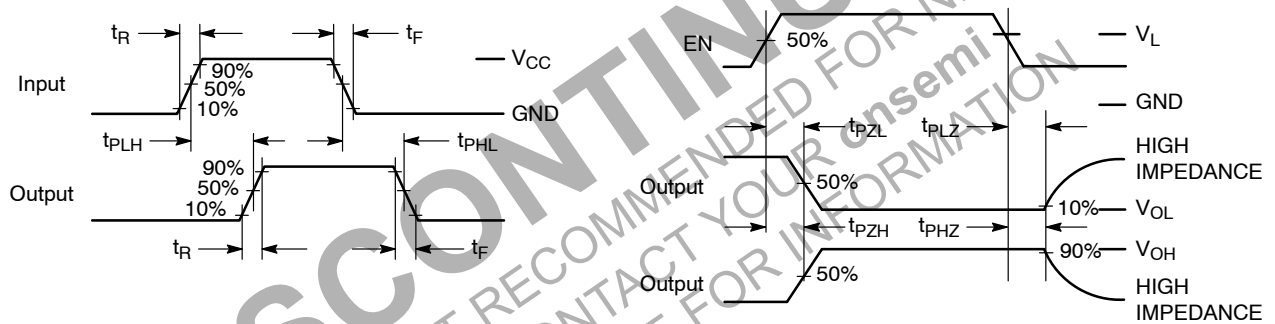


Figure 8. Timing Definitions for Propagation Delays and Enable/Disable Measurement



## APPLICATIONS INFORMATION

**Level Translator Architecture**

The NLSX0102 auto sense translator provides bi-directional voltage level shifting to transfer data in multiple supply voltage systems. This device has two supply voltages,  $V_L$  and  $V_{CC}$ , which set the logic levels on the input and output sides of the translator. When used to transfer data from the  $V_L$  to the  $V_{CC}$  ports, input signals referenced to the  $V_L$  supply are translated to output signals with a logic level matched to  $V_{CC}$ . In a similar manner, the  $V_{CC}$  to  $V_L$  translation shifts input signals with a logic level compatible to  $V_{CC}$  to an output signal matched to  $V_L$ .

The NLSX0102 consists of two bi-directional channels that independently determine the direction of the data flow without requiring a directional pin. The one-shot circuits are used to detect the rising or falling input signals. In addition, the one shots decrease the rise and fall time of the output signal for high-to-low and low-to-high transitions. Each input/output channel has an internal 10 k $\Omega$  pull-up. The magnitude of the pull-up resistors can be reduced by connecting external resistors in parallel to the internal 10 k $\Omega$  resistors.

**Input Driver Requirements**

The rise ( $t_R$ ) and fall ( $t_F$ ) timing parameters of the open drain outputs depend on the magnitude of the pull-up resistors. In addition, the propagation times ( $t_{PD}$ ), skew ( $t_{PSKEW}$ ) and maximum data rate depend on the impedance

of the device that is connected to the translator. The timing parameters listed in the data sheet assume that the output impedance of the drivers connected to the translator is less than 50 k $\Omega$ .

**Enable Input (EN)**

The NLSX0102 has an Enable pin (EN) that provides tri-state operation at the I/O pins. Driving the Enable pin to a low logic level minimizes the power consumption of the device and drives the I/O  $V_{CC}$  and I/O  $V_L$  pins to a high impedance state. Normal translation operation occurs when the EN pin is equal to a logic high signal. The EN pin is referenced to the  $V_L$  supply and has Overvoltage Tolerant (OVT) protection.

**Power Supply Guidelines**

During normal operation, supply voltage  $V_L$  must be less than or equal to  $V_{CC}$ . The sequencing of the power supplies will not damage the device during the power up operation. For optimal performance, 0.01  $\mu$ F to 0.1  $\mu$ F decoupling capacitors should be used on the  $V_L$  and  $V_{CC}$  power supply pins. Ceramic capacitors are a good design choice to filter and bypass any noise signals on the voltage lines to the ground plane of the PCB. The noise immunity will be maximized by placing the capacitors as close as possible to the supply and ground pins, along with minimizing the PCB connection traces.

**ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
NLSX0102FCT1G	Flip-Chip 8 (Pb-Free)	3000 / Tape & Reel
NLSX0102FCT2G	Flip-Chip 8 (Pb-Free)	3000 / Tape & Reel (4mm Pitch Carrier Tape)
NLSX0102FC2T2G	Flip-Chip 8 (Pb-Free)	3000 / Tape & Reel (2mm Pitch Carrier Tape)

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

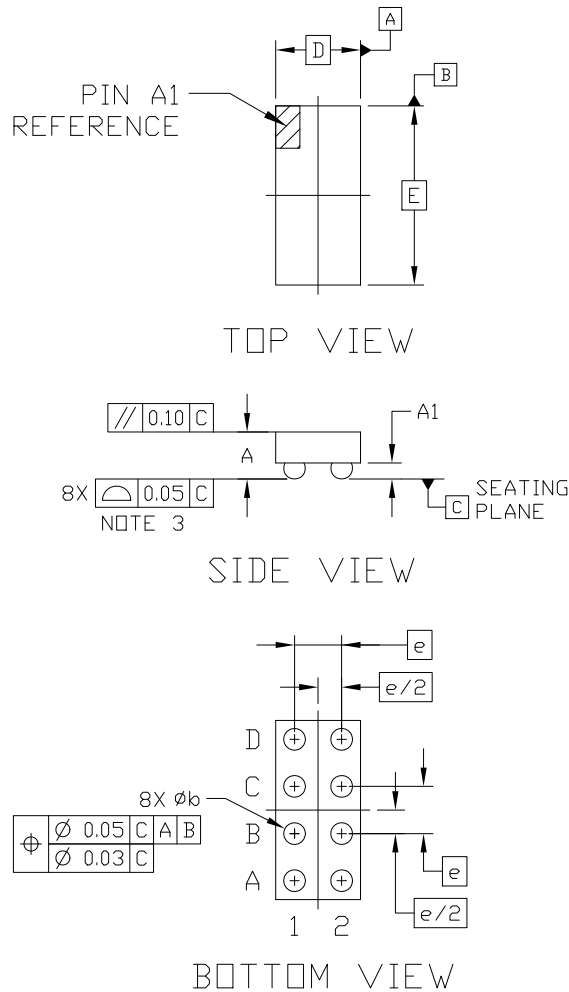


A1

SCALE 4:1

**8 PIN FLIP-CHIP, 0.9x1.9, 0.5P**  
**CASE 499BF**  
**ISSUE A**

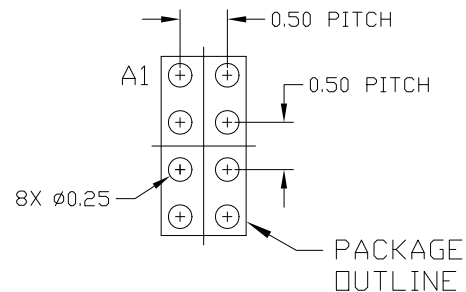
DATE 12 JAN 2022



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.

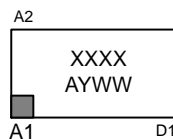
DIM	MILLIMETERS	
	MIN	MAX
A	0.44	0.50
A1	0.18	0.22
b	0.24	0.28
D	0.90 BSC	
E	1.90 BSC	
e	0.50 BSC	



**SOLDERING FOOTPRINT\***

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi soldering and mounting techniques reference manual, SOLDERRM/D.

**GENERIC MARKING DIAGRAM\***



XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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<b>DESCRIPTION:</b>	<b>8 PIN FLIP-CHIP, 0.9X1.9, 0.5P</b>	<b>PAGE 1 OF 1</b>

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