

# NLSV2T244

## 2-Bit Dual-Supply Non-Inverting Level Translator

The NLSV2T244 is a 2-bit configurable dual-supply voltage level translator. The input  $A_n$  and output  $B_n$  ports are designed to track two different power supply rails,  $V_{CCA}$  and  $V_{CCB}$  respectively. Both supply rails are configurable from 0.9 V to 4.5 V allowing universal low-voltage translation from the input  $A_n$  to the output  $B_n$  port.

### Features

- Wide  $V_{CCA}$  and  $V_{CCB}$  Operating Range: 0.9 V to 4.5 V
- High-Speed w/ Balanced Propagation Delay
- Inputs and Outputs have OVT Protection to 4.5 V
- Non-preferential  $V_{CCA}$  and  $V_{CCB}$  Sequencing
- Outputs at 3-State until Active  $V_{CC}$  is Reached
- Power-Off Protection
- Outputs Switch to 3-State with  $V_{CCB}$  at GND
- Small Packaging: UDFN8, SO-8, Micro8
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- Mobile Phones, PDAs, Other Portable Devices

### Important Information

- ESD Protection for All Pins:  
HBM (Human Body Model) > 5000 V



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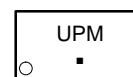
[www.onsemi.com](http://www.onsemi.com)

### MARKING DIAGRAMS



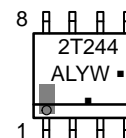
**UDFN8**  
**MU SUFFIX**  
**CASE 517AJ**

UP = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package



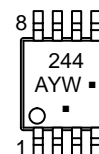
**SO-8**  
**D SUFFIX**  
**CASE 751**

A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package



**Micro8**  
**DM SUFFIX**  
**CASE 846A**

A = Assembly Location  
Y = Year  
W = Work Week  
▪ = Pb-Free Package



### ORDERING INFORMATION

| Device         | Package             | Shipping†          |
|----------------|---------------------|--------------------|
| NLSV2T244MUTAG | UDFN8<br>(Pb-Free)  | 3000 / Tape & Reel |
| NLSV2T244DR2G  | SO-8<br>(Pb-Free)   | 2500 / Tape & Reel |
| NLSV2T244DMR2G | Micro8<br>(Pb-Free) | 4000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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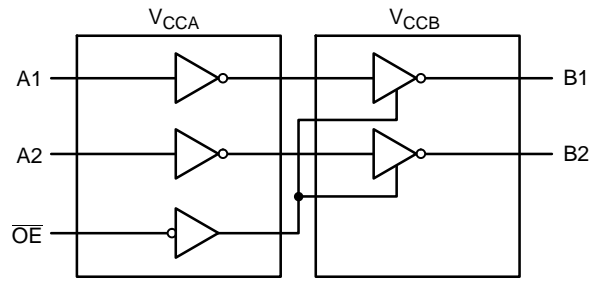
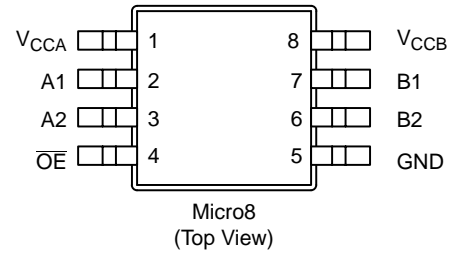
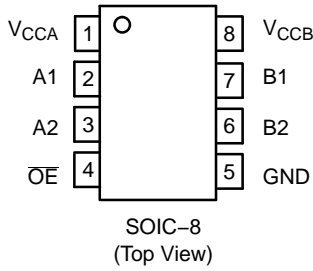
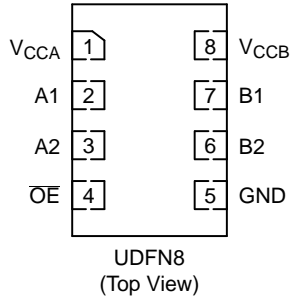


Figure 1. Logic Diagram

## PIN ASSIGNMENTS



## PIN ASSIGNMENT

| PIN                    | FUNCTION                    |
|------------------------|-----------------------------|
| V <sub>CCA</sub>       | Input Port DC Power Supply  |
| V <sub>CCB</sub>       | Output Port DC Power Supply |
| GND                    | Ground                      |
| A <sub>n</sub>         | Input Port                  |
| B <sub>n</sub>         | Output Port                 |
| $\overline{\text{OE}}$ | Output Enable               |

## TRUTH TABLE

| Inputs                 |                | Outputs        |
|------------------------|----------------|----------------|
| $\overline{\text{OE}}$ | A <sub>n</sub> | B <sub>n</sub> |
| L                      | L              | L              |
| L                      | H              | H              |
| H                      | X              | 3-State        |

# NLSV2T244

## MAXIMUM RATINGS

| Symbol             | Rating                               | Value        | Condition               | Unit               |
|--------------------|--------------------------------------|--------------|-------------------------|--------------------|
| $V_{CCA}, V_{CCB}$ | DC Supply Voltage                    | -0.5 to +5.5 |                         | V                  |
| $V_I$              | DC Input Voltage $A_n$               | -0.5 to +5.5 |                         | V                  |
| $V_C$              | Control Input $\overline{OE}$        | -0.5 to +5.5 |                         | V                  |
| $V_O$              | DC Output Voltage (Power Down) $B_n$ | -0.5 to +5.5 | $V_{CCA} = V_{CCB} = 0$ | V                  |
|                    | (Active Mode) $B_n$                  | -0.5 to +5.5 |                         | V                  |
|                    | (Tri-State Mode) $B_n$               | -0.5 to +5.5 |                         | V                  |
| $I_{IK}$           | DC Input Diode Current               | -20          | $V_I < \text{GND}$      | mA                 |
| $I_{OK}$           | DC Output Diode Current              | -50          | $V_O < \text{GND}$      | mA                 |
| $I_O$              | DC Output Source/Sink Current        | $\pm 50$     |                         | mA                 |
| $I_{CCA}, I_{CCB}$ | DC Supply Current Per Supply Pin     | $\pm 100$    |                         | mA                 |
| $I_{GND}$          | DC Ground Current per Ground Pin     | $\pm 100$    |                         | mA                 |
| $T_{STG}$          | Storage Temperature                  | -65 to +150  |                         | $^{\circ}\text{C}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## RECOMMENDED OPERATING CONDITIONS

| Symbol                | Parameter   | Min | Max       | Unit               |
|-----------------------|---|-----|-----------|--------------------|
| $V_{CCA}, V_{CCB}$    | Positive DC Supply Voltage  | 0.9 | 4.5       | V                  |
| $V_I$                 | Bus Input Voltage   | GND | 4.5       | V                  |
| $V_C$                 | Control Input $\overline{OE}$   | GND | 4.5       | V                  |
| $V_{IO}$              | Bus Output Voltage (Power Down Mode) $B_n$  | GND | 4.5       | V                  |
|                       | (Active Mode) $B_n$   | GND | $V_{CCB}$ | V                  |
|                       | (Tri-State Mode) $B_n$  | GND | 4.5       | V                  |
| $T_A$                 | Operating Temperature Range   | -40 | +85       | $^{\circ}\text{C}$ |
| $\Delta t / \Delta V$ | Input Transition Rise or Rate<br>$V_I$ , from 30% to 70% of $V_{CC}$ ; $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ | 0   | 10        | nS                 |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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## DC ELECTRICAL CHARACTERISTICS

| Symbol                              | Parameter   | Test Conditions  | V <sub>CCA</sub> (V) | V <sub>CCB</sub> (V) | -40°C to +85°C          |                         | Unit |
|-------------------------------------|---|--|----------------------|----------------------|-------------------------|-------------------------|------|
|                                     |   |  |                      |                      | Min                     | Max                     |      |
| V <sub>IH</sub>                     | Input HIGH Voltage<br>(An, OE)  |  | 3.6 – 4.5            | 0.9 – 4.5            | 2.2                     | –                       | V    |
|                                     |   |  | 2.7 – 3.6            |                      | 2.0                     | –                       |      |
|                                     |   |  | 2.3 – 2.7            |                      | 1.6                     | –                       |      |
|                                     |   |  | 1.4 – 2.3            |                      | 0.65 * V <sub>CCA</sub> | –                       |      |
|                                     |   |  | 0.9 – 1.4            |                      | 0.9 * V <sub>CCA</sub>  | –                       |      |
| V <sub>IL</sub>                     | Input LOW Voltage<br>(An, OE)   |  | 3.6 – 4.5            | 0.9 – 4.5            | –                       | 0.8                     | V    |
|                                     |   |  | 2.7 – 3.6            |                      | –                       | 0.8                     |      |
|                                     |   |  | 2.3 – 2.7            |                      | –                       | 0.7                     |      |
|                                     |   |  | 1.4 – 2.3            |                      | –                       | 0.35 * V <sub>CCA</sub> |      |
|                                     |   |  | 0.9 – 1.4            |                      | –                       | 0.1 * V <sub>CCA</sub>  |      |
| V <sub>OH</sub>                     | Output HIGH Voltage   | I <sub>OH</sub> = –100 μA; V <sub>I</sub> = V <sub>IH</sub>  | 0.9 – 4.5            | 0.9 – 4.5            | V <sub>CCB</sub> – 0.2  | –                       | V    |
|                                     |   | I <sub>OH</sub> = –0.5 mA; V <sub>I</sub> = V <sub>IH</sub>  | 0.9                  | 0.9                  | 0.75 * V <sub>CCB</sub> | –                       |      |
|                                     |   | I <sub>OH</sub> = –2 mA; V <sub>I</sub> = V <sub>IH</sub>  | 1.4                  | 1.4                  | 1.05                    | –                       |      |
|                                     |   | I <sub>OH</sub> = –6 mA; V <sub>I</sub> = V <sub>IH</sub>  | 1.65                 | 1.65                 | 1.25                    | –                       |      |
|                                     |   |  | 2.3                  | 2.3                  | 2.0                     | –                       |      |
|                                     |   | I <sub>OH</sub> = –12 mA; V <sub>I</sub> = V <sub>IH</sub>   | 2.3                  | 2.3                  | 1.8                     | –                       |      |
|                                     |   |  | 2.7                  | 2.7                  | 2.2                     | –                       |      |
|                                     |   | I <sub>OH</sub> = –18 mA; V <sub>I</sub> = V <sub>IH</sub>   | 2.3                  | 2.3                  | 1.7                     | –                       |      |
| 3.0                                 | 3.0   |  | 2.4                  | –                    |                         |                         |      |
| V <sub>OL</sub>                     | Output LOW Voltage  | I <sub>OL</sub> = 100 μA; V <sub>I</sub> = V <sub>IL</sub>   | 0.9 – 4.5            | 0.9 – 4.5            | –                       | 0.2                     | V    |
|                                     |   | I <sub>OL</sub> = 0.5 mA; V <sub>I</sub> = V <sub>IL</sub>   | 1.1                  | 1.1                  | –                       | 0.3                     |      |
|                                     |   | I <sub>OL</sub> = 2 mA; V <sub>I</sub> = V <sub>IL</sub>   | 1.4                  | 1.4                  | –                       | 0.35                    |      |
|                                     |   | I <sub>OL</sub> = 6 mA; V <sub>I</sub> = V <sub>IL</sub>   | 1.65                 | 1.65                 | –                       | 0.3                     |      |
|                                     |   |  | 2.3                  | 2.3                  | –                       | 0.4                     |      |
|                                     |   | I <sub>OL</sub> = 12 mA; V <sub>I</sub> = V <sub>IL</sub>  | 2.7                  | 2.7                  | –                       | 0.4                     |      |
|                                     |   |  | 2.3                  | 2.3                  | –                       | 0.6                     |      |
|                                     |   | I <sub>OL</sub> = 18 mA; V <sub>I</sub> = V <sub>IL</sub>  | 3.0                  | 3.0                  | –                       | 0.4                     |      |
| 3.0                                 | 3.0   |  | –                    | 0.55                 |                         |                         |      |
| I <sub>I</sub>                      | Input Leakage Current   | V <sub>I</sub> = V <sub>CCA</sub> or GND   | 0.9 – 4.5            | 0.9 – 4.5            | –1.0                    | 1.0                     | μA   |
| I <sub>OFF</sub>                    | Power–Off Leakage Current   | OE = 0 V   | 0<br>0.9 – 4.5       | 0.9 – 4.5<br>0       | –1.0<br>–1.0            | 1.0<br>1.0              | μA   |
| I <sub>CCA</sub>                    | Quiescent Supply Current  | V <sub>I</sub> = V <sub>CCA</sub> or GND;<br>I <sub>O</sub> = 0, V <sub>CCA</sub> = V <sub>CCB</sub> | 0.9 – 4.5            | 0.9 – 4.5            | –                       | 1.0                     | μA   |
| I <sub>CCB</sub>                    | Quiescent Supply Current  | V <sub>I</sub> = V <sub>CCA</sub> or GND;<br>I <sub>O</sub> = 0, V <sub>CCA</sub> = V <sub>CCB</sub> | 0.9 – 4.5            | 0.9 – 4.5            | –                       | 1.0                     | μA   |
| I <sub>CCA</sub> + I <sub>CCB</sub> | Quiescent Supply Current  | V <sub>I</sub> = V <sub>CCA</sub> or GND;<br>I <sub>O</sub> = 0, V <sub>CCA</sub> = V <sub>CCB</sub> | 0.9 – 4.5            | 0.9 – 4.5            | –                       | 2.0                     | μA   |
| ΔI <sub>CCA</sub>                   | Increase in I <sub>CC</sub> per Input Voltage,<br>Other Inputs at V <sub>CCA</sub> or GND | V <sub>I</sub> = V <sub>CCA</sub> – 0.6 V;<br>V <sub>I</sub> = V <sub>CCA</sub> or GND               | 4.5                  | 4.5                  | –                       | 10                      | μA   |
|                                     |   |  | 3.6                  | 3.6                  | –                       | 5.0                     |      |
| ΔI <sub>CCB</sub>                   | Increase in I <sub>CC</sub> per Input Voltage,<br>Other Inputs at V <sub>CCA</sub> or GND | V <sub>I</sub> = V <sub>CCA</sub> – 0.6 V;<br>V <sub>I</sub> = V <sub>CCA</sub> or GND               | 4.5                  | 4.5                  | –                       | 10                      | μA   |
|                                     |   |  | 3.6                  | 3.6                  | –                       | 5.0                     |      |
| I <sub>OZ</sub>                     | I/O Tri–State Output Leakage Current  | T <sub>A</sub> = 25°C, OE = 0 V  | 0.9 – 4.5            | 0.9 – 4.5            | –1.0                    | 1.0                     | μA   |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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## TOTAL STATIC POWER CONSUMPTION ( $I_{CCA} + I_{CCB}$ )

| $V_{CCA}$ (V) | -40°C to +85°C |       |     |       |     |       |     |       |     |       | Unit    |
|---------------|----------------|-------|-----|-------|-----|-------|-----|-------|-----|-------|---------|
|               | $V_{CCB}$ (V)  |       |     |       |     |       |     |       |     |       |         |
|               | 4.5            |       | 3.3 |       | 2.8 |       | 1.8 |       | 0.9 |       |         |
|               | Min            | Max   | Min | Max   | Min | Max   | Min | Max   | Min | Max   |         |
| 4.5           |                | 2     |     | 2     |     | 2     |     | 2     |     | < 1.5 | $\mu$ A |
| 3.3           |                | 2     |     | 2     |     | 2     |     | 2     |     | < 1.5 | $\mu$ A |
| 2.8           |                | < 2   |     | < 1   |     | < 1   |     | < 0.5 |     | < 0.5 | $\mu$ A |
| 1.8           |                | < 1   |     | < 1   |     | < 0.5 |     | < 0.5 |     | < 0.5 | $\mu$ A |
| 0.9           |                | < 0.5 |     | < 0.5 |     | < 0.5 |     | < 0.5 |     | < 0.5 | $\mu$ A |

NOTE: Connect ground before applying supply voltage  $V_{CCA}$  or  $V_{CCB}$ . This device is designed with the feature that the power-up sequence of  $V_{CCA}$  and  $V_{CCB}$  will not damage the IC.

## AC ELECTRICAL CHARACTERISTICS

| Symbol                                 | Parameter                                   | $V_{CCA}$ (V) | -40°C to +85°C |      |     |      |     |      |     |      |     |      | Unit |
|--|---|---------------|----------------|------|-----|------|-----|------|-----|------|-----|------|------|
|  |   |               | $V_{CCB}$ (V)  |      |     |      |     |      |     |      |     |      |      |
|  |   |               | 4.5            |      | 3.3 |      | 2.8 |      | 1.8 |      | 1.2 |      |      |
|  |   |               | Min            | Max  | Min | Max  | Min | Max  | Min | Max  | Min | Max  |      |
| $t_{PLH}$ ,<br>$t_{PHL}$<br>(Note 1)   | Propagation Delay,<br>$A_n$ to $B_n$        | 4.5           |                | 1.6  |     | 1.8  |     | 2.0  |     | 2.1  |     | 2.3  | nS   |
|  |   | 3.3           |                | 1.7  |     | 1.9  |     | 2.1  |     | 2.3  |     | 2.6  |      |
|  |   | 2.8           |                | 1.9  |     | 2.1  |     | 2.3  |     | 2.5  |     | 2.8  |      |
|  |   | 1.8           |                | 2.1  |     | 2.4  |     | 2.5  |     | 2.7  |     | 3.0  |      |
|  |   | 1.2           |                | 2.4  |     | 2.7  |     | 2.8  |     | 3.0  |     | 3.3  |      |
| $t_{PZH}$ ,<br>$t_{PZL}$<br>(Note 1)   | Output Enable,<br>$\overline{OE}$ to $B_n$  | 4.5           |                | 2.6  |     | 3.8  |     | 4.0  |     | 4.1  |     | 4.3  | nS   |
|  |   | 3.3           |                | 3.7  |     | 3.9  |     | 4.1  |     | 4.3  |     | 4.6  |      |
|  |   | 2.5           |                | 3.9  |     | 4.1  |     | 4.3  |     | 4.5  |     | 4.8  |      |
|  |   | 1.8           |                | 4.1  |     | 4.4  |     | 4.5  |     | 4.7  |     | 5.0  |      |
|  |   | 1.2           |                | 4.4  |     | 4.7  |     | 4.8  |     | 5.0  |     | 5.3  |      |
| $t_{PHZ}$ ,<br>$t_{PLZ}$<br>(Note 1)   | Output Disable,<br>$\overline{OE}$ to $B_n$ | 4.5           |                | 2.6  |     | 3.8  |     | 4.0  |     | 4.1  |     | 4.3  | nS   |
|  |   | 3.3           |                | 3.7  |     | 3.9  |     | 4.1  |     | 4.3  |     | 4.6  |      |
|  |   | 2.5           |                | 3.9  |     | 4.1  |     | 4.3  |     | 4.5  |     | 4.8  |      |
|  |   | 1.8           |                | 4.1  |     | 4.4  |     | 4.5  |     | 4.7  |     | 5.0  |      |
|  |   | 1.2           |                | 4.4  |     | 4.7  |     | 4.8  |     | 5.0  |     | 5.3  |      |
| $t_{OSHL}$ ,<br>$t_{OSLH}$<br>(Note 1) | Output to Output Skew, Time                 | 4.5           |                | 0.15 |     | 0.15 |     | 0.15 |     | 0.15 |     | 0.15 | nS   |
|  |   | 3.3           |                | 0.15 |     | 0.15 |     | 0.15 |     | 0.15 |     | 0.15 |      |
|  |   | 2.5           |                | 0.15 |     | 0.15 |     | 0.15 |     | 0.15 |     | 0.15 |      |
|  |   | 1.8           |                | 0.15 |     | 0.15 |     | 0.15 |     | 0.15 |     | 0.15 |      |
|  |   | 1.2           |                | 0.15 |     | 0.15 |     | 0.15 |     | 0.15 |     | 0.15 |      |

1. Propagation delays defined per Figure 2.

## CAPACITANCE

| Symbol    | Parameter                     | Test Conditions  | Typ (Note 2) | Unit |
|-----------|-------------------------------|--|--------------|------|
| $C_{IN}$  | Control Pin Input Capacitance | $V_{CCA} = V_{CCB} = 3.3$ V, $V_I = 0$ V or $V_{CCA/B}$              | 3.5          | pF   |
| $C_{I/O}$ | I/O Pin Input Capacitance     | $V_{CCA} = V_{CCB} = 3.3$ V, $V_I = 0$ V or $V_{CCA/B}$              | 5.0          | pF   |
| $C_{PD}$  | Power Dissipation Capacitance | $V_{CCA} = V_{CCB} = 3.3$ V, $V_I = 0$ V or $V_{CCA}$ , $f = 10$ MHz | 20           | pF   |

2. Typical values are at  $T_A = +25^\circ\text{C}$ .

3.  $C_{PD}$  is defined as the value of the IC's equivalent capacitance from which the operating current can be calculated from:  
 $I_{CC(\text{operating})} \cong C_{PD} \times V_{CC} \times f_{IN} \times N_{SW}$  where  $I_{CC} = I_{CCA} + I_{CCB}$  and  $N_{SW}$  = total number of outputs switching.

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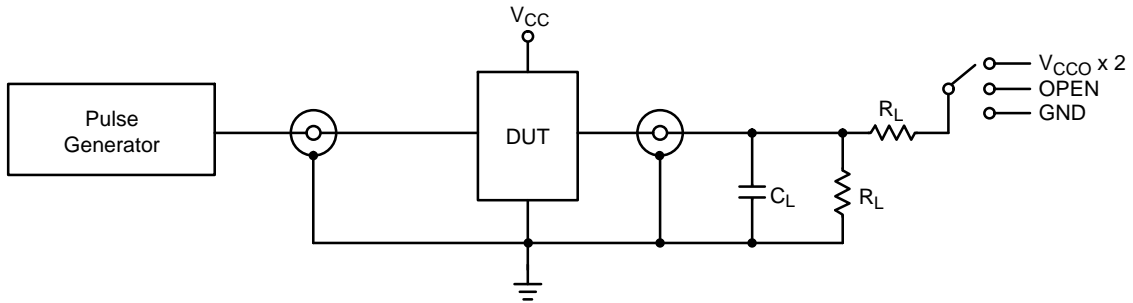
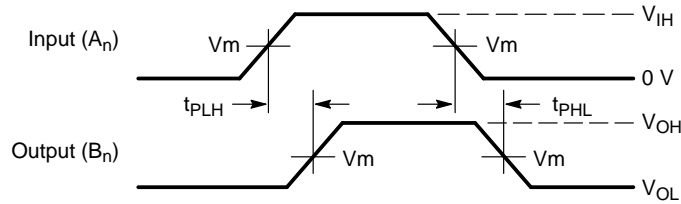


Figure 2. AC (Propagation Delay) Test Circuit

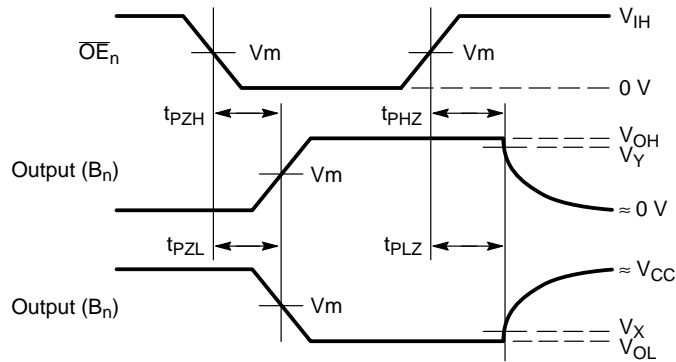
| Test                  | Switch             |
|-----------------------|--------------------|
| $t_{PLH}$ , $t_{PHL}$ | OPEN               |
| $t_{PLZ}$ , $t_{PZL}$ | $V_{CCO} \times 2$ |
| $t_{PHZ}$ , $t_{PZH}$ | GND                |

$C_L = 15 \text{ pF}$  or equivalent (includes probe and jig capacitance)  
 $R_L = 2 \text{ k}\Omega$  or equivalent  
 $Z_{OUT}$  of pulse generator =  $50 \Omega$



Waveform 1 - Propagation Delays

$t_R = t_F = 2.0 \text{ ns}$ , 10% to 90%;  $f = 1 \text{ MHz}$ ;  $t_W = 500 \text{ ns}$



Waveform 2 - Output Enable and Disable Times

$t_R = t_F = 2.0 \text{ ns}$ , 10% to 90%;  $f = 1 \text{ MHz}$ ;  $t_W = 500 \text{ ns}$

Figure 3. AC (Propagation Delay) Test Circuit Waveforms

| Symbol   | $V_{CC}$            |                     |                     |                     |                     |
|----------|---------------------|---------------------|---------------------|---------------------|---------------------|
|          | 3.0 V - 4.5 V       | 2.3 V - 2.7 V       | 1.65 V - 1.95 V     | 1.4 V - 1.6 V       | 0.9 V - 1.3 V       |
| $V_{mA}$ | $V_{CCA}/2$         | $V_{CCA}/2$         | $V_{CCA}/2$         | $V_{CCA}/2$         | $V_{CCA}/2$         |
| $V_{mB}$ | $V_{CCB}/2$         | $V_{CCB}/2$         | $V_{CCB}/2$         | $V_{CCB}/2$         | $V_{CCB}/2$         |
| $V_X$    | $V_{OL} \times 0.1$ | $V_{OL} \times 0.1$ | $V_{OL} \times 0.1$ | $V_{OL} \times 0.1$ | $V_{OL} \times 0.1$ |
| $V_Y$    | $V_{OH} \times 0.9$ | $V_{OH} \times 0.9$ | $V_{OH} \times 0.9$ | $V_{OH} \times 0.9$ | $V_{OH} \times 0.9$ |

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

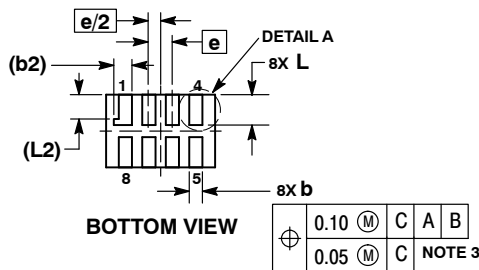
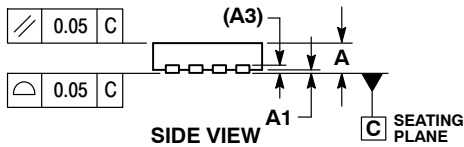
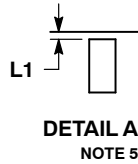
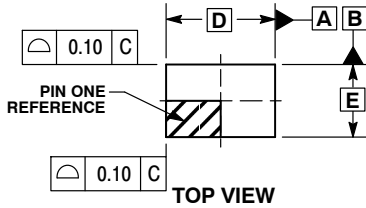
ON Semiconductor®



SCALE 4:1

UDFN8 1.8x1.2, 0.4P  
CASE 517AJ-01  
ISSUE O

DATE 08 NOV 2006

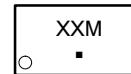


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH MAY NOT EXCEED 0.03 ONTO BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

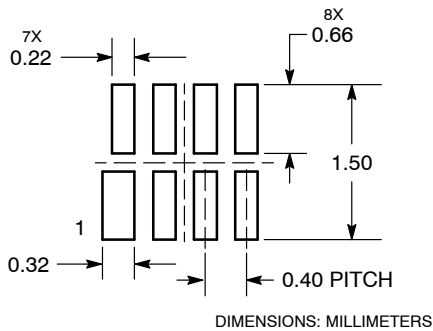
| DIM | MILLIMETERS |      |
|-----|-------------|------|
|     | MIN         | MAX  |
| A   | 0.45        | 0.55 |
| A1  | 0.00        | 0.05 |
| A3  | 0.127       | REF  |
| b   | 0.15        | 0.25 |
| b2  | 0.30        | REF  |
| D   | 1.80        | BSC  |
| E   | 1.20        | BSC  |
| e   | 0.40        | BSC  |
| L   | 0.45        | 0.55 |
| L1  | 0.00        | 0.03 |
| L2  | 0.40        | REF  |

GENERIC MARKING DIAGRAM\*



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

MOUNTING FOOTPRINT  
SOLDERMASK DEFINED



\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 0.10        | 0.25 | 0.004     | 0.010 |
| J   | 0.19        | 0.25 | 0.007     | 0.010 |
| K   | 0.40        | 1.27 | 0.016     | 0.050 |
| M   | 0°          | 8°   | 0°        | 8°    |
| N   | 0.25        | 0.50 | 0.010     | 0.020 |
| S   | 5.80        | 6.20 | 0.228     | 0.244 |

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
 A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 W = Work Week  
 ■ = Pb-Free Package

XXXXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |  |   |   |   |
|--|---|---|---|
| <p><b>STYLE 1:</b><br/> PIN 1. EMITTER<br/> 2. COLLECTOR<br/> 3. COLLECTOR<br/> 4. EMITTER<br/> 5. EMITTER<br/> 6. BASE<br/> 7. BASE<br/> 8. EMITTER</p>   | <p><b>STYLE 2:</b><br/> PIN 1. COLLECTOR, DIE, #1<br/> 2. COLLECTOR, #1<br/> 3. COLLECTOR, #2<br/> 4. COLLECTOR, #2<br/> 5. BASE, #2<br/> 6. EMITTER, #2<br/> 7. BASE, #1<br/> 8. EMITTER, #1</p>               | <p><b>STYLE 3:</b><br/> PIN 1. DRAIN, DIE #1<br/> 2. DRAIN, #1<br/> 3. DRAIN, #2<br/> 4. DRAIN, #2<br/> 5. GATE, #2<br/> 6. SOURCE, #2<br/> 7. GATE, #1<br/> 8. SOURCE, #1</p>                            | <p><b>STYLE 4:</b><br/> PIN 1. ANODE<br/> 2. ANODE<br/> 3. ANODE<br/> 4. ANODE<br/> 5. ANODE<br/> 6. ANODE<br/> 7. ANODE<br/> 8. COMMON CATHODE</p>   |
| <p><b>STYLE 5:</b><br/> PIN 1. DRAIN<br/> 2. DRAIN<br/> 3. DRAIN<br/> 4. DRAIN<br/> 5. GATE<br/> 6. GATE<br/> 7. SOURCE<br/> 8. SOURCE</p>   | <p><b>STYLE 6:</b><br/> PIN 1. SOURCE<br/> 2. DRAIN<br/> 3. DRAIN<br/> 4. SOURCE<br/> 5. SOURCE<br/> 6. GATE<br/> 7. GATE<br/> 8. SOURCE</p>  | <p><b>STYLE 7:</b><br/> PIN 1. INPUT<br/> 2. EXTERNAL BYPASS<br/> 3. THIRD STAGE SOURCE<br/> 4. GROUND<br/> 5. DRAIN<br/> 6. GATE 3<br/> 7. SECOND STAGE Vd<br/> 8. FIRST STAGE Vd</p>                    | <p><b>STYLE 8:</b><br/> PIN 1. COLLECTOR, DIE #1<br/> 2. BASE, #1<br/> 3. BASE, #2<br/> 4. COLLECTOR, #2<br/> 5. COLLECTOR, #2<br/> 6. EMITTER, #2<br/> 7. EMITTER, #1<br/> 8. COLLECTOR, #1</p>                              |
| <p><b>STYLE 9:</b><br/> PIN 1. EMITTER, COMMON<br/> 2. COLLECTOR, DIE #1<br/> 3. COLLECTOR, DIE #2<br/> 4. EMITTER, COMMON<br/> 5. EMITTER, COMMON<br/> 6. BASE, DIE #2<br/> 7. BASE, DIE #1<br/> 8. EMITTER, COMMON</p> | <p><b>STYLE 10:</b><br/> PIN 1. GROUND<br/> 2. BIAS 1<br/> 3. OUTPUT<br/> 4. GROUND<br/> 5. GROUND<br/> 6. BIAS 2<br/> 7. INPUT<br/> 8. GROUND</p>  | <p><b>STYLE 11:</b><br/> PIN 1. SOURCE 1<br/> 2. GATE 1<br/> 3. SOURCE 2<br/> 4. GATE 2<br/> 5. DRAIN 2<br/> 6. DRAIN 2<br/> 7. DRAIN 1<br/> 8. DRAIN 1</p>   | <p><b>STYLE 12:</b><br/> PIN 1. SOURCE<br/> 2. SOURCE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>   |
| <p><b>STYLE 13:</b><br/> PIN 1. N.C.<br/> 2. SOURCE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>  | <p><b>STYLE 14:</b><br/> PIN 1. N-SOURCE<br/> 2. N-GATE<br/> 3. P-SOURCE<br/> 4. P-GATE<br/> 5. P-DRAIN<br/> 6. P-DRAIN<br/> 7. N-DRAIN<br/> 8. N-DRAIN</p>   | <p><b>STYLE 15:</b><br/> PIN 1. ANODE 1<br/> 2. ANODE 1<br/> 3. ANODE 1<br/> 4. ANODE 1<br/> 5. CATHODE, COMMON<br/> 6. CATHODE, COMMON<br/> 7. CATHODE, COMMON<br/> 8. CATHODE, COMMON</p>               | <p><b>STYLE 16:</b><br/> PIN 1. EMITTER, DIE #1<br/> 2. BASE, DIE #1<br/> 3. EMITTER, DIE #2<br/> 4. BASE, DIE #2<br/> 5. COLLECTOR, DIE #2<br/> 6. COLLECTOR, DIE #2<br/> 7. COLLECTOR, DIE #1<br/> 8. COLLECTOR, DIE #1</p> |
| <p><b>STYLE 17:</b><br/> PIN 1. VCC<br/> 2. V2OUT<br/> 3. V1OUT<br/> 4. TXE<br/> 5. RXE<br/> 6. VEE<br/> 7. GND<br/> 8. ACC</p>  | <p><b>STYLE 18:</b><br/> PIN 1. ANODE<br/> 2. ANODE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. CATHODE<br/> 8. CATHODE</p>   | <p><b>STYLE 19:</b><br/> PIN 1. SOURCE 1<br/> 2. GATE 1<br/> 3. SOURCE 2<br/> 4. GATE 2<br/> 5. DRAIN 2<br/> 6. MIRROR 2<br/> 7. DRAIN 1<br/> 8. MIRROR 1</p>   | <p><b>STYLE 20:</b><br/> PIN 1. SOURCE (N)<br/> 2. GATE (N)<br/> 3. SOURCE (P)<br/> 4. GATE (P)<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>   |
| <p><b>STYLE 21:</b><br/> PIN 1. CATHODE 1<br/> 2. CATHODE 2<br/> 3. CATHODE 3<br/> 4. CATHODE 4<br/> 5. CATHODE 5<br/> 6. COMMON ANODE<br/> 7. COMMON ANODE<br/> 8. CATHODE 6</p>  | <p><b>STYLE 22:</b><br/> PIN 1. I/O LINE 1<br/> 2. COMMON CATHODE/VCC<br/> 3. COMMON CATHODE/VCC<br/> 4. I/O LINE 3<br/> 5. COMMON ANODE/GND<br/> 6. I/O LINE 4<br/> 7. I/O LINE 5<br/> 8. COMMON ANODE/GND</p> | <p><b>STYLE 23:</b><br/> PIN 1. LINE 1 IN<br/> 2. COMMON ANODE/GND<br/> 3. COMMON ANODE/GND<br/> 4. LINE 2 IN<br/> 5. LINE 2 OUT<br/> 6. COMMON ANODE/GND<br/> 7. COMMON ANODE/GND<br/> 8. LINE 1 OUT</p> | <p><b>STYLE 24:</b><br/> PIN 1. BASE<br/> 2. EMITTER<br/> 3. COLLECTOR/ANODE<br/> 4. COLLECTOR/ANODE<br/> 5. CATHODE<br/> 6. CATHODE<br/> 7. COLLECTOR/ANODE<br/> 8. COLLECTOR/ANODE</p>                                      |
| <p><b>STYLE 25:</b><br/> PIN 1. VIN<br/> 2. N/C<br/> 3. REXT<br/> 4. GND<br/> 5. IOUT<br/> 6. IOUT<br/> 7. IOUT<br/> 8. IOUT</p>   | <p><b>STYLE 26:</b><br/> PIN 1. GND<br/> 2. dv/dt<br/> 3. ENABLE<br/> 4. ILIMIT<br/> 5. SOURCE<br/> 6. SOURCE<br/> 7. SOURCE<br/> 8. VCC</p>  | <p><b>STYLE 27:</b><br/> PIN 1. ILIMIT<br/> 2. OVLO<br/> 3. UVLO<br/> 4. INPUT+<br/> 5. SOURCE<br/> 6. SOURCE<br/> 7. SOURCE<br/> 8. DRAIN</p>  | <p><b>STYLE 28:</b><br/> PIN 1. SW_TO_GND<br/> 2. DASIC OFF<br/> 3. DASIC_SW_DET<br/> 4. GND<br/> 5. V_MON<br/> 6. VBULK<br/> 7. VBULK<br/> 8. VIN</p>  |
| <p><b>STYLE 29:</b><br/> PIN 1. BASE, DIE #1<br/> 2. EMITTER, #1<br/> 3. BASE, #2<br/> 4. EMITTER, #2<br/> 5. COLLECTOR, #2<br/> 6. COLLECTOR, #2<br/> 7. COLLECTOR, #1<br/> 8. COLLECTOR, #1</p>                        | <p><b>STYLE 30:</b><br/> PIN 1. DRAIN 1<br/> 2. DRAIN 1<br/> 3. GATE 2<br/> 4. SOURCE 2<br/> 5. SOURCE 1/DRAIN 2<br/> 6. SOURCE 1/DRAIN 2<br/> 7. SOURCE 1/DRAIN 2<br/> 8. GATE 1</p>                           |   |   |

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

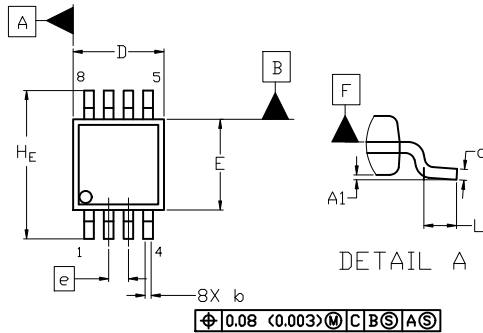
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SCALE 2:1

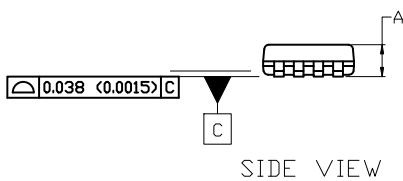
### Micro8 CASE 846A-02 ISSUE K

DATE 16 JUL 2020

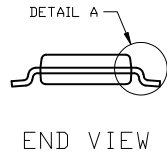


TOP VIEW

NOTE 3



SIDE VIEW



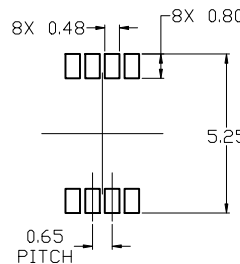
END VIEW

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION *b* DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

⌀ 0.08 (0.003) M C B S A S

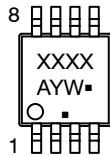
| DIM            | MILLIMETERS |      |      |
|----------------|-------------|------|------|
|                | MIN.        | NOM. | MAX. |
| A              | ---         | ---  | 1.10 |
| A1             | 0.05        | 0.08 | 0.15 |
| <i>b</i>       | 0.25        | 0.33 | 0.40 |
| <i>c</i>       | 0.13        | 0.18 | 0.23 |
| D              | 2.90        | 3.00 | 3.10 |
| E              | 2.90        | 3.00 | 3.10 |
| <i>e</i>       | 0.65 BSC    |      |      |
| H <sub>E</sub> | 4.75        | 4.90 | 5.05 |
| L              | 0.40        | 0.55 | 0.70 |



RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

### GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**STYLE 1:**

1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

**STYLE 2:**

1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

**STYLE 3:**

1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

|                         |                    |  |
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