ON Semiconductor

Is Now



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Single 2-Input NOR Gate

NL17SV02

The NL17SV02 is a single 2-input NOR gate in tiny footprint packages. The device is designed to operate for $V_{CC} = 0.9 \text{ V}$ to 3.6 V.

Features

- Designed for 0.9 V to 3.6 V V_{CC} Operation
- 1.5 ns t_{PD} at 3.3 V (Typ)
- Inputs/Outputs Over-Voltage Tolerant up to 3.6 V
- I_{OFF} Supports Partial Power Down Protection
- Source/Sink 24 mA at 3.3 V
- Available in SOT-353, SOT-553, SOT-953, SC-74A and UDFN 1Packages
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

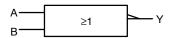
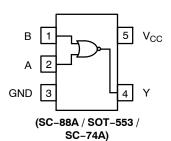
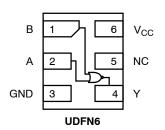


Figure 1. Logic Symbol





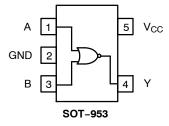
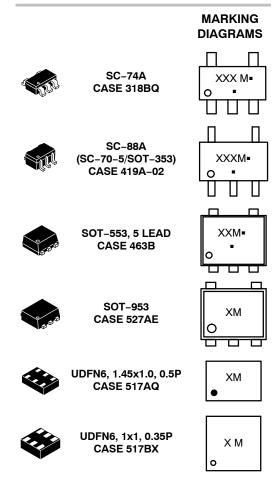


Figure 2. Pinout (Top View)



ON Semiconductor®

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X, XX = Specific Device Code M = Date Code*

= Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present.

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

PIN ASSIGNMENT

Pin	SOT-953	SC88A / SOT553 / SC-74A	UDFN6
1	Α	В	В
2	GND	Α	А
3	В	GND	GND
4	Υ	Υ	Y
5	V _{CC}	V _{CC}	NC
6	-	-	V _{CC}

FUNCTION TABLE

Inp	Output Y = A + B	
Α	В	Υ
L	L	Н
L	Н	L
Н	L	L
Н	Н	L

MAXIMUM RATINGS

Symbol	Characteristics		Value	Unit
V _{CC}	DC Supply Voltage		-0.5 to +4.3	V
V _{IN}	DC Input Voltage		-0.5 to +4.3	V
V _{OUT}	Tri–St	High or Low State) ate Mode (Note 1) Mode (V _{CC} = 0 V)	-0.5 to V _{CC} + 0.5 -0.5 to +4.3 -0.5 to +4.3	V
I _{IK}	DC Input Diode Current	V _{IN} < GND	-50	mA
I _{OK}	DC Output Diode Current	V _{OUT} < GND	-50	mA
l _{OUT}	DC Output Source/Sink Current		±50	mA
I _{CC} or I _{GND}	DC Supply Current per Supply Pin or Ground Pin		±50	mA
T _{STG}	Storage Temperature Range		-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
TJ	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)	SC-88A SOT-553 SOT-953 SC-74A UDFN6	377 324 254 320 154	°C/W
P _D	Power Dissipation in Still Air	SC-88A SOT-553 SOT-953 SC-74A UDFN6	332 386 491 390 812	mW
MSL	Moisture Sensitivity		Level 1	-
F _R	Flammability Rating Oxyg	en Index: 28 to 34	UL 94 V-0 @ 0.125 in	-
V _{ESD}		uman Body Model ged Device Model	2000 1000	V
I _{Latchup}	Latchup Performance (Note 4)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. Applicable to devices with outputs that may be tri-stated.
- Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow per JESD51-7.
 HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.
 4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Max	Unit
V _{CC}	Positive DC Supply Voltage	0.9	3.6	V
V _{IN}	DC Input Voltage	0	3.6	V
V _{OUT}	DC Output Voltage Active-Mode (Higher Tri-State Power-Down Mode)	Mode (Note 1) 0	V _{CC} 3.6 3.6	
T _A	Operating Temperature Range		+125	°C
t _r , t _f	Input Transition Rise and Fall Time		20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

				T	A = 25°	С	T _A = -55°C	to +125°C	
Symbol	Parameter	Condition	V _{CC} (V)	Min	Тур	Max	Min	Max	Unit
V _{IH} High-Level Input	•		0.9	-	0.5	-	-	-	٧
	Voltage		1.1 to 1.3	0.65 x V _{CC}	-	-	0.65 x V _{CC}	-	1
			1.4 to 1.6	0.65 x V _{CC}	-	-	0.65 x V _{CC}	-	1
			1.65 to 1.95	0.65 x V _{CC}	-	-	0.65 x V _{CC}	-	1
			2.3 to < 2.7	1.6	-	-	1.6	-	
			2.7 to 3.6	2.0	-	-	2.0	-	
V _{IL}	Low-Level Input		0.9	-	0.5	-	-	-	٧
	Voltage		1.1 to 1.3	-	-	0.35 x V _{CC}	_	0.35 x V _{CC}	1
			1.4 to 1.6	-	-	0.35 x V _{CC}	-	0.35 x V _{CC}	
			1.65 to 1.95	-	-	0.35 x V _{CC}	-	0.35 x V _{CC}	
			2.3 to < 2.7	-	-	0.7	-	0.7	
			2.7 to 3.6	-	-	0.8	-	0.8	
V _{OH}	High-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}							٧
		I _{OH} = -100 μA	0.9	_	V _{CC} – 0.1	_	-	-	
			1.1 to 1.3	V _{CC} - 0.1	-	-	V _{CC} - 0.1	-	
			1.4 to 1.6	V _{CC} – 0.1	_	-	V _{CC} – 0.1	-	
			1.65 to 1.95	V _{CC} - 0.2	-	-	V _{CC} - 0.2	-	
			2.3 to <2.7	V _{CC} – 0.2	-	-	V _{CC} - 0.2	-	
			2.7 to 3.6	V _{CC} – 0.2	-	-	V _{CC} - 0.2	-	
		$I_{OH} = -2 \text{ mA}$	1.1 to 1.3	0.75 x V _{CC}	_	-	0.75 x V _{CC}	-	
		$I_{OH} = -4 \text{ mA}$	1.4 to 1.6	0.75 x V _{CC}	_	-	0.75 x V _{CC}	-	
		$I_{OH} = -6 \text{ mA}$	1.65 to 1.95	1.25	-	-	1.25	-	
			2.3 to 2.7	2.0	-	-	2.0	-	
		I _{OH} = −12 mA	2.3 to 2.7	1.8	_	-	1.8	-	
			2.7 to 3.6	2.2	-	-	2.2	-	
		I _{OH} = −18 mA	2.3 to 2.7	1.7	_	-	1.7	-	
			2.7 to 3.6	2.4	-	-	2.4	-	
		$I_{OH} = -24 \text{ mA}$	2.7 to 3.6	2.2	-	-	2.2	_	

DC ELECTRICAL CHARACTERISTICS (continued)

				$T_A = 25^{\circ}C$ $T_A = -55^{\circ}C \text{ to } +125^{\circ}$		C to +125°C			
Symbol	Parameter	Condition	V _{CC} (V)	Min	Тур	Max	Min	Max	Unit
V _{OL}	Low-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}							V
		I _{OL} = 100 μA	0.9	_	0.1	-	_	-	
			1.1 to 1.3	-	-	0.1	-	0.1	
			1.4 to 1.6	_	_	0.1	_	0.1	
			1.65 to 1.95	-	-	0.2	-	0.2	
			2.3 to < 2.7	-	-	0.2	-	0.2	
			2.7 to 3.6	_	_	0.2	_	0.2	
		I _{OL} = 2 mA	1.1 to 1.3	-	-	0.25 x V _{CC}	-	0.25 x V _{CC}	
		I _{OL} = 4 mA	1.4 to 1.6	-	-	0.25 x V _{CC}	-	0.25 x V _{CC}	
		I _{OL} = 6 mA	1.65 to 1.95	-	_	0.3	-	0.3	
			2.3 to 2.7	-	-	0.3	1	0.3	
		I _{OL} = 12 mA	2.3 to 2.7	-	_	0.4	-	0.4	
			2.7 to 3.6	-	-	0.4	-	0.4	
		I _{OL} = 18 mA	2.3 to 2.7	-	_	0.6	-	0.6	
			2.7 to 3.6	-	-	0.4	-	0.4	
		I _{OL} = 24 mA	2.7 to 3.6	-	-	0.55	1	0.55	
I _{IN}	Input Leakage Current	V _{IN} = 3.6 V or GND	0.9 to 3.6	-	-	±0.1	-	±0.9	μΑ
l _{OFF}	Power Off Leakage Current	V _{IN} = 3.6 V or V _{OUT} = 3.6 V	0	_	-	1.0	_	5.0	μΑ
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND	0.9 to 3.6	_	-	0.9	_	5.0	μΑ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

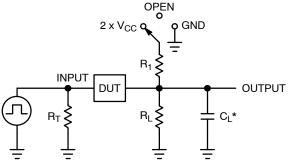
AC ELECTRICAL CHARACTERISTICS

				1	Γ _A = 25°0)	T _A = -55°C	to +125°C	
Symbol	Parameter	Condition	V _{CC} (V)	Min	Тур	Max	Min	Max	Unit
t _{PLH} , t _{PHL} Propagation Delay,		$R_L = 1 M\Omega$, $C_L = 15 pF$	0.9	-	14.4	-	-	-	ns
	(A or B) to Y (Figures 3 and 4)	(A or B) to Y (Figures 3 and 4) $R_L = 2 k\Omega, C_L = 15 pF$	1.10 to 1.30	-	6.3	15.0	-	18.6	
	,		1.40 to 1.60	-	3.4	8.7	-	9.7	
		$R_L = 500 \ \Omega, \ C_L = 30 \ pF$	1.65 to 1.95	-	2.4	6.0	-	6.8	
			2.3 to 2.7	-	1.8	4.1	-	4.7	
			2.7 to 3.6	-	1.5	3.3	_	4.0	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition	Typical (T _A = 25°C)	Unit
C _{IN}	Input Capacitance	V _{CC} = 0 V	2.0	pF
C _{OUT}	Output Capacitance	V _{CC} = 0 V	4.5	pF
C _{PD}	Power Dissipation Capacitance (Note 5)	10 MHz, V_{CC} = 0.9 to 3.6 V, V_{IN} = 0 V or V_{CC}	20	pF

^{5.} C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no–load dynamic power consumption: P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

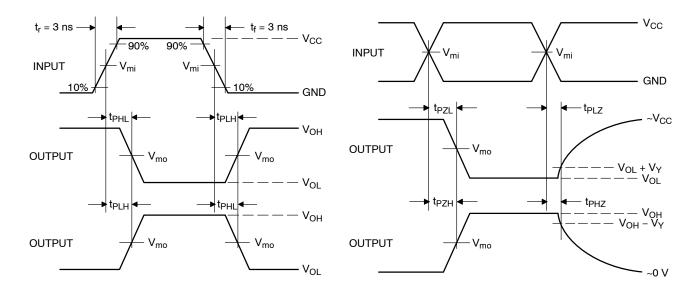


Test	Switch Position
t _{PLH} / t _{PHL}	Open
t _{PLZ} / t _{PZL}	2 x V _{CC}
t _{PHZ} / t _{PZH}	GND

C_L includes probe and jig capacitance

 R_T is Z_{OUT} of pulse generator (typically 50 Ω) f=1 MHz

Figure 3. Test Circuit



		V _{mo} , V		
V _{CC} , V	V _{mi} , V	t _{PLH} , t _{PHL}	t _{PZL} , t _{PLZ} , t _{PZH} , t _{PHZ}	V _Y , V
0.9	V _{CC} /2	V _{CC} / 2	V _{CC} / 2	0.1
1.1 to 1.3	V _{CC} /2	V _{CC} / 2	V _{CC} / 2	0.1
1.4 to 1.6	V _{CC} /2	V _{CC} / 2	V _{CC} / 2	0.1
1.65 to 1.95	V _{CC} /2	V _{CC} / 2	V _{CC} / 2	0.15
2.3 to 2.7	V _{CC} /2	V _{CC} / 2	V _{CC} / 2	0.15
3.0 to 3.6	1.5	1.5	1.5	0.3

Figure 4. Switching Waveforms

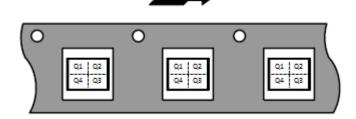
ORDERING INFORMATION

Device	Package	Marking	Pin 1 Orientation (See below)	Shipping [†]
NL17SV02DFT2G (Contact ON Semiconductor)	SC-88A	TBD	Q4	3000 / Tape & Reel
NL17SV02XV5T2G	SOT-553	UK	Q4	4000 / Tape & Reel
NL17SV02P5T5G (Contact ON Semiconductor)	SOT-953	TBD	Q2	8000 / Tape & Reel
NL17SV02DBVT1G (Contact ON Semiconductor)	SC-74A	TBD	Q4	3000 / Tape & Reel
NL17SV02MU1TCG (Contact ON Semiconductor)	UDFN6, 1.45 x 1.0, 0.5P	TBD	Q4	3000 / Tape & Reel
NL17SV02MU3TCG (Contact ON Semiconductor)	UDFN6, 1.0 x 1.0, 0.35P	TBD	Q4	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Pin 1 Orientation in Tape and Reel

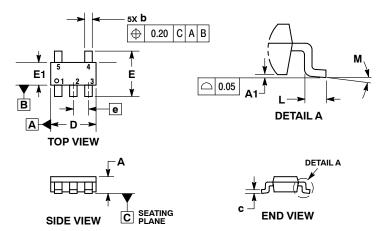
Direction of Feed



^{*}NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

PACKAGE DIMENSIONS

SC-74A CASE 318BQ **ISSUE B**



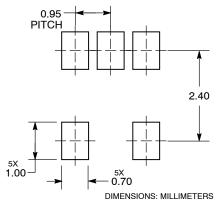
NOTES:

- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
 4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEPT 0.15 PER SIDE EXCEED 0.15 PER SIDE.

	MILLIMETERS				
DIM	MIN	MAX			
Α	0.90	1.10			
A1	0.01	0.10			
b	0.25	0.50			
С	0.10	0.26			
D	2.85	3.15			
E	2.50	3.00			
E1	1.35	1.65			
е	0.95 BSC				
L	0.20	0.60			
М	0°	10°			

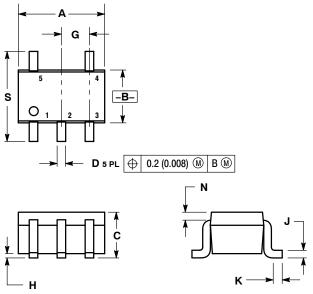
RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

SC-88A (SC-70-5/SOT-353) CASE 419A-02 ISSUE L



NOTES:

- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

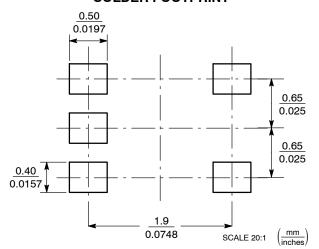
 2. CONTROLLING DIMENSION: INCH.

 3. 419A-01 OBSOLETE: NEW STANDARD 419A-02.

 4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE PLURGE. BURRS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.071	0.087	1.80	2.20
В	0.045	0.053	1.15	1.35
С	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
Н		0.004		0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

SOLDER FOOTPRINT



STYLE 1:
PIN 1. BASE
EMITTER
3. BASE
COLLECTOR
COLLECTOR

STYLE 6:

PIN 1. ANODE 2. EMITTER 3. BASE 4. COLLECTOR 5. CATHODE

STYLE 2:

STYLE 3: PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. CATHODE 1 STYLE 4: PIN 1. SOURCE 1 2. DRAIN 1/2 3. SOURCE 1 4. GATE 1 5. GATE 2

STYLE 5: PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 8:

STYLE 9: PIN 1. ANODE 2. CATHODE 3. ANODE 4. ANODE 5. ANODE

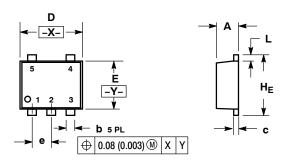
PIN 1. EMITTER 2 2. BASE 2 3. EMITTER 1 4. COLLECTOR 5. COLLECTOR 2/BASE 1 STYLE 7: PIN 1. BASE 2. EMITTER 3. BASE 4. COLLECTOR 5. COLLECTOR

PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE 5. EMITTER

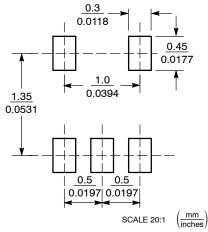
PACKAGE DIMENSIONS

SOT-553, 5 LEAD CASE 463B

ISSUE C



RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

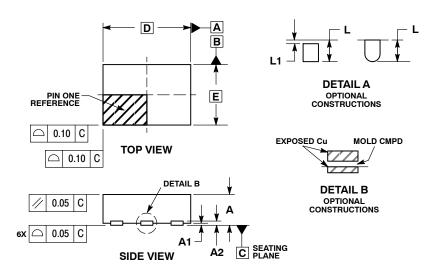
- IES:
 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: MILLIMETERS
 MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH
 THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM
 THICKNESS OF BASE MATERIAL.

	MILLIMETERS		INCHES			
DIM	MIN	NOM	MAX	MIN	NOM	MAX
Α	0.50	0.55	0.60	0.020	0.022	0.024
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.08	0.13	0.18	0.003	0.005	0.007
D	1.55	1.60	1.65	0.061	0.063	0.065
Е	1.15	1.20	1.25	0.045	0.047	0.049
е	0.50 BSC			0.020 BS0		
L	0.10	0.20	0.30	0.004	0.008	0.012
HE	1.55	1.60	1.65	0.061	0.063	0.065

STYLE 1: PIN 1. BASE 2. EMITTER 3. BASE 4. COLLECTOR 5. COLLECTOR	STYLE 2: PIN 1. CATHODE 2. COMMON ANODE 3. CATHODE 2 4. CATHODE 3 5. CATHODE 4	STYLE 3: PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. CATHODE 1	STYLE 4: PIN 1. SOURCE 1 2. DRAIN 1/2 3. SOURCE 1 4. GATE 1 5. GATE 2	STYLE 5: PIN 1. ANODE 2. EMITTER 3. BASE 4. COLLECTOR 5. CATHODE
STYLE 6: PIN 1. EMITTER 2 2. BASE 2 3. EMITTER 1 4. COLLECTOR 1 5. COLLECTOR 2/BASE 1	STYLE 7: PIN 1. BASE 2. EMITTER 3. BASE 4. COLLECTOR 5. COLLECTOR	STYLE 8: PIN 1. CATHODE 2. COLLECTOR 3. N/C 4. BASE 5. EMITTER	STYLE 9: PIN 1. ANODE 2. CATHODE 3. ANODE 4. ANODE 5. ANODE	

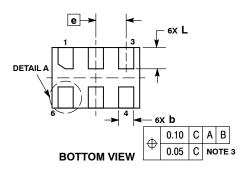
PACKAGE DIMENSIONS

UDFN6, 1.45x1.0, 0.5P CASE 517AQ ISSUE O

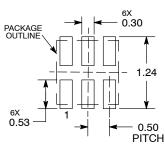


- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

	MILLIMETERS		
DIM	MIN	MAX	
Α	0.45	0.55	
A1	0.00	0.05	
A2	0.07 REF		
b	0.20	0.30	
D	1.45	BSC	
E	1.00 BSC		
е	0.50 BSC		
L	0.30	0.40	
L1		0.15	



MOUNTING FOOTPRINT

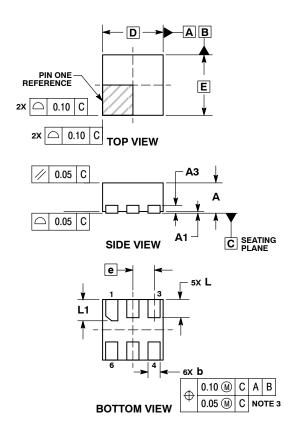


DIMENSIONS: MILLIMETERS

^{*}For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

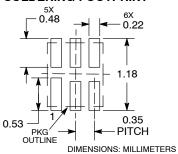
UDFN6, 1x1, 0.35P CASE 517BX ISSUE O



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 CONTROLLING DIMENSION: MILLIMETERS.
 DIMENSION & APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
 PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

	MILLIMETERS		
DIM	MIN	MAX	
Α	0.45	0.55	
A1	0.00	0.05	
А3	0.13 REF		
b	0.12	0.22	
D	1.00 BSC		
Е	1.00 BSC		
е	0.35 BSC		
L	0.25	0.35	
L1	0.30	0.40	

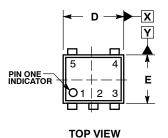
RECOMMENDED SOLDERING FOOTPRINT*

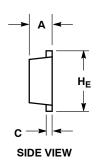


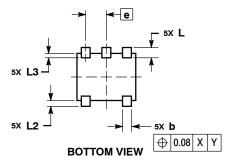
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

SOT-953 CASE 527AE ISSUE E







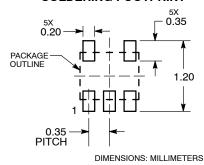
NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL
- MINIMUM THICKNESS OF THE BASE MATERIAL.

 DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

FLASH, FROTRUSIONS, ON C				
	MILLIMETERS			
DIM	MIN	NOM	MAX	
Α	0.34	0.37	0.40	
b	0.10	0.15	0.20	
С	0.07	0.12	0.17	
D	0.95	1.00	1.05	
Е	0.75	0.80	0.85	
е	0.35 BSC			
HE	0.95	1.00	1.05	
L	0.175 REF			
L2	0.05	0.10	0.15	
L3			0.15	

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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