NILMS4501N

Power MOSFET with Current Mirror FET

24 V, 9.5 A, N−Channel, ESD Protected, 1:250 Current Mirror, SO−8 Leadless

N−Channel MOSFET with 1:250 current mirror device utilizing the latest ON Semiconductor technology to achieve low figure of merit while keeping a high accuracy in the linear region. This device takes advantage of the latest leadless QFN package to improve thermal transfer.

Features

- Current Sense MOSFET
- ± 15% Current Mirror Accuracy
- ESD Protected on the Main and the Mirror MOSFET
- Low Gate Charge
- Pb−Free Package is Available*

Applications

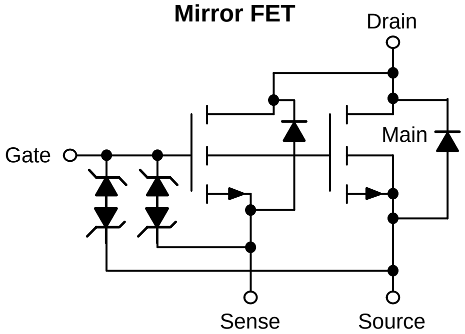
- DC−DC Converters
- Voltage Regulator Modules
- Small DC Motor Controls

ON Semiconductor®

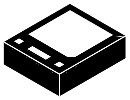
http://onsemi.com

V_{DSS}	$R_{DS(on)}$ Typ	I_D MAX
24 V	12 mΩ @ 4.5 V	9.5 A

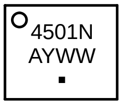
N−Channel with Current Mirror FET



MARKING DIAGRAM

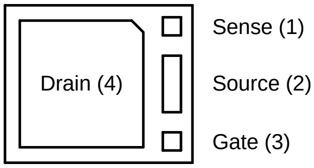


PLLP4
CASE 508AA



4501N = Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

PIN CONNECTIONS



(Bottom View)

ORDERING INFORMATION

Device	Package	Shipping†
NILMS4501NR2	PLLP4	2500/Tape & Reel
NILMS4501NR2G	PLLP4 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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MAIN MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	24	V
Gate−to−Source Voltage	V_{GS}	±10	V
Drain Current (Note 1)			
Continuous @ T_A = 25°C	I_D	9.5	Adc
Continuous @ T_A = 100°C	I_D	6.7	Adc
Pulsed ($t_p \leq 10$ s)	I_{DM}	14	Apk
Total Power Dissipation @ T_A = 25°C (Note 1)	P_D	2.7	W
Total Power Dissipation @ T_A = 25°C (Note 2)	P_D	1.4	
Thermal Resistance			°C/W
Junction−to−Ambient (Note 1)	$R_{\theta JA}$	55	
Junction−to−Ambient (Note 2)	$R_{\theta JA}$	110	
Junction−to−Ambient ($t_p \leq 10$ s) (Note 3)	$R_{\theta JA}$	25	
Operating Junction and Storage Temperature	T_J, T_{STG}	−55 to 175	°C
Single Pulse Drain−to−Source Avalanche (V_{DD} = 24 V, V_{GS} = 10 V, I_L = 9.5 A, L = 1.0 mH, R_G = 25 Ω)	E_{AS}	50	mJ
Electrostatic Discharge Capability			V
Human Body Model	ESD_{HBM}	4000	
Charged Device Model	CMD	2000	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Surface mounted on FR4 board using the minimum recommended pad size (Cu area = 0.0821 in sq).
3. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces) and 200 LFM airflow.

MAIN MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$				
(V_{GS} = 0 V, I_D = 250 μA)		24	29	−	V
Temperature Coefficient (Positive)		−	23	−	mV/°C
Zero Gate Voltage Drain Current	I_{DSS}				μA
(V_{DS} = 24 V, V_{GS} = 0 V)		−	0.05	1.0	
(V_{DS} = 24 V, V_{GS} = 0 V, T_J = 125°C)		−	1.0	100	
(V_{DS} = 24 V, V_{GS} = 0 V, T_J = 175°C)		−	30	100	
Gate−Body Leakage Current	I_{GSS}				
(V_{GS} = 3.0 V, V_{DS} = 0 V)		−	40	100	nA
(V_{GS} = 9.0 V, V_{DS} = 0 V)		−	1.3	10	μA
ON CHARACTERISTICS					
Gate Threshold Voltage	$V_{GS(th)}$				
(V_{DS} = V_{GS}, I_D = 250 μA)		1.1	1.60	2.0	V
Threshold Temperature Coefficient (Negative)		−	−5.0	−	mV/°C
Static Drain−to−Source On−Resistance (Note 4)	$R_{DS(on)}$				mΩ
(V_{GS} = 10 V, I_D = 6.0 A, T_J @ 25°C)		−	9.0	13	
(V_{GS} = 10 V, I_D = 6.0 A, T_J @ 125°C)		−	12	17	
(V_{GS} = 10 V, I_D = 6.0 A, T_J @ 175°C)		−	14	20	
Static Drain−to−Source On−Resistance (Note 4)	$R_{DS(on)}$				mΩ
(V_{GS} = 4.5 V, I_D = 6.0 A, T_J @ 25°C)		−	12	16	
(V_{GS} = 4.5 V, I_D = 6.0 A, T_J @ 125°C)		−	16	20	
(V_{GS} = 4.5 V, I_D = 6.0 A, T_J @ 175°C)		−	18	24	
Main/Mirror MOSFET Current Ratio	I_{RAT}	212	250	287	−
(V_{GS} = 4.5 V, I_D = 1.0 A)		−	268	−	
(V_{GS} = 4.5 V, I_D = 1.0 A, T_A = 175°C)					
Forward Transconductance (Note 4) (V_{DS} = 6.0 V, I_D = 6.0 A)	g_{FS}	15	23	−	Mhos

4. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

MAIN MOSFET ELECTRICAL CHARACTERISTICS (continued) (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS (Note 6)						
Input Capacitance	(V_{DS} = 6.0 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}	−	1380	1500	pF
Output Capacitance		C_{oss}	−	870	1000	
Transfer Capacitance		C_{rss}	−	275	350	
SWITCHING CHARACTERISTICS (Note 6)						
Turn−On Delay Time	(V_{DD} = 6.0 V, I_D = 2.0 A, V_{GS} = 4.5 V, R_G = 2.5 Ω)	$t_{d(on)}$	−	12	14	ns
Rise Time		t_r	−	15	18	
Turn−Off Delay Time		$t_{d(off)}$	−	17	20	
Fall Time		t_f	−	6.0	8.0	
Turn−On Delay Time	(V_{DD} = 6.0 V, I_D = 2.0 A, V_{GS} = 10 V, R_G = 2.5 Ω)	$t_{d(on)}$	−	8.5	11	ns
Rise Time		t_r	−	15	20	
Turn−Off Delay Time		$t_{d(off)}$	−	22.5	27	
Fall Time		t_f	−	6.5	9.0	
Gate Charge	(V_{DS} = 6.0 V, I_D = 2.0 A, V_{GS} = 4.5 V)	Q_T	−	11	14	nC
		$Q_{G(th)}$	−	1.7	2.5	
		Q_{gs}	−	3.5	4.5	
		Q_{gd}	−	3.6	4.3	
Gate Charge	(V_{DS} = 6.0 V, I_D = 2.0 A, V_{GS} = 10 V)	Q_T	−	23.5	25	nC
		$Q_{G(th)}$	−	4.4	5.5	
		Q_{gs}	−	5.6	10	
		Q_{gd}	−	2.5	7.0	
SOURCE−DRAIN DIODE CHARACTERISTICS						
Forward On−Voltage (Notes 5 & 6)	(I_S = 6.0 A, V_{GS} = 0 V) (I_S = 6.0 A, V_{GS} = 0 V, T_J = 175°C)	V_{SD}	− −	0.80 0.57	1.1 −	V
Reverse Recovery Time (Note 6)	(I_S = 3.0 A, V_{GS} = 0 V, dI_S/dt = 100 A/μs)	t_{rr}	−	42	55	ns
		t_a	−	19.5	25	
		t_b	−	22.5	30	
Reverse Recovery Stored Charge (Note 6)		Q_{RR}	−	0.042	0.06	μC

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

TYPICAL ELECTRICAL CHARACTERISTICS

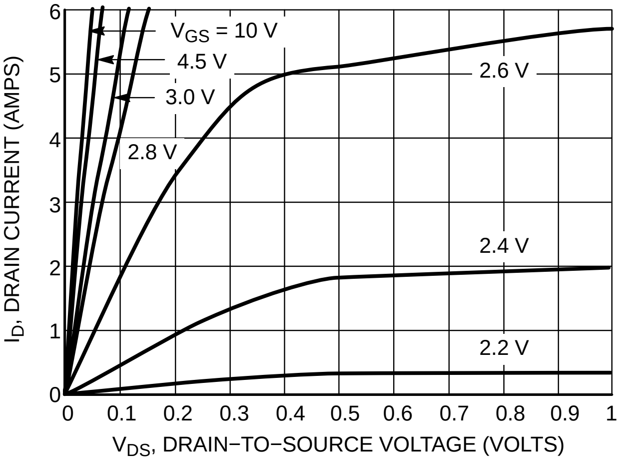


Figure 1. On−Region Characteristics

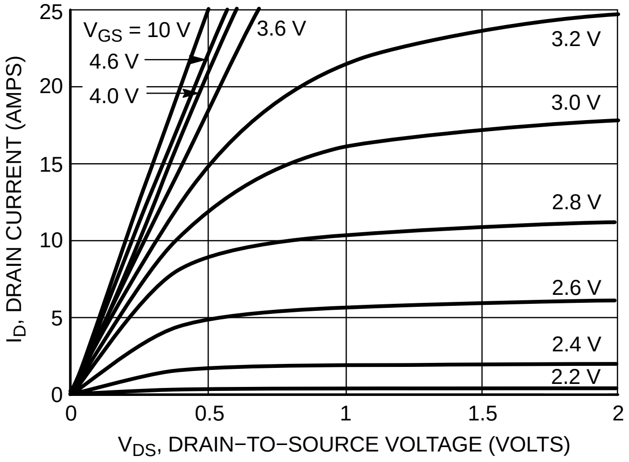


Figure 2. On−Region Characteristics

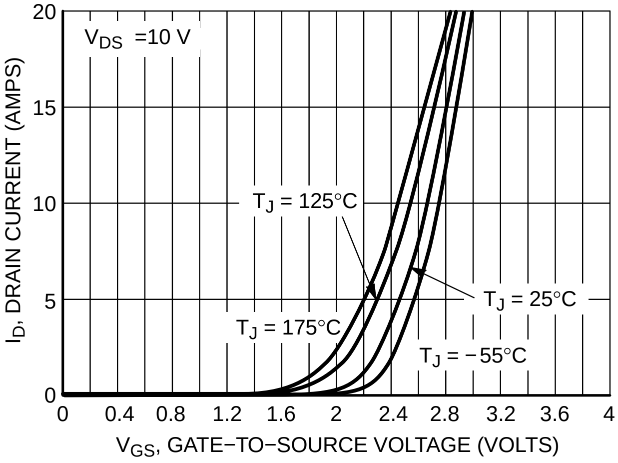


Figure 3. Transfer Characteristics

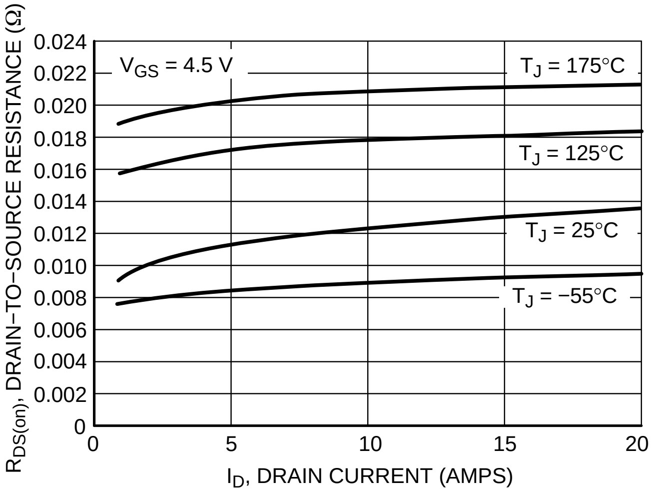


Figure 4. On−Resistance versus Drain Current and Temperature

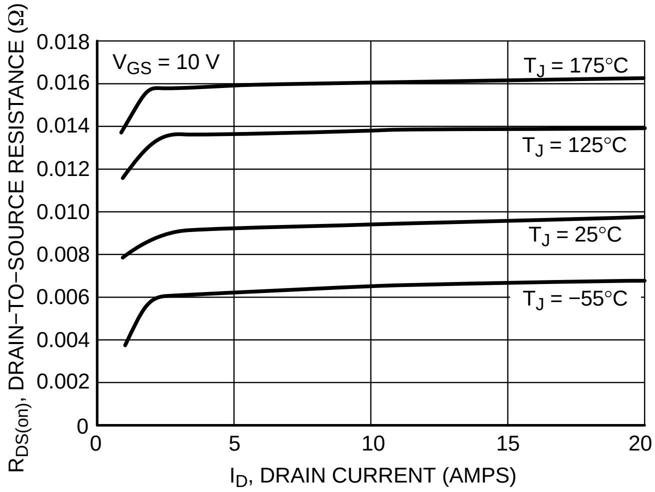


Figure 5. On−Resistance versus Drain Current and Temperature

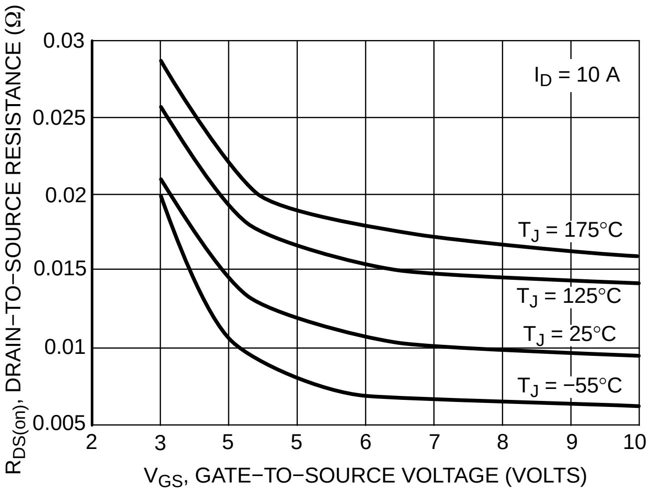


Figure 6. On−Resistance versus Gate Voltage and Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

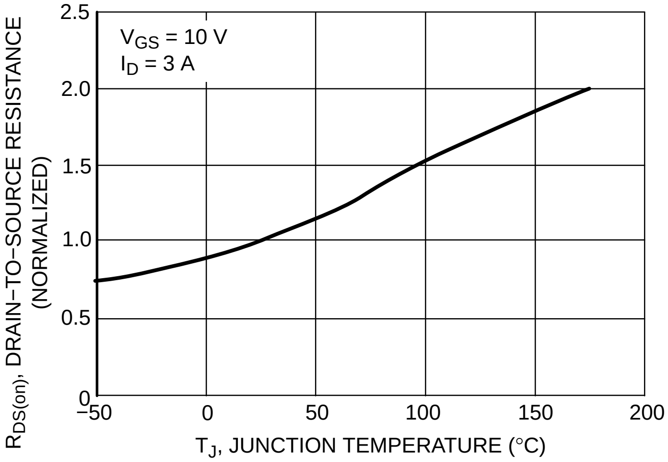


Figure 7. On−Resistance Variation with Temperature

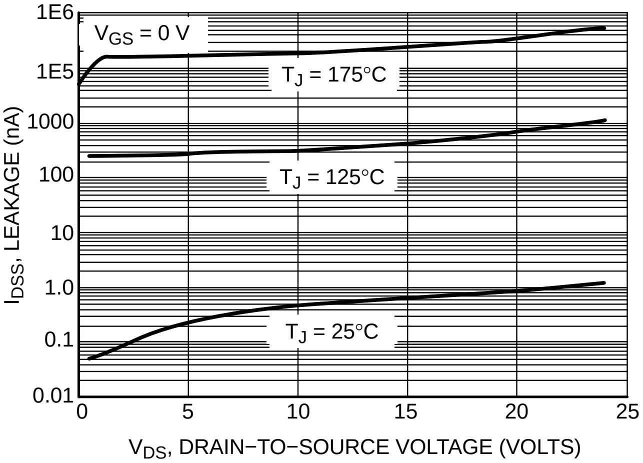


Figure 8. Drain−To−Source Leakage Current versus Voltage

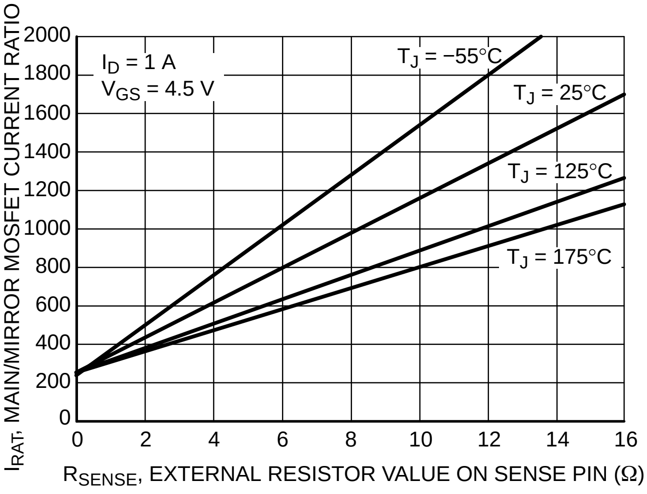


Figure 9. Current Ratio versus R_{SENSE}

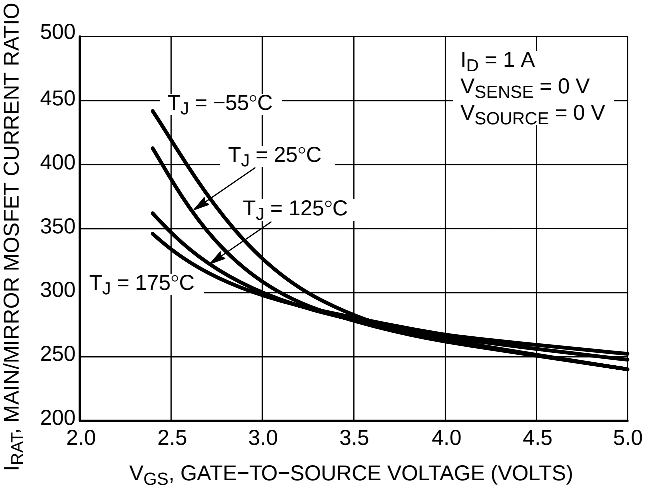


Figure 10. Current Ratio versus V_{GS}

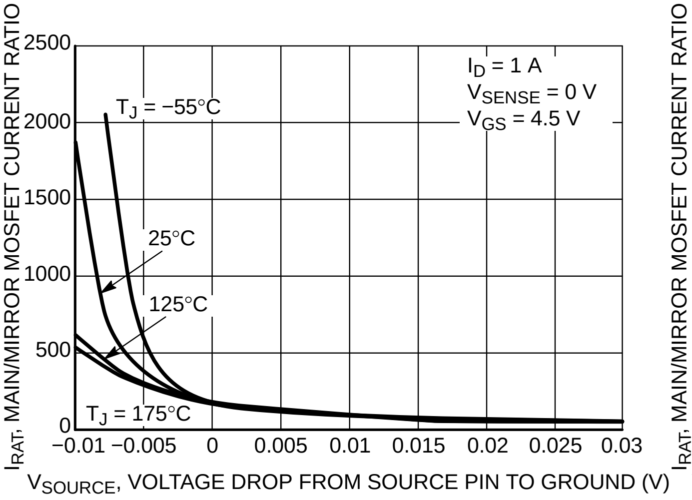


Figure 11. I_{RATIO} versus V_{SOURCE}

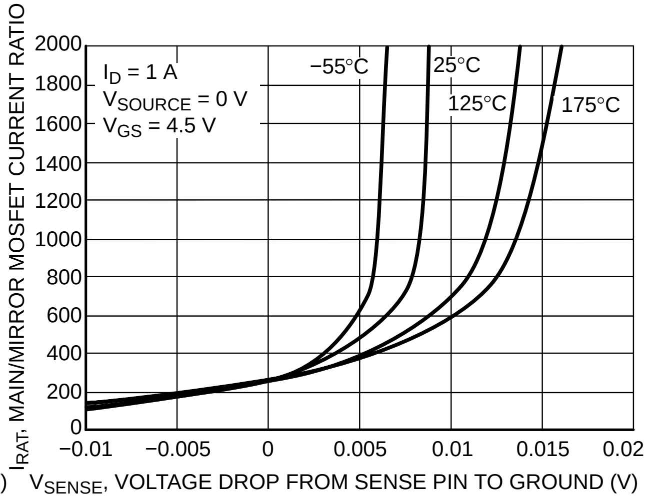


Figure 12. Current Ratio versus V_{SENSE}

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain−gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \text{ x } R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \text{ x } R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn−on and turn−off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \text{ In } [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \text{ In } (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off−state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on−state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

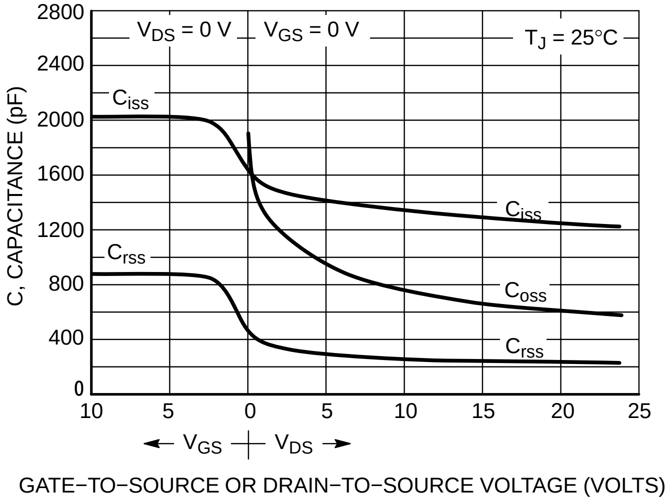


Figure 13. Capacitance Variation

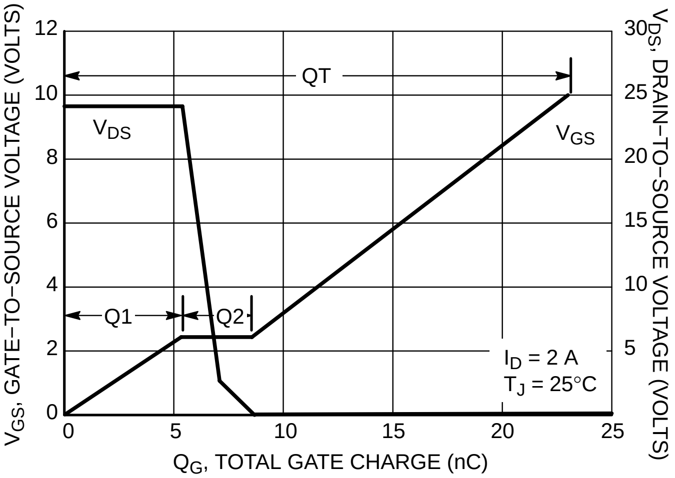


Figure 14. Gate−To−Source and Drain−To−Source Voltage versus Total Charge

DRAIN−TO−SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 15. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

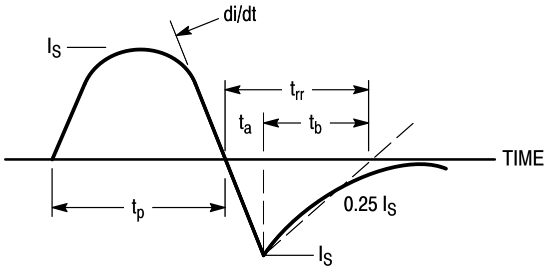


Figure 15. Diode Reverse Recovery Waveform

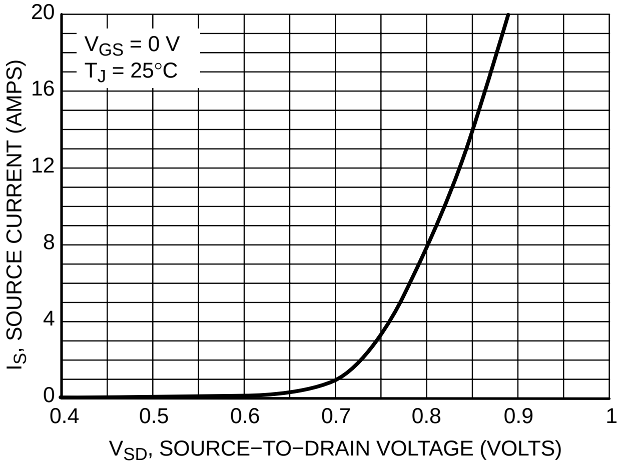


Figure 16. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain−to−source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance − General Data and Its Use.”

Switching between the off−state and the on−state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A power MOSFET designated E−FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non−linearly with an increase of peak current in avalanche and peak junction temperature.

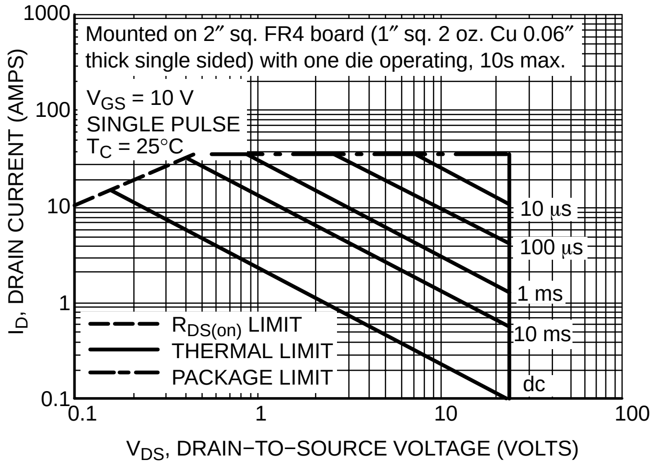


Figure 17. Maximum Rated Forward Biased Safe Operating Area

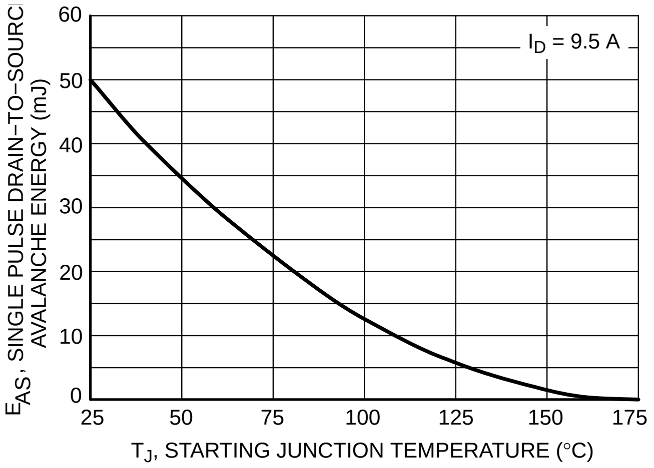
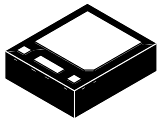


Figure 18. Maximum Avalanche Energy versus Starting Junction Temperature

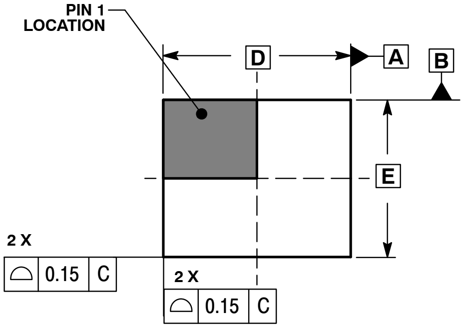
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

PLLP4
CASE 508AA
ISSUE O

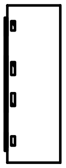
DATE 21 JUL 2004

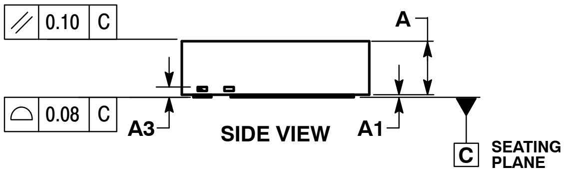


SCALE 1:1

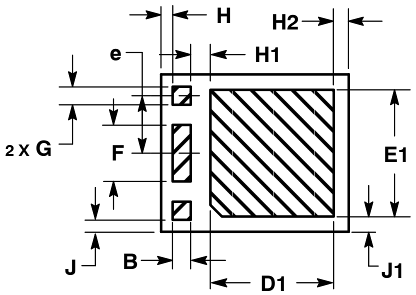


TOP VIEW





SIDE VIEW

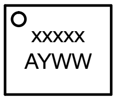


BOTTOM VIEW

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. TOLERANCES: ±0.10 MM.

	MILLIMETERS	
DIM	**MIN**	**MAX**
A	1.750	1.950
A1	0.000	0.050
A3	0.254 REF	
B	0.500	0.700
D	6.200 BSC	
D1	3.979	4.179
E	5.200 BSC	
E1	4.087	4.287
e	1.905 BSC	
F	1.860	1.880
G	0.500	0.700
H	0.379 REF	
H1	0.635 REF	
H2	0.507 REF	
J	0.404 REF	
J1	0.507 REF	

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	98AON19199D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**PLLP4, 6.2X5.2X1.85 MM PITCH**	**PAGE 1 OF 1**

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