Intelligent Power Module (IPM)
600 V, 8 A

NFAQ0860L36T

The NFAQ0860L36T is a fully−integrated inverter power stage consisting of a high−voltage driver, six IGBT's and a thermistor, suitable for driving permanent magnet synchronous motors (PMSM), brushless−DC (BLDC) motors and AC asynchronous motors. The IGBT's are configured in a 3−phase bridge with separate emitter connections for the lower legs for maximum flexibility in the choice of control algorithm. The power stage has a full range of protection functions including cross−conduction protection, external shutdown and under−voltage lockout functions. An internal comparator and reference connected to the over−current protection circuit allows the designer to set the over−current protection level.

Features

- Three−phase 8 A / 600 V IGBT Module with Integrated Drivers
- Compact 29.6 mm x 18.2 mm Dual In−Line Package
- Built−in Under Voltage Protection
- Cross−conduction Protection
- ITRIP Input to Shut Down All IGBT's
- Integrated Bootstrap Diodes and Resistors
- Thermistor for Substrate Temperature Measurement
- Shut Down Pin
- UL1557 Certification (File Number: E339285)

Typical Applications

- Industrial Pumps
- Industrial Fans
- Industrial Automation
- Home Appliances

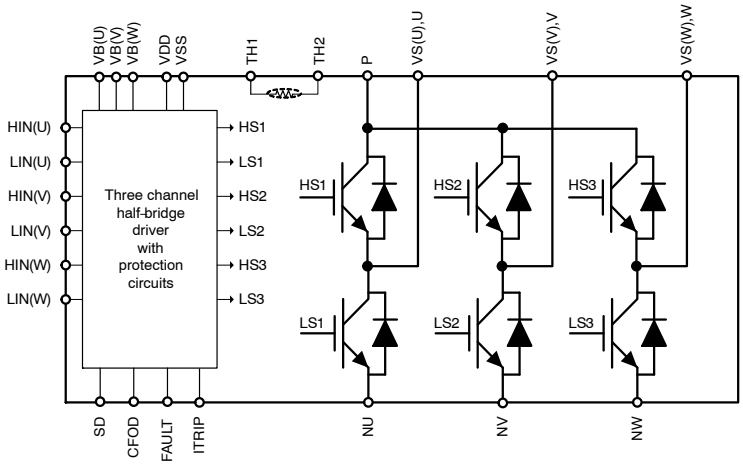

Figure 1. Function Diagram

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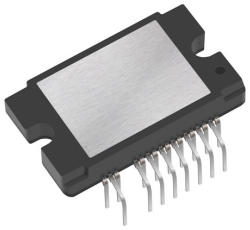
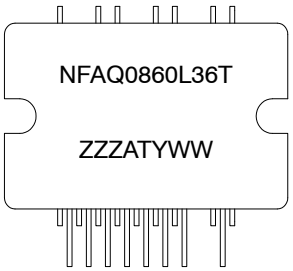


DIP38 29.6x18.2
CASE 125BS

MARKING DIAGRAM



NFAQ0860L36T	= Specific Device Code
ZZZ	= Assembly Lot Code
A	= Assembly Location
T	= Test Location
Y	= Year
WW	= Work Week

Device marking is on package top side

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
NFAQ0860L36T	DIP38 (Pb-Free)	400 / Box

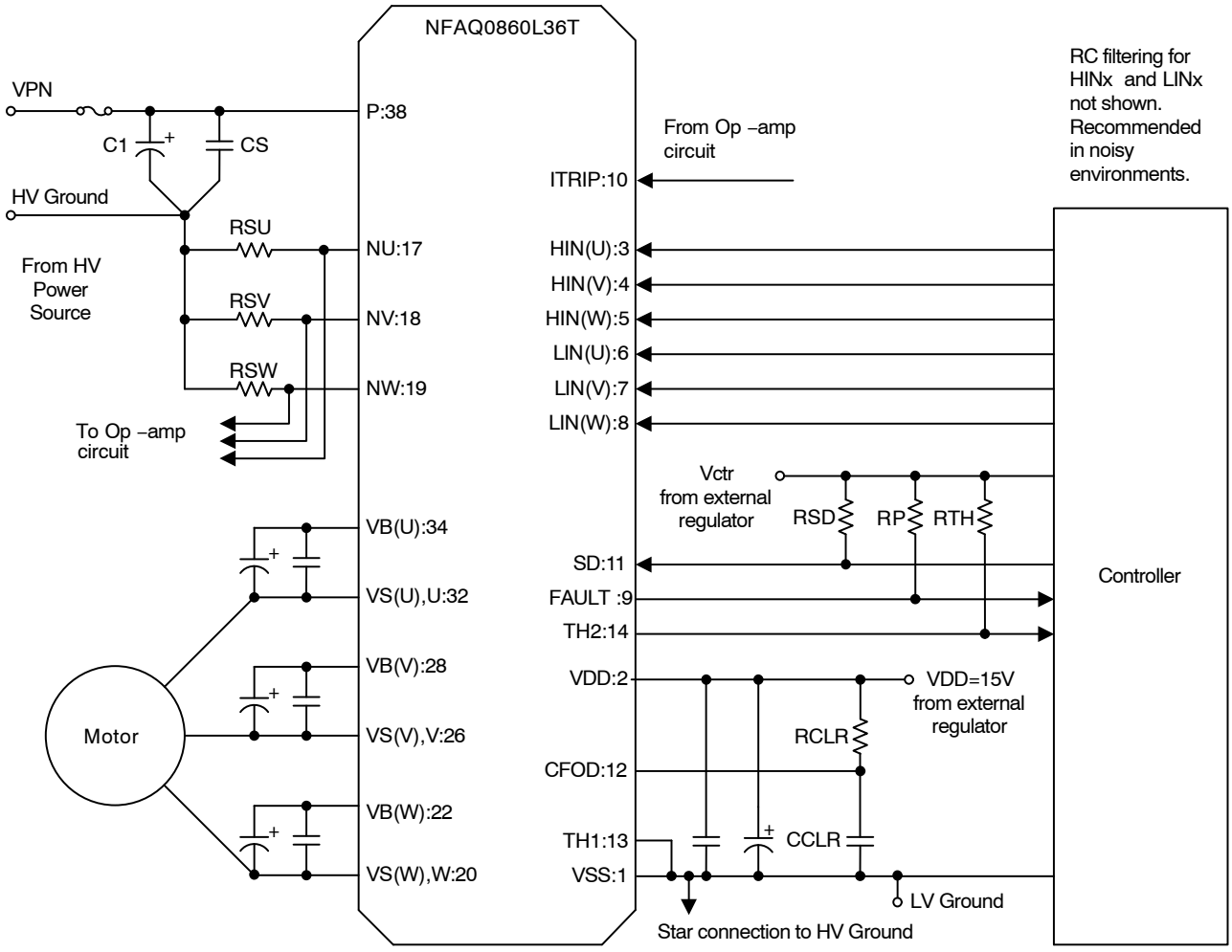


Figure 2. Application Schematic

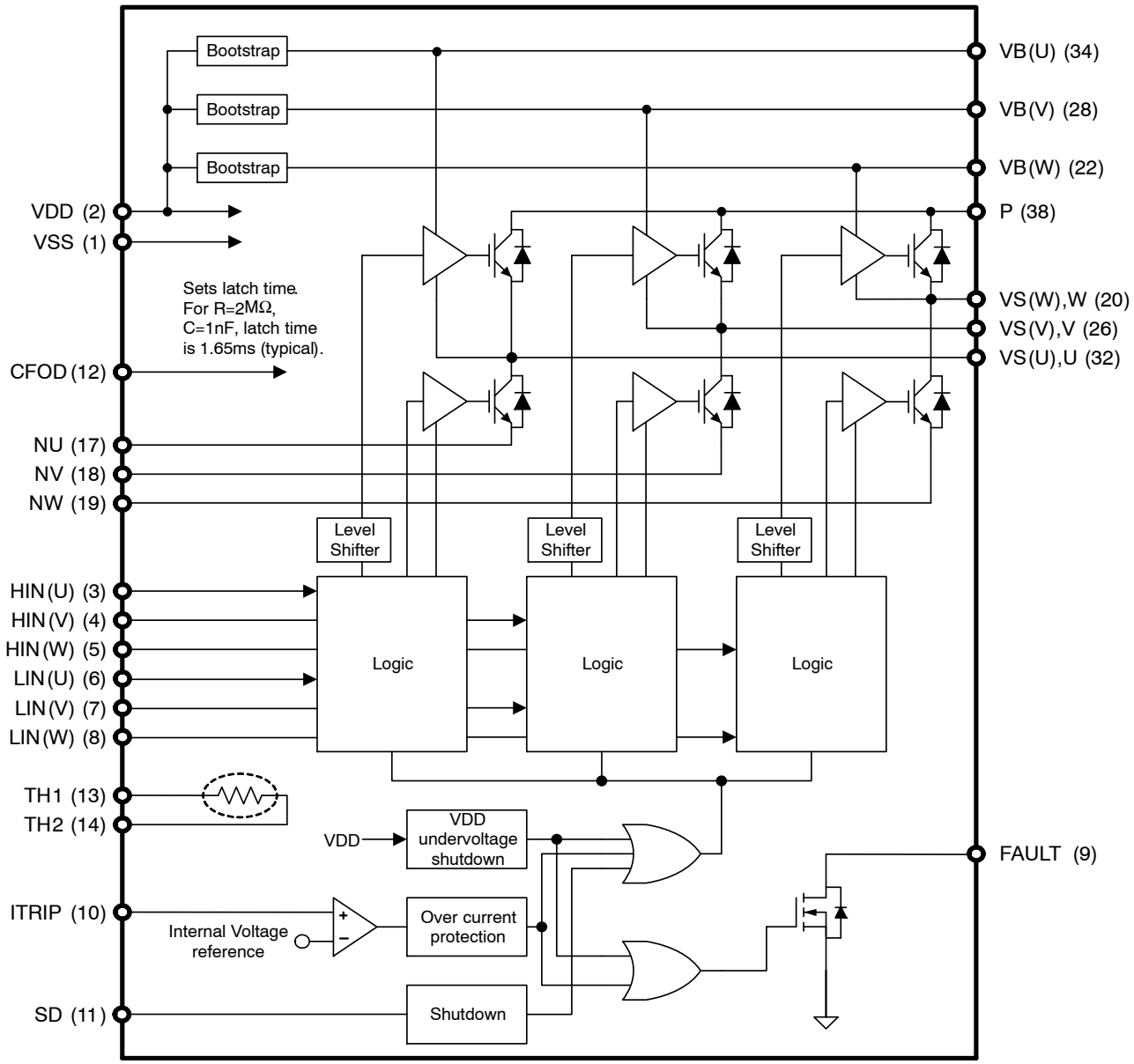


Figure 3. Simplified Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	VSS	Low−Side Common Supply Ground
2	VDD	Low−Side Bias Voltage for IC and IGBTs Driving
3	HIN(U)	Signal Input for High−Side U Phase
4	HIN(V)	Signal Input for High−Side V Phase
5	HIN(W)	Signal Input for High−Side W Phase
6	LIN(U)	Signal Input for Low−Side U Phase
7	LIN(V)	Signal Input for Low−Side V Phase
8	LIN(W)	Signal Input for Low−Side W Phase
9	FAULT	Fault output
10	ITRIP	Input for Over Current Protection
11	SD	Shut Down Input
12	CFOD	Capacitor and Resistor for Fault Output Duration Selection
13	TH1	Thermistor Bias Voltage
14	TH2	Series Resistor for Thermistor
17	NU	Negative DC−Link Input for U Phase
18	NV	Negative DC−Link Input for V Phase
19	NW	Negative DC−Link Input for W Phase
20	VS(W), W	High−Side Bias Voltage GND for W phase IGBT Driving, Output for W Phase
22	VB(W)	High−Side Bias Voltage for W phase IGBT Driving
26	VS(V), V	High−Side Bias Voltage GND for V phase IGBT Driving, Output for V Phase
28	VB(V)	High−Side Bias Voltage for V phase IGBT Driving
32	VS(U), U	High−Side Bias Voltage GND for U phase IGBT Driving, Output for U Phase
34	VB(U)	High−Side Bias Voltage for U phase IGBT Driving
38	P	Positive DC−Link Input

NOTE: Pins 15, 16, 21, 23, 24, 25, 27, 29, 30, 31, 33, 35, 36 and 37 are not present

Table 2. ABSOLUTE MAXIMUM RATINGS at T_C = 25°C (Note 1)

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	VPN	P−NU,NV,NW, VPN (surge) < 500 V (Note 2)	450	V
Collector − Emitter Voltage	VCES	P-U,V,W; U-NU; V-NV; W-NW	600	V
Each IGBT Collector Current	IC	P,U,V,W,NU,NV,NW terminal current	±8	A
		P,U,V,W,NU,NV,NW terminal current, Tc = 100°C	±4	A
Each IGBT Collector Current (Peak)	ICp	Tc = 25°C, Under 1 ms Pulse Width	±16	A
Corrector Dissipation	Pc	Tc = 25°C, Per One Chip	32	W
High−Side Control Bias voltage	VBS	VB(U)−VS(U), VB(V)−VS(V), VB(W)−VS(W) (Note 3)	−0.3 to +20.0	V
Control Supply Voltage	VDD	VDD−VSS	−0.3 to +20.0	V
Input Signal Voltage	VIN	HIN(U), HIN(V), HIN(W), LIN(U), LIN(V), LIN(W) − VSS	−0.3 to V_{DD}	V
FAULT Terminal Voltage	VFAULT	FAULT−VSS	−0.3 to V_{DD}	V
CFOD Terminal Voltage	VCFOD	CFOD−VSS	−0.3 to V_{DD}	V
SD Terminal Voltage	VSD	SD−VSS	−0.3 to V_{DD}	V
Current Sensing Input Voltage	VITRIP	ITRIP−VSS	−0.3 to +10.0	V
Operating Junction Temperature	Tj		150	°C
Storage Temperature	Tstg		−40 to +125	°C
Module Case Operation Temperature	Tc		−40 to +125	°C
Tightening Torque	MT	Case mounting screws	0.6	Nm
Isolation Voltage	Viso	50 Hz sine wave AC 1 minute (Note 4)	2000	Vrms

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters
2. This surge voltage developed by the switching operation due to the wiring inductance between P and NU, NV, NW terminal.
3. VBS=VB(U)−VS(U), VB(V)−VS(V), VB(W)−VS(W)
4. Test conditions : AC2500V, 1 s

Table 3. RECOMMENDED OPERATING RANGES

Rating	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	VPN	P − NU, NV, NW	0	280	450	V
High−Side Control Bias Voltage	VBS	VB(U) − VS(U), VB(V) − VS(V), VB(W) − VS(W)	13.0	15	17.5	V
Control Supply Voltage	VDD	VDD − VSS	14.0	15	16.5	V
ON−state Input Voltage	VIN(ON)	HIN(U), HIN(V), HIN(W), LIN(U), LIN(V), LIN(W) − VSS	3.0	−	5.0	V
OFF−state Input Voltage	VIN(OFF)		0	−	0.3	V
PWM Frequency	fPWM		1	−	20	kHz
Dead Time	DT	Turn−off to Turn−on (external)	1	−	−	μs
Allowable Input Pulse Width	PWIN	ON and OFF	1	−	−	μs
Tightening Torque		‘M3’ Type Screw	0.4	−	0.6	Nm

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ELECTRICAL CHARACTERISTICS at T_C = 25 °C, V_{BIAS} (VBS, VDD) = 15 V unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Power Output Section						
Collector−Emitter Leakage Current	V_{CE} = 600 V	ICES	–	–	100	μA
Collector−Emitter Saturation Voltage	IN = 5 V, IC = 8 A, Tj = 25 °C	VCE(sat)	–	2.4	3.0	V
	IN = 5 V, IC = 4 A, Tj = 100 °C		–	1.9	–	V
FWDi Forward Voltage	IN = 0 V, IC = −8 A, Tj = 25 °C	VF	–	2.1	2.7	V
	IN = 0 V, IC = −4 A, Tj = 100 °C		–	1.6	–	V
Junction to Case Thermal Resistance	Inverter IGBT Part (per 1/6 Module)	Rth(j−c)Q	–	–	3.9	°C/W
	Inverter FRD Part (per 1/6 Module)	Rth(j−c)F	–	–	7.3	°C/W
Switching Character						
Switching Time	IC = 8 A, VPN = 300 V, Tj = 25°C, Inductive Switching	t_{ON}	–	0.4	1.1	μs
		t_{OFF}	–	0.4	1.1	μs
Turn−on Switching Loss	IC = 8 A, VPN = 300 V, Tj = 25°C	E_{ON}	–	190	–	μJ
Turn−off Switching Loss		E_{OFF}	–	90	–	μJ
Total Switching Loss		E_{TOT}	–	280	–	μJ
Turn−on Switching Loss	IC = 4 A, VPN = 300 V, Tj = 100°C	E_{ON}	–	100	–	μJ
Turn−off Switching Loss		E_{OFF}	–	50	–	μJ
Total Switching Loss		E_{TOT}	–	150	–	μJ
Diode Reverse Recovery Energy	IC = 4 A, VPN = 300 V, Tj = 100°C, (di/dt set by internal driver)	E_{REC}	–	25	–	μJ
Diode Reverse Recovery Time		t_{RR}	–	140	–	ns
Reverse Bias Safe Operating Area	IC = 16 A, V_{CE} = 450 V	RBSOA	Full Square			
Short Circuit Safe Operating Area	V_{CE} = 400 V, Tj = 100°C	SCSOA	4	–	–	μs
Driver Section						
Quiescent VBS Supply Current	VBS = 15 V, HIN = 0 V, per driver	IQBS	–	0.07	0.4	mA
Quiescent VDD Supply Current	VDD = 15 V, LIN = 0 V, VDD−VSS	IQDD	–	0.95	3.0	mA
ON Threshold Voltage	HIN(U), HIN(V), HIN(W), LIN(U), LIN(V), LIN(W) − VSS	VIN(ON)	–	–	2.5	V
OFF Threshold Voltage		VIN(OFF)	0.8	–	–	V
Logic 1 Input Current	VIN = +3.3 V	IIN+	–	660	900	μA
Logic 0 Input Current	VIN = 0 V	IIN−	–	–	3	μA
Bootstrap ON Resistance	IB = 1 mA	RB	–	500	–	Ω
FAULT Terminal Sink Current	FAULT: ON / VFAULT = 0.1 V	IoSD	–	2	–	mA
Fault−Output Pulse Width	FAULT−VSS	tFOD	1.1	1.65	2.2	ms
CFOD Threshold	CFOD−VSS	VCFOD	–	8	–	V
Shut Down Threshold	SD−VSS	VSD+	–	–	2.5	V
		VSD−	0.8	–	–	V
ITRIP Trip Level	ITRIP−VSS	VITRIP	0.44	0.49	0.54	V
ITRIP to Shutdown Propagation Delay		tITRIP	–	1.1	–	μs
ITRIP Blanking Time		tITRIPBL	250	350	–	ns
High−Side Control Bias Voltage Under−Voltage Protection	Reset Level	UVBSR	10.3	11.1	11.9	V
	Detection Level	UVBSD	10.1	10.9	11.7	V
	Hysteresis	UVBSH	–	0.2	–	V
Supply Voltage Under−Voltage Protection	Reset Level	UVDDR	10.3	11.1	11.7	V
	Detection Level	UVDDD	10.1	10.9	11.5	V
	Hysteresis	UVDDH	–	0.2	–	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

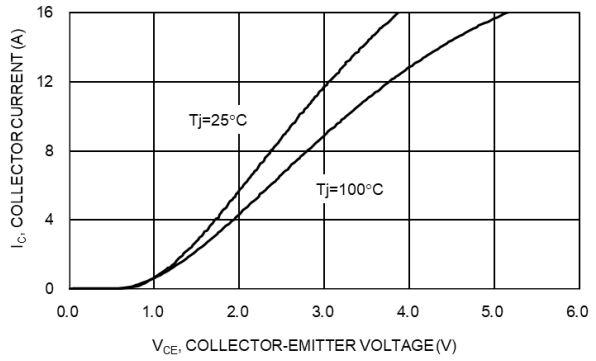


Figure 4. V_{CE} versus I_C for Different Temperatures (V_{DD} = 15 V)

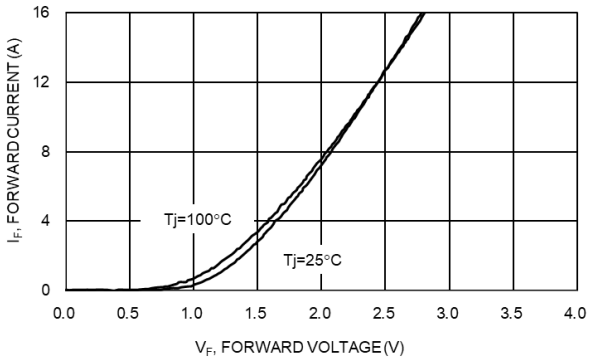


Figure 5. V_F versus I_F for Different Temperatures

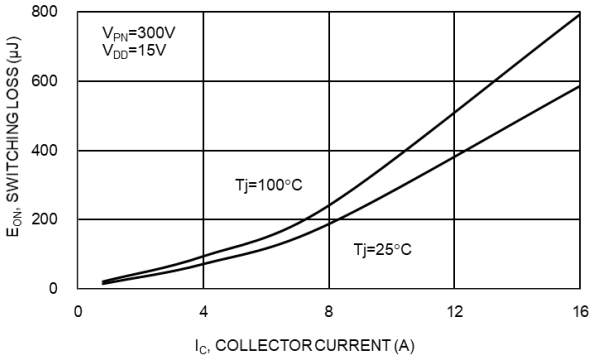


Figure 6. E_{ON} versus I_C for Different Temperatures

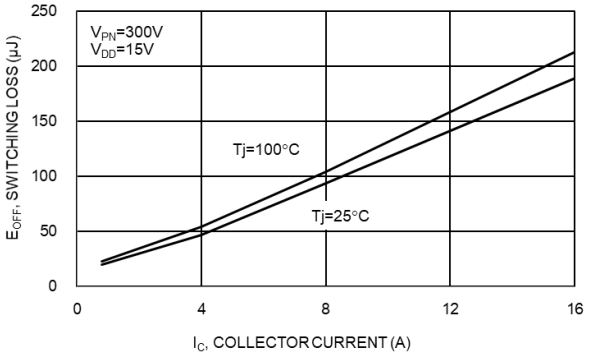


Figure 7. E_{OFF} versus I_C for Different Temperatures

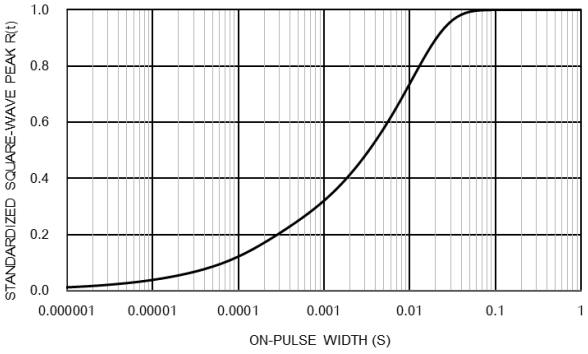


Figure 8. Thermal Impedance Plot (IGBT)

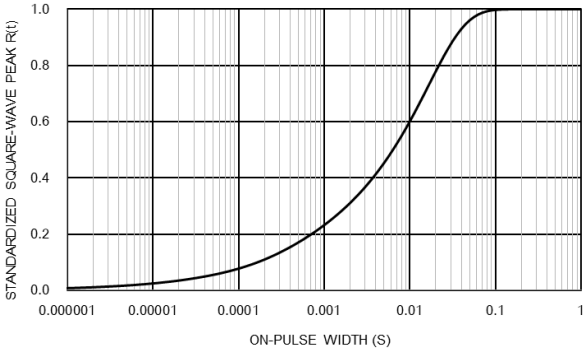


Figure 9. Thermal Impedance Plot (FRD)

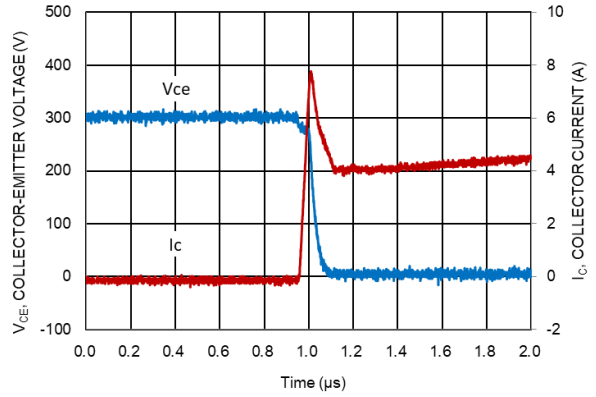


Figure 10. Turn−on Waveform Tj = 100°C, V_{CC} = 300 V

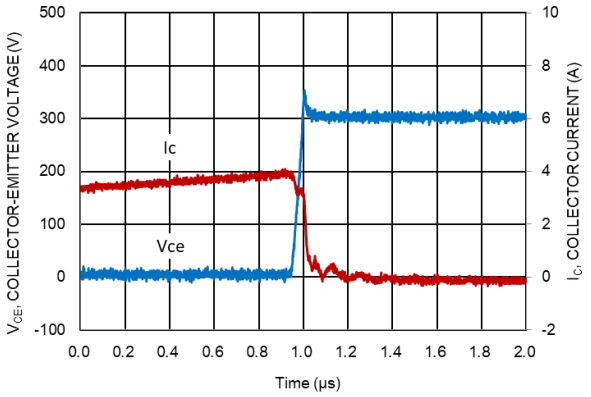
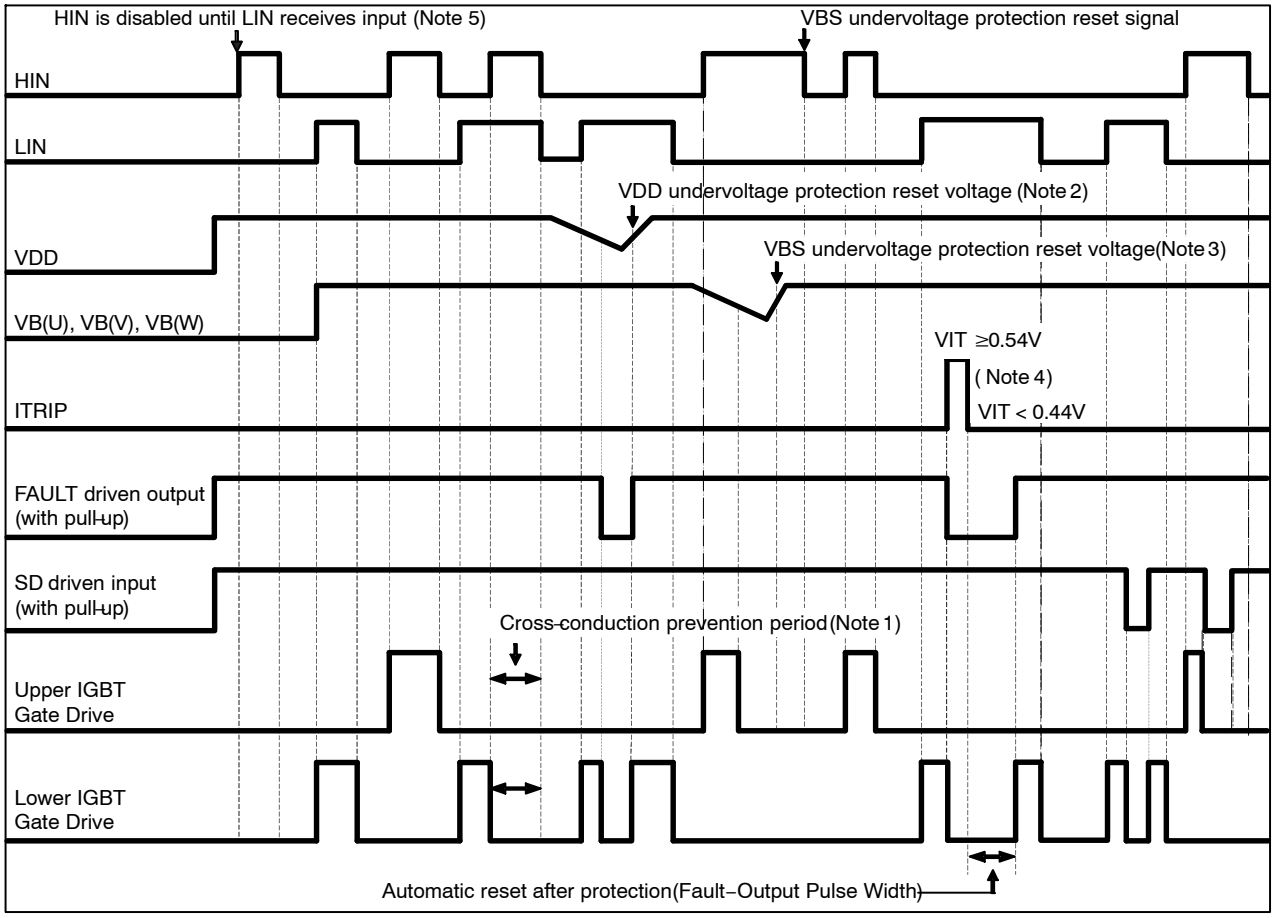


Figure 11. Turn−off Waveform Tj = 100°C, V_{CC} = 300 V

APPLICATIONS INFORMATION

Input / Output Timing Chart



NOTES:

1. This section of the timing diagram shows the effect of cross−conduction prevention.
2. This section of the timing diagram shows that when the voltage on VDD decreases sufficiently all gate output signals will go low, switching off all six IGBTs. When the voltage on VDD rises sufficiently, normal operation will resume.
3. This section shows that when the bootstrap voltage on VB(U) (VB(V), VB(W)) drops, the corresponding high side output U (V, W) is switched off. When the voltage on VB(U) (VB(V), VB(W)) rises sufficiently, normal operation will resume.
4. This section shows that when the voltage on ITRIP exceeds the threshold, all IGBTs are turned off. Normal operation resumes later after the over−current condition is removed.
5. After VDD has risen above the threshold to enable normal operation, the driver waits to receive an input signal on the LIN input before enabling the driver for the HIN signal.

Figure 12. Input / Output Timing Chart

Table 5. INPUT / OUTPUT LOGIC TABLE

INPUT				OUTPUT			
HIN	**LIN**	**ITRIP**	**SD**	**High side IGBT**	**Low side IGBT**	**U,V,W**	**FAULT**
H	L	L	H	ON (Note 5)	OFF	P	OFF
L	H	L	H	OFF	ON	NU,NV,NW	OFF
L	L	L	H	OFF	OFF	High Impedance	OFF
H	H	L	H	OFF	OFF	High Impedance	OFF
X	X	H	X	OFF	OFF	High Impedance	ON
X	X	L	L	OFF	OFF	High Impedance	OFF

Table 6. THERMISTOR CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Resistance	R_{25}	Tth = 25°C	99	100	101	kΩ
	R_{100}	Tth = 100°C	5.18	5.38	5.60	kΩ
B−Constant (25 to 50°C)	B		4208	4250	4293	K
Temperature Range			−40	−	+125	°C

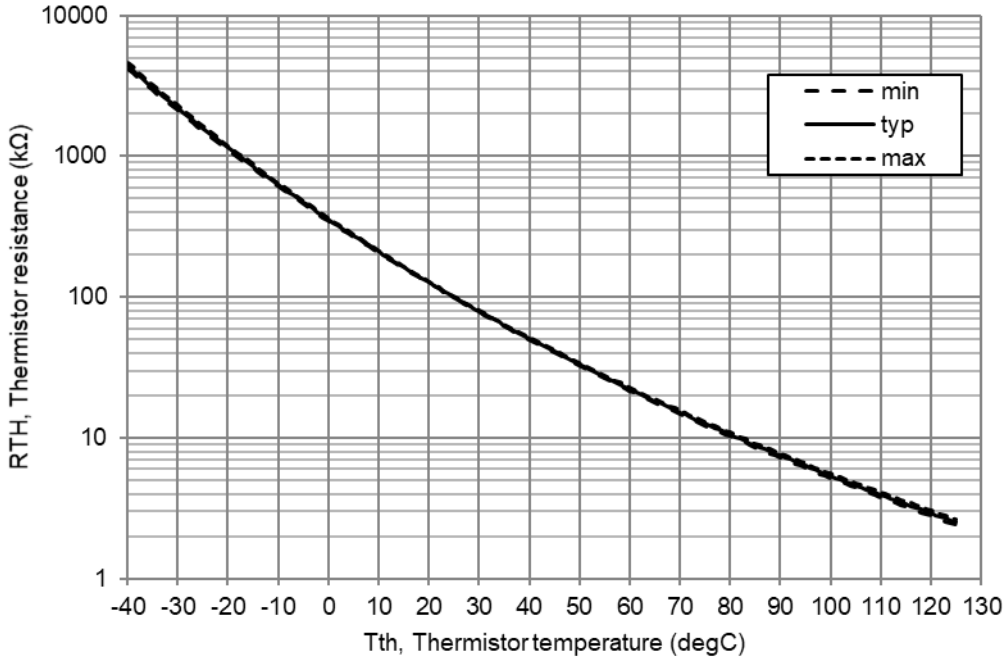


Figure 13. Thermistor Resistance versus Thermistor Temperature

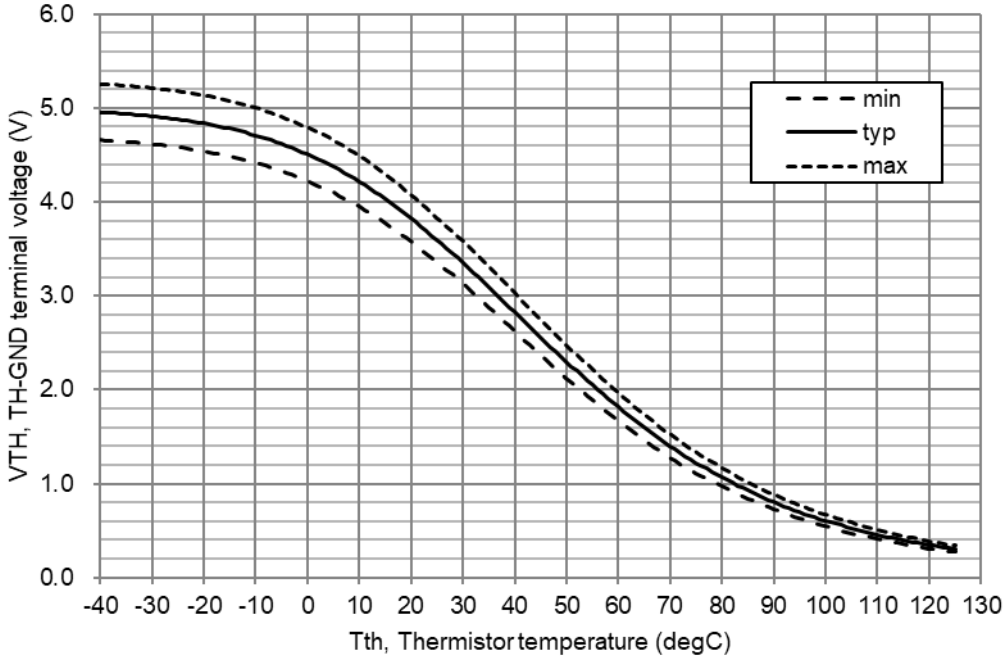


Figure 14. Thermistor Voltage versus Thermistor Temperature
Conditions: RTH = 39 kΩ, Pull−up Voltage 5.0 V (see Figure 2)

FAULT Pin

The FAULT output is an open drain output requiring a pull−up resistor. If the pull−up voltage is 5 V, use a pull−up resistor with a value of 6.8 kΩ or higher. If the pull−up voltage is 15 V, use a pull−up resistor with a value of 20 kΩ or higher. The FAULT output is triggered if there is a VDD undervoltage or an overcurrent condition.

Under−voltage Protection

If VDD goes below the VDD supply under−voltage lockout falling threshold, the FAULT output is switched on. The FAULT output stays on until VDD rises above the VDD supply under−voltage lockout rising threshold. After VDD has risen above the threshold to enable normal operation, the driver waits to receive an input signal on the LIN input before enabling the driver for the HIN signal.

Overcurrent Protection

An over−current condition is detected if the voltage on the ITRIP pin is larger than the reference voltage. There is a blanking time of typically 350 ns to improve noise immunity. After a shutdown propagation delay of typically 1.1 μs, the FAULT output is switched on. The FAULT output is held on for a time determined by the resistor and capacitor connected to the CFOD pin. If RCLR = 2 MΩ and CCLR = 1 nF, the FAULT output is switched on for 1.65 ms (typ.) because the FAULT pin goes back to high impedance when CFOD is higher than 8 V (typ.).

The over−current protection threshold should be set to be equal or lower to 2 times the module rated current (Io).

An additional fuse is recommended to protect against system level or abnormal over−current fault conditions.

Capacitors on High Voltage and VDD Supplies

Both the high voltage and VDD supplies require an electrolytic capacitor and an additional high frequency capacitor. The recommended value of the high frequency capacitor is between 100 nF and 10 μF.

SD Pin

The SD terminal pin is used to enable or shut down the built−in driver. If the voltage on the SD pin rises above the VSD+ voltage, the output drivers are enabled. If the voltage on the SD pin falls below the VSD− voltage, the drivers are disabled.

Minimum Input Pulse Width

When input pulse width is less than 1 μs, an output may not react to the pulse. (Both ON signal and OFF signal)

Calculation of Bootstrap Capacitor Value

The bootstrap capacitor value CB is calculated using the following approach. The following parameters influence the choice of bootstrap capacitor:

- VBS: Bootstrap power supply.
  15 V is recommended.
- QG: Total gate charge of IGBT at VBS = 15 V.
  8 nC
- UVLO: Falling threshold for UVLO.
  Specified as 12 V.
- IDMAX: High side drive power dissipation.
  Specified as 0.4 mA
- TONMAX: Maximum ON pulse width of high side IGBT.

Capacitance calculation formula:

$$CB = (QG + IDMAX * TONMAX) / (VBS - UVLO)$$

CB is recommended to be approximately 3 times the value calculated above. The recommended value of CB is in the range of 1 to 47 μF, however, the value needs to be verified prior to production. When not using the bootstrap circuit, each high side driver power supply requires an external independent power supply.

The internal bootstrap circuit uses a MOSFET. The turn on time of this MOSFET is synchronized with the turn on of the low side IGBT. The bootstrap capacitor is charged by turning on the low side IGBT.

If the low side IGBT is held on for a long period of time (more than one second for example), the bootstrap voltage on the high side MOSFET will slowly discharge.

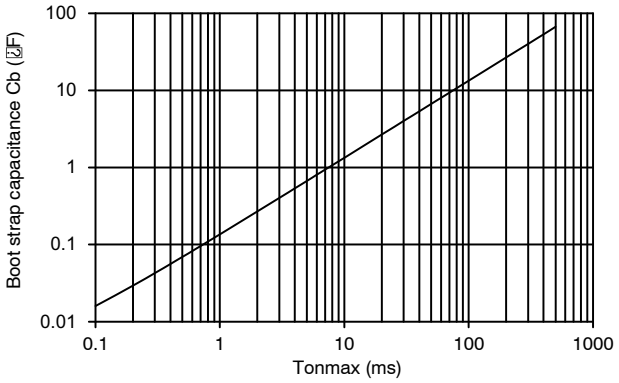


Figure 15. Bootstrap Capacitance versus Tonmax

TEST CIRCUITS

- ICES

	U+	V+	W+	U−	V−	W−
A	38	38	38	32	26	20
B	32	26	20	17	18	19

U+, V+, W+ : High side phase
U−, V−, W− : Low side phase

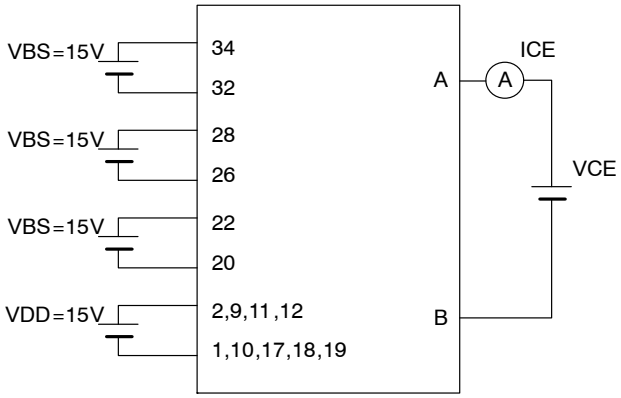


Figure 16. Test Circuit for I_{CE}

- VCE(sat) (Test by pulse)

	U+	V+	W+	U−	V−	W−
A	38	38	38	32	26	20
B	32	26	20	17	18	19
C	3	4	5	6	7	8

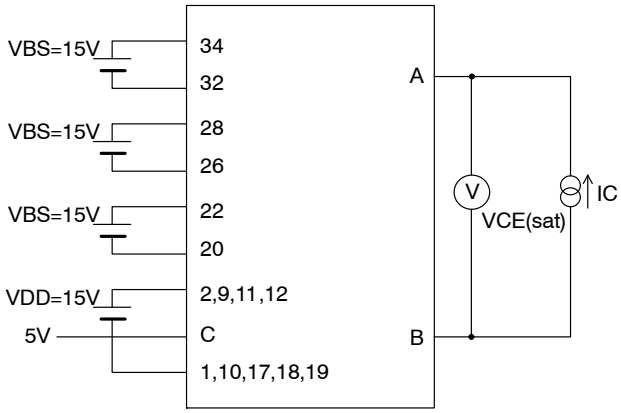


Figure 17. Test Circuit for $V_{CE(SAT)}$

- VF (Test by pulse)

	U+	V+	W+	U−	V−	W−
A	38	38	38	32	26	20
B	32	26	20	17	18	19

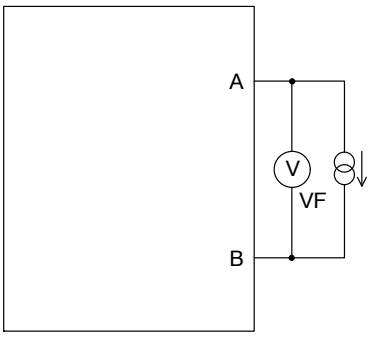


Figure 18. Test Circuit for V_F

- RB (Test by pulse)

	U+	V+	W+
A	2	2	2
B	34	28	22
C	6	7	8

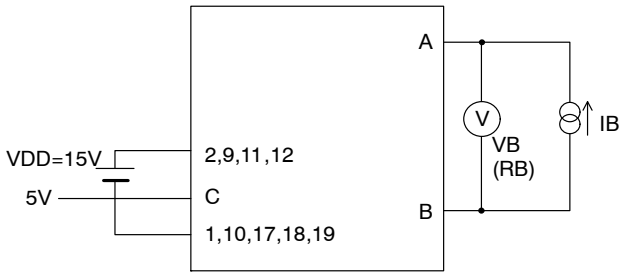


Figure 19. Test Circuit for RB

- IQBS, IQDD

	VBS U+	VBS V+	VBS W+	V_{DD}
A	34	28	22	2
B	32	26	20	1

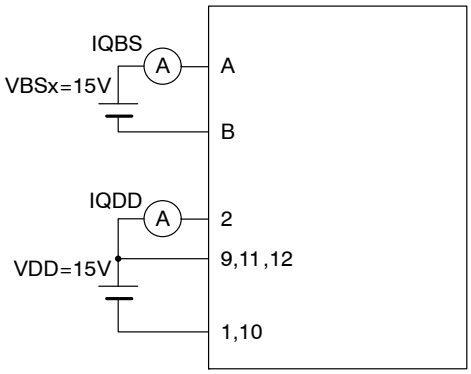
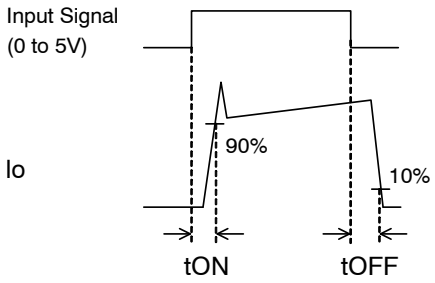


Figure 20. Test Circuit for I_D

- Switching Time (The circuit is a representative example of the Inverter Low side U phase.)



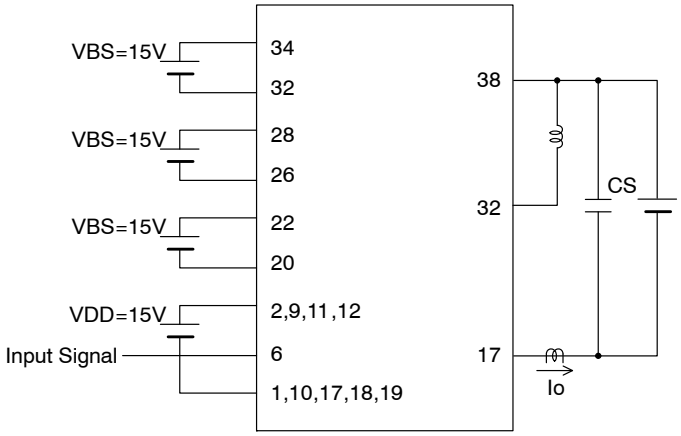
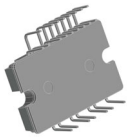


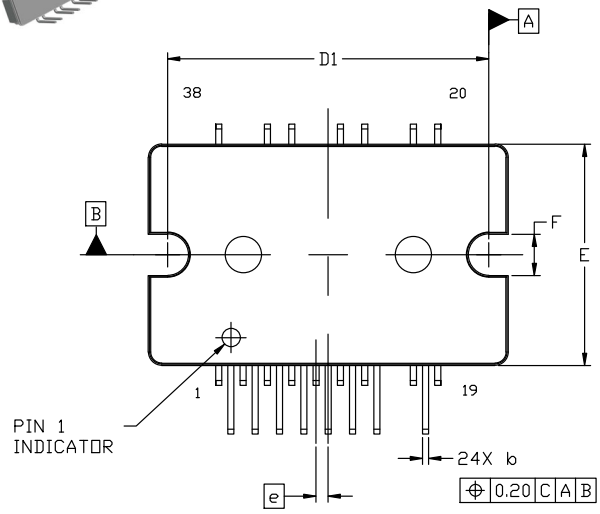
Figure 21. Test Circuit for Switching Time

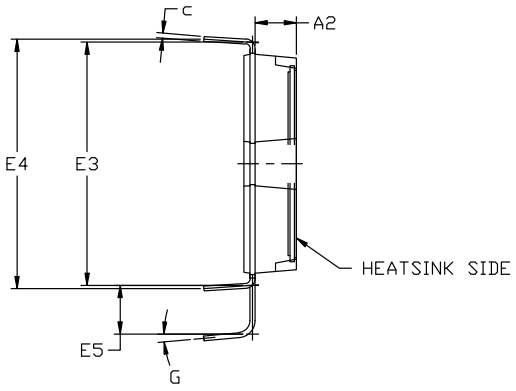
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

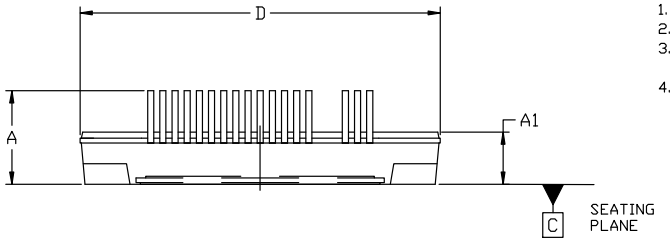


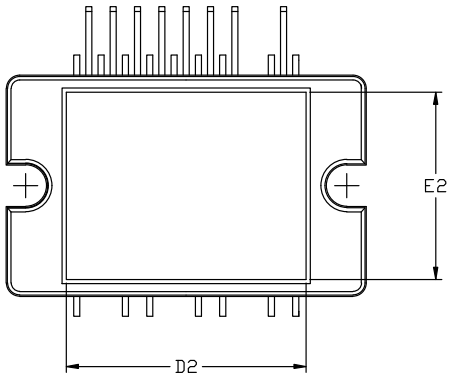
DIP38, 29.60x18.20x7.70, 1.00P (EP−4)
CASE 125BS
ISSUE B

DATE 26 APR 2023









NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO THE PLATED LEAD AND IS MEASURED BETWEEN 0.10 AND 0.25 FROM THE LEAD TIP.
4. PACKAGE IS MISSING PINS: 15, 16, 21, 23, 24, 25, 27, 29, 30, 31, 33, 35, 36, AND 37.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	7.20	7.70	8.20
A1	4.00	4.30	4.60
A2	3.10	3.40	3.70
b	0.40	0.50	0.60
c	0.35	0.40	0.60
D	29.10	29.60	30.10
D1	26.30	26.40	26.50
D2	19.20	19.70	20.20
E	17.70	18.20	18.70
E2	14.90	15.40	15.90
E3	19.50	20.00	20.50
E4	20.00	20.50	21.00
E5	3.50	4.00	4.50
e	1.00 BSC		
F	2.90	3.40	3.90
G	4°	5°	6°

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
ZZZ = Lot ID
AT = Assembly & Test Location
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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