

# Intelligent Power Module (IPM)

650 V, 30 A

## NFAM3065L4B

### General Description

The NFAM3065L4B is a fully-integrated inverter power module consisting of an independent High side gate driver, LVIC, six IGBT's and a temperature sensor (VTS), suitable for driving permanent magnet synchronous (PMSM) motors, brushless DC (BLDC) motors and AC asynchronous motors. The IGBT's are configured in a three-phase bridge with separate emitter connections for the lower legs for maximum flexibility in the choice of control algorithm.

The power stage has under voltage lockout protection (UVP). Internal boost diodes are provided for high side gate boost drive.

### Features

- Three-phase 650 V, 30 A IGBT Module with Independent Drivers
- Active Logic Interface
- Built-in Undervoltage Protection (UVP)
- Integrated Bootstrap Diodes and Resistors
- Separate Low-side IGBT Emitter Connections for Individual Current Sensing of Each Phase
- Temperature Sensor (VTS)
- UL1557 Certified (File No.339285)
- This Device is Pb-Free and RoHS Compliant

### Typical Applications

- Industrial Drives
- Industrial Pumps
- Industrial Fans
- Industrial Automation

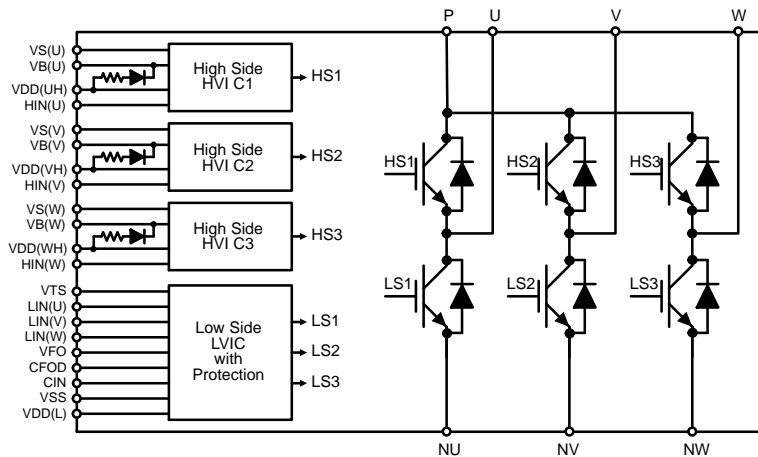
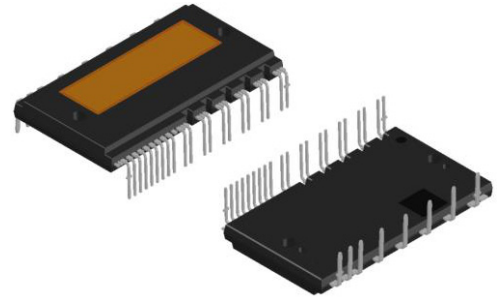


Figure 1. Application Schematic



DIP39 54.5 x 31.0  
CASE MODGX

### MARKING DIAGRAM



Device marking is on package top side

NFAM3065L4B = Specific Device Code  
ZZZ = Assembly Lot Code  
A = Assembly Location  
T = Test Location  
Y = Year  
WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
NFAM3065L4B	DIP39 54.5 x 31.0 (Pb-Free)	90 / Box

# NFAM3065L4B

## APPLICATION SCHEMATIC

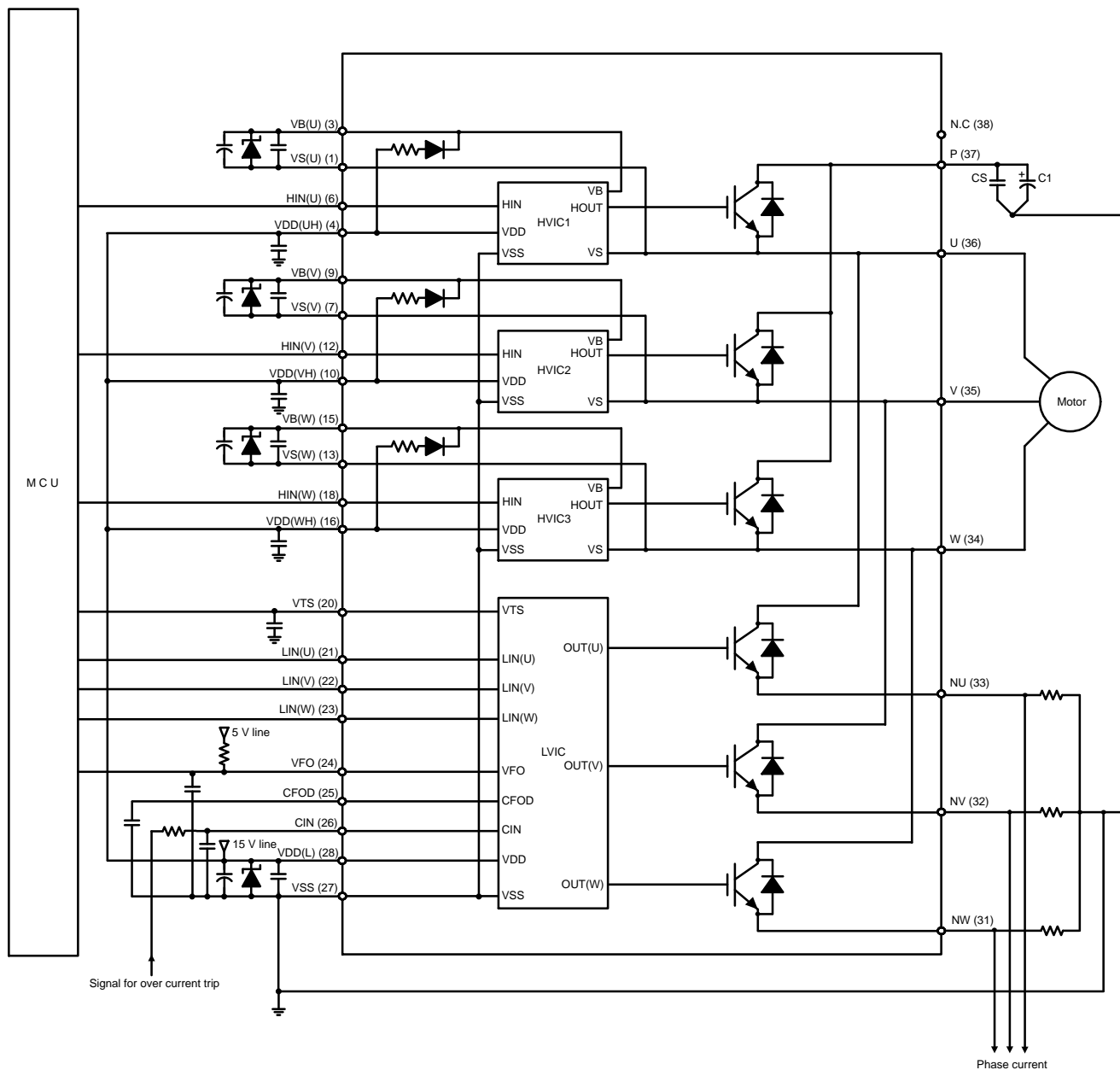


Figure 2. Application Schematic – Adjustable Option

# NFAM3065L4B

## BLOCK DIAGRAM

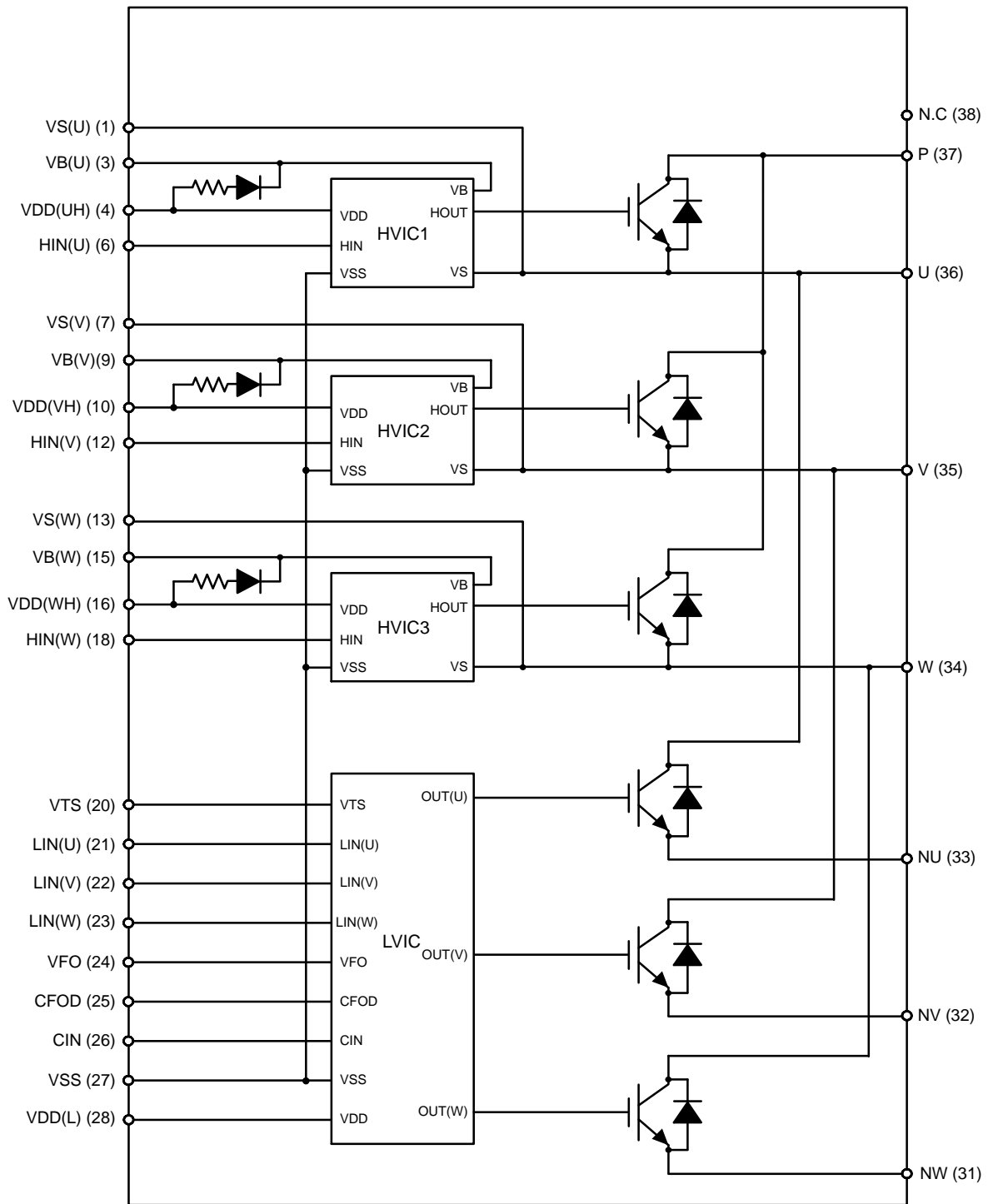


Figure 3. Equivalent Block Diagram

# NFAM3065L4B

## PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	VS(U)	High-Side Bias Voltage GND for U phase IGBT Driving
(2)	-	Dummy
3	VB(U)	High-Side Bias Voltage for U phase IGBT Driving
4	VDD(UH)	High-Side Bias Voltage for U phase IC
(5)	-	Dummy
6	HIN(U)	Signal Input for High-Side U Phase
7	VS(V)	High-Side Bias Voltage GND for V phase IGBT Driving
(8)	-	Dummy
9	VB(V)	High-Side Bias Voltage for V phase IGBT Driving
10	VDD(VH)	High-Side Bias Voltage for V phase IC
(11)	-	Dummy
12	HIN(V)	Signal Input for High-Side V Phase
13	VS(W)	High-Side Bias Voltage GND for W phase IGBT Driving
(14)	-	Dummy
15	VB(W)	High-Side Bias Voltage for W phase IGBT Driving
16	VDD(WH)	High-Side Bias Voltage for W phase IC
(17)	-	Dummy
18	HIN(W)	Signal Input for High-Side W Phase
(19)	-	Dummy
20	VTS	Voltage Output for LVIC Temperature Sensing Unit
21	LIN(U)	Signal Input for Low-Side U Phase
22	LIN(V)	Signal Input for Low-Side V Phase
23	LIN(W)	Signal Input for Low-Side W Phase
24	VFO	Fault Output
25	CFOD	Capacitor for Fault Output Duration Selection
26	CIN	Input for Current Protection
27	VSS	Low-Side Common Supply Ground
28	VDD(L)	Low-Side Bias Voltage for IC and IGBTs Driving
(29)	-	Dummy
(30)	-	Dummy
31	NW	Negative DC-Link Input for U Phase
32	NV	Negative DC-Link Input for V Phase
33	NU	Negative DC-Link Input for W Phase
34	W	Output for U Phase
35	V	Output for V Phase
36	U	Output for W Phase
37	P	Positive DC-Link Input
38	N.C	No Connection
(39)	-	Dummy

1. Pins of () are the dummy for internal connection. These pins should be no connection.

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## ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25°C) (Note 2)

Symbol	Rating	Conditions	Value	Unit
VPN	Supply Voltage	P–NU, NV, NW	450	V
VPN(surge)	Supply Voltage (Surge)	P–NU, NV, NW (Note 3)	550	V
VPN(PROT)	Self Protection Supply Voltage Limit (Short-Circuit Protection Capability)	VDD = VBS = 13.5 V ~ 16.5 V, T <sub>j</sub> = 150°C, VCES < 650 V, Non-Repetitive, < 2 μs	400	V
Vces	Collector–emitter voltage		650	V
VRRM	Maximum Repetitive Revers Voltage		650	V
±Ic	Each IGBT Collector Current		±30	A
±Icp	Each IGBT Collector Current (Peak)	Under 1 ms Pulse Width	±60	A
VDD	Control Supply Voltage	VDD(UH,VH,WH), VDD(L)–VSS	–0.3 to 20	V
VBS	High–Side Control Bias Voltage	VB(U)–VS(U), VB(V)–VS(V), VB(W)–VS(W)	–0.3 to 20	V
VIN	Input Signal Voltage	HIN(U), HIN(V), HIN(W), LIN(U), LIN(V), LIN(W)–VSS	–0.3 to VDD	V
VFO	Fault Output Supply Voltage	VFO–VSS	–0.3 to VDD	V
IFO	Fault Output Current	Sink Current at VFO pin	2	mA
VCIN	Current Sensing Input Voltage	CIN–VSS	–0.3 to VDD	V
Pc	Corrector Dissipation	Per One Chip	113	W
Tj	Operating Junction Temperature		–40 to +150	°C
Tstg	Storage temperature		–40 to +125	°C
Tc	Module Case Operation Temperature		–40 to +125	°C
Viso	Isolation voltage	60 Hz, Sinusoidal, AC 1 minute, Connection Pins to Heat Sink Plate	2500	V rms

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Refer to [ELECTRICAL CHARACTERISTICS](#), [RECOMMENDED OPERATING RANGES](#) and/or APPLICATION INFORMATION for Safe Operating parameters.
- This surge voltage developed by the switching operation due to the wiring inductance between P and NU, NV, NW terminal.

## THERMAL CHARACTERISTICS

Symbol	Rating	Conditions	Min	Typ	Max	Unit
R <sub>th(j-c)Q</sub>	Junction-to-Case Thermal Resistance	Inverter IGBT Part (per 1/6 module)	–	–	1.1	°C/W
R <sub>th(j-c)F</sub>		Inverter FWD Part (per 1/6 module)	–	–	2.2	°C/W

- Refer to [ELECTRICAL CHARACTERISTICS](#), [RECOMMENDED OPERATING RANGES](#) and/or APPLICATION INFORMATION for Safe Operating parameters.

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## RECOMMENDED OPERATING CONDITIONS

Symbol	Rating	Conditions	Min	Typ	Max	Unit	
VPN	Supply Voltage	P-NU, NV, NW	-	300	400	V	
VDD	Gate Driver Supply Voltages	VDD(UH,VH,WH), VDD(L)-VSS	13.5	15	16.5	V	
VBS		VB(U)-VS(U), VB(V)-VS(V), VB(W)-VS(W)	13.0	15	18.5	V	
dVDD / dt, dVBS / dt	Supply Voltage Variation		-1	-	1	V/ $\mu$ s	
fPWM	PWM Frequency		1	-	20	kHz	
DT	Dead Time	Turn-off to Turn-on (external)	1.5	-	-	$\mu$ s	
Io	Allowable r.m.s. Current	VPN = 300 V, VDD = 15 V, P.F. = 0.8 Tc $\leq$ 125°C, Tj $\leq$ 150°C (Note 5)	f <sub>PWM</sub> = 5 kHz	-	-	25.7	A rms
			f <sub>PWM</sub> = 15 kHz	-	-	18.8	
PWIN (on)	Allowable Input Pulse Width	200 V $\leq$ VPN $\leq$ 400 V 13.5 V $\leq$ VDD $\leq$ 16.5 V 13.0 V $\leq$ VBS $\leq$ 18.5 V -20°C $\leq$ Tc $\leq$ 100°C	1.0	-	-	$\mu$ s	
PWIN (off)			1.5	-	-		
	Package Mounting Torque	M3 type screw	0.6	0.7	0.9	Nm	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

- Allowable r.m.s current depends on the actual conditions.
- Flatness tolerance of the heatsink should be within  $-50 \mu\text{m}$  to  $+100 \mu\text{m}$ .

## ELECTRICAL CHARACTERISTICS (Tc = 25°C, VDD = 15 V, VBS = 15 V, unless otherwise specified.) (Note 7)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### INVERTER SECTION

Ices	Collector-Emitter Leakage Current		Vce = Vces, Tj = 25°C	-	-	1	mA
			Vce = Vces, Tj = 150°C	-	-	10	mA
VCE(sat)	Collector-Emitter Saturation Voltage		VDD = VBS = 15 V, IN = 5 V Ic = 30 A, Tj = 25°C	-	1.60	2.30	V
			VDD = VBS = 15 V, IN = 5 V Ic = 30 A, Tj = 150°C	-	1.80	-	V
VF	FWDi Forward Voltage		IN = 0 V, If = 30 A, Tj = 25°C	-	2.00	2.40	V
			IN = 0 V, If = 30 A, Tj = 150°C	-	2.00	-	V
ton	High side	Switching Times	VPN = 300 V, VDD(H) = VDD(L) = 15 V Ic = 30 A, Tj = 25°C, IN = 0 $\Leftrightarrow$ 5 V Inductive Load	0.80	1.25	1.85	$\mu$ s
tc(on)				-	0.25	0.65	$\mu$ s
toff				-	1.60	2.20	$\mu$ s
tc(off)				-	0.25	0.75	$\mu$ s
trr				-	0.15	-	$\mu$ s
ton	Low side	Switching Times	VPN = 300 V, VDD(H) = VDD(L) = 15 V Ic = 30 A, Tj = 25°C, IN = 0 $\Leftrightarrow$ 5 V Inductive Load	0.80	1.40	2.00	$\mu$ s
tc(on)				-	0.25	0.55	$\mu$ s
toff				-	1.60	2.20	$\mu$ s
tc(off)				-	0.25	0.75	$\mu$ s
trr				-	0.10	-	$\mu$ s

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**ELECTRICAL CHARACTERISTICS** ( $T_c = 25^\circ\text{C}$ ,  $V_{DD} = 15\text{ V}$ ,  $V_{BS} = 15\text{ V}$ , unless otherwise specified.) (Note 7) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit	
<b>DRIVER SECTION</b>							
IQDDH	Quiescent VDD Supply Current	$V_{DD}(UH, VH, WH) = 15\text{ V}$ , $HIN(U, V, W) = 0\text{ V}$	$V_{DD}(UH)-V_{SS}$ $V_{DD}(VH)-V_{SS}$ $V_{DD}(WH)-V_{SS}$	-	-	0.30	mA
IQDDL		$V_{DD}(L) = 15\text{ V}$ , $LIN(U, V, W) = 0\text{ V}$	$V_{DD}(L)-V_{SS}$	-	-	3.50	mA
IPDDH	Operating VDD Supply Current	$V_{DD}(UH, VH, WH) = 15\text{ V}$ , $f_{PWM} = 20\text{ kHz}$ , Duty = 50%, Applied to one PWM Signal Input for High-Side	$V_{DD}(UH)-V_{SS}$ $V_{DD}(VH)-V_{SS}$ $V_{DD}(WH)-V_{SS}$	-	-	0.40	mA
IPDDL		$V_{DD}(L) = 15\text{ V}$ , $f_{PWM} = 20\text{ kHz}$ , Duty = 50%, Applied to one PWM Signal Input for Low-Side	$V_{DD}(L)-V_{SS}$	-	-	6.00	mA
IQBS	Quiescent VBS Supply Current	$V_{BS} = 15\text{ V}$ , $HIN(U, V, W) = 0\text{ V}$	$VB(U)-VS(U)$ $VB(V)-VS(V)$ $VB(W)-VS(W)$	-	-	0.30	mA
IPBS	Operating VBS Supply Current	$V_{DD} = V_{BS} = 15\text{ V}$ , $f_{PWM} = 20\text{ kHz}$ , Duty = 50%, Applied to one PWM Signal Input for High-Side	$VB(U)-VS(U)$ $VB(V)-VS(V)$ $VB(W)-VS(W)$	-	-	5.00	mA
VIN(ON)	ON Threshold voltage	$HIN(U, V, W)-V_{SS}$ , $LIN(U, V, W)-V_{SS}$	-	-	2.6	V	
VIN(OFF)	OFF Threshold voltage		0.8	-	-	V	
VCIN(ref)	Short Circuit Trip Level	$V_{DD} = 15\text{ V}$ , $CIN-V_{SS}$	0.46	0.48	0.50	V	
UVDDD	Supply Circuit Under-Voltage Protection	Detection Level	10.3	-	12.5	V	
UVDDR		Reset Level	10.8	-	13.0	V	
UVBSD		Detection Level	10.0	-	12.0	V	
UVBSR		Reset Level	10.5	-	12.5	V	
VTS	Voltage Output for LVIC Temperature Sensing Unit	$V_{TS}-V_{SS} = 10\text{ nF}$ , Temp. = $25^\circ\text{C}$	0.905	1.030	1.155	V	
VFOH	Fault Output Voltage	$V_{DD} = 0\text{ V}$ , $CIN = 0\text{ V}$ , VFO Circuit: $10\text{ k}\Omega$ to $5\text{ V}$ Pull-up	4.9	-	-	V	
VFOL		$V_{DD} = 0\text{ V}$ , $CIN = 1\text{ V}$ , VFO Circuit: $10\text{ k}\Omega$ to $5\text{ V}$ Pull-up	-	-	0.95	V	
$t_{FOD}$	Fault-Output Pulse Width	$CFOD = 22\text{ nF}$	1.6	2.4	-	ms	

## BOOTSTRAP SECTION

VF	Bootstrap Diode Forward Voltage	$I_f = 0.1\text{ A}$	3.4	4.6	5.8	V
RBOOT	Built-in Limiting Resistance		30	38	46	$\Omega$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at  $T_J = T_A = 25^\circ\text{C}$ . Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

8. The fault-out pulse width  $t_{FOD}$  depends on the capacitance value of CFOD according to the following approximate equation:

$$t_{FOD} = 0.11 \times 10^6 \times CFOD \text{ (s)}$$

9. Values based on design and/or characterization.

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## Temperature of LVIC versus VTS Characteristics

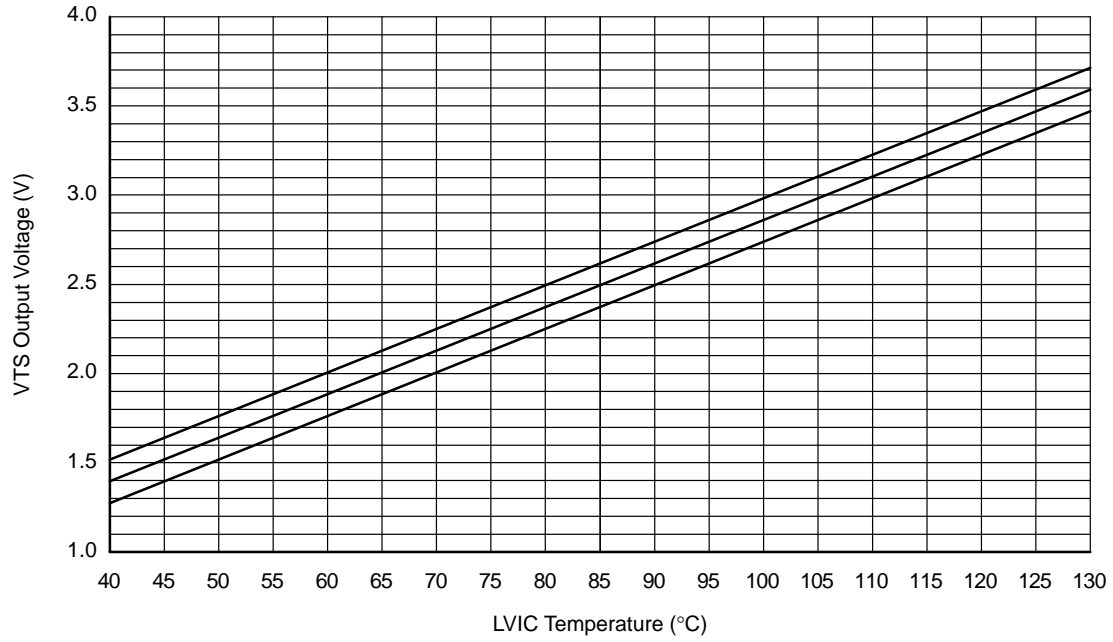
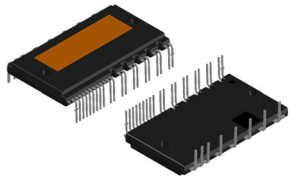


Figure 4. Temperature of LVIC versus VTS Characteristics



# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



## DIP39, 54.50x31.00x5.60, 1.78P EP-2 CASE MODGX ISSUE A

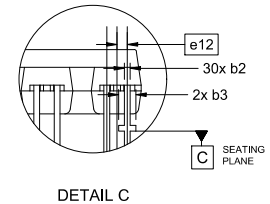
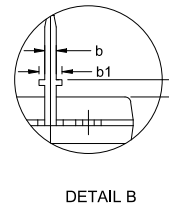
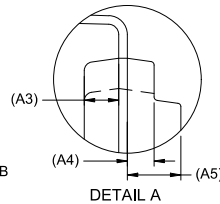
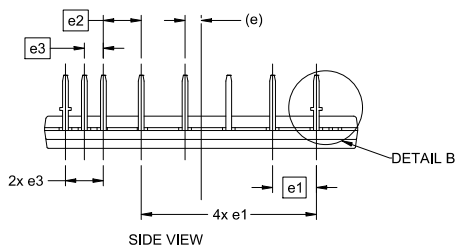
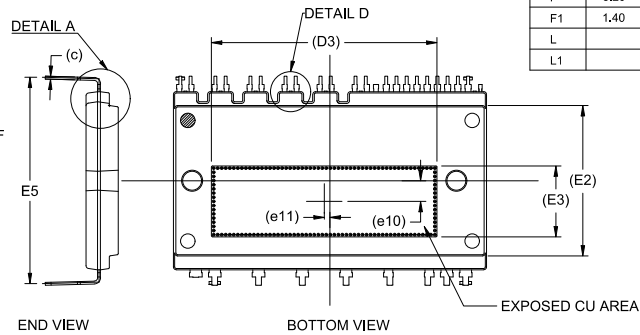
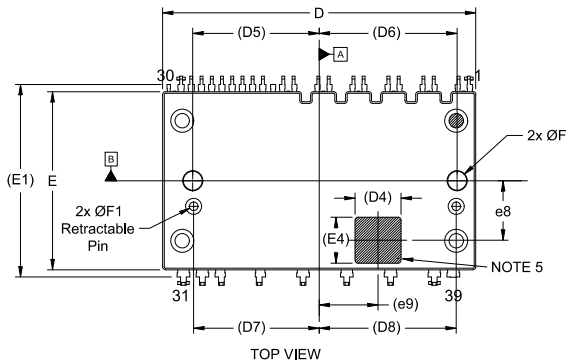
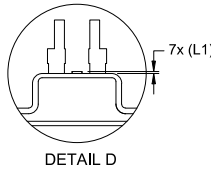
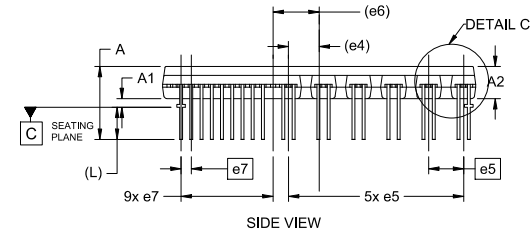
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**NOTES:**

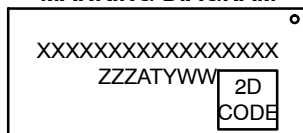
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b and c APPLY TO THE PLATED LEADS AND ARE MEASURED BETWEEN 1.00 AND 2.00 FROM THE LEAD TIP
4. POSITION OF THE LEAD IS DETERMINED AT THE BASE OF THE LEAD WHERE IT EXITS THE PACKAGE BODY
5. AREA FOR 2D BAR CODE
6. SHORTENED/CUT PINS ARE 2,5,8,11,14,17,19,29, 30 AND 39

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	12.20	12.7	13.2
A1	1.00	1.50	2.00
A2	5.50	5.60	5.70
A3	2.00 REF		
A4	1.55 REF		
A5	3.10 REF		
b	0.90	1.00	1.10
b1	1.90	2.00	2.10
b2	0.40	0.50	0.60
b3	1.40	1.50	1.60
c	0.50 REF		
D	54.40	54.50	54.60
D3	39.25 REF		
D4	8.00 REF		
D5	22.00 REF		
D6	24.00 REF		
D7	21.85 REF		
D8	23.85 REF		

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E	30.90	31.00	31.10
E1	33.50 REF		
E2	26.14 REF		
E3	12.35 REF		
E4	8.00 REF		
E5	35.40	35.90	36.40
e	2.81 REF		
e1	7.62 BSC		
e2	6.60 BSC		
e3	3.30 BSC		
e4	5.35 REF		
e5	6.10 BSC		
e6	8.02 REF		
e7	1.78 BSC		
e8	10.35 REF		
e9	10.25 REF		
e10	3.60 REF		
e11	1.00 REF		
e12	0.89 BSC		
F	3.20	3.30	3.40
F1	1.40	1.50	1.60
L	5.60 REF		
L1	0.10 REF		



**GENERIC MARKING DIAGRAM\***



XXXXX = Specific Device Code  
 ZZZ = Assembly Lot Code  
 AT = Assembly & Test Location  
 Y = Year  
 WW = Work Week

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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<b>DESCRIPTION:</b>	<b>DIP39, 54.50x31.00x5.60, 1.78P EP-2</b>	<b>PAGE 1 OF 1</b>

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