Dual Operational Transconductance Amplifier

NE5517

The NE5517 contains two current-controlled transconductance amplifiers, each with a differential input and push-pull output. The NE5517 offers significant design and performance advantages over similar devices for all types of programmable gain applications. Circuit performance is enhanced through the use of linearizing diodes at the inputs which enable a 10 dB signal-to-noise improvement referenced to 0.5% THD. The NE5517 is suited for a wide variety of industrial and consumer applications.

Constant impedance of the buffers on the chip allow general use of the NE5517. These buffers are made of Darlington transistors and a biasing network that virtually eliminate the change of offset voltage due to a burst in the bias current IABC, hence eliminating the audible noise that could otherwise be heard in high quality audio applications.

Features
• Constant Impedance Buffers
• $\Delta V_{BE}$ of Buffer is Constant with Amplifier IBIAS Change
• Excellent Matching Between Amplifiers
• Linearizing Diodes
• High Output Signal-to-Noise Ratio
• This is a Pb–Free Device

Applications
• Multiplexers
• Timers
• Electronic Music Synthesizers
• Dolby® HX Systems
• Current-Controlled Amplifiers, Filters
• Current-Controlled Oscillators, Impedances

MARKING DIAGRAM

PIN CONNECTIONS

ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.
## PIN DESCRIPTION

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$I_{ABCa}$</td>
<td>Amplifier Bias Input A</td>
</tr>
<tr>
<td>2</td>
<td>$D_a$</td>
<td>Diode Bias A</td>
</tr>
<tr>
<td>3</td>
<td>$+IN_a$</td>
<td>Non-inverted Input A</td>
</tr>
<tr>
<td>4</td>
<td>$-IN_a$</td>
<td>Inverted Input A</td>
</tr>
<tr>
<td>5</td>
<td>$VO_a$</td>
<td>Output A</td>
</tr>
<tr>
<td>6</td>
<td>$V-$</td>
<td>Negative Supply</td>
</tr>
<tr>
<td>7</td>
<td>$IN_{BUFFERa}$</td>
<td>Buffer Input A</td>
</tr>
<tr>
<td>8</td>
<td>$VO_{BUFFERa}$</td>
<td>Buffer Output A</td>
</tr>
<tr>
<td>9</td>
<td>$VO_{BUFFERb}$</td>
<td>Buffer Output B</td>
</tr>
<tr>
<td>10</td>
<td>$IN_{BUFFERb}$</td>
<td>Buffer Input B</td>
</tr>
<tr>
<td>11</td>
<td>$V+$</td>
<td>Positive Supply</td>
</tr>
<tr>
<td>12</td>
<td>$VO_b$</td>
<td>Output B</td>
</tr>
<tr>
<td>13</td>
<td>$-IN_b$</td>
<td>Inverted Input B</td>
</tr>
<tr>
<td>14</td>
<td>$+IN_b$</td>
<td>Non-inverted Input B</td>
</tr>
<tr>
<td>15</td>
<td>$D_b$</td>
<td>Diode Bias B</td>
</tr>
<tr>
<td>16</td>
<td>$I_{ABCb}$</td>
<td>Amplifier Bias Input B</td>
</tr>
</tbody>
</table>

---

**Figure 1. Circuit Schematic**
NOTE: V+ of output buffers and amplifiers are internally connected.

Figure 2. Connection Diagram

MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (Note 1)</td>
<td>VS</td>
<td>44 VDC or ±22 V</td>
<td></td>
</tr>
<tr>
<td>Power Dissipation, $T_{amb} = 25$ °C (Still Air) (Note 2)</td>
<td>PD</td>
<td>1125 mW</td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, Junction–to–Ambient</td>
<td>$R_{JA}$</td>
<td>140 °C/W</td>
<td></td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>$V_{IN}$</td>
<td>±5.0 V</td>
<td></td>
</tr>
<tr>
<td>Diode Bias Current</td>
<td>$I_{D}$</td>
<td>2.0 mA</td>
<td></td>
</tr>
<tr>
<td>Amplifier Bias Current</td>
<td>$I_{ABC}$</td>
<td>2.0 mA</td>
<td></td>
</tr>
<tr>
<td>Output Short-Circuit Duration</td>
<td>$I_{SC}$</td>
<td>Indefinite</td>
<td></td>
</tr>
<tr>
<td>Buffer Output Current (Note 3)</td>
<td>$I_{OUT}$</td>
<td>20 mA</td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>$T_{amb}$</td>
<td>0 °C to +70 °C</td>
<td>°C</td>
</tr>
<tr>
<td>Operating Junction Temperature</td>
<td>$T_{J}$</td>
<td>150 °C</td>
<td></td>
</tr>
<tr>
<td>DC Input Voltage</td>
<td>$V_{DC}$</td>
<td>$+V_{S}$ to $-V_{S}$</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$T_{stg}$</td>
<td>−65 °C to +150 °C</td>
<td>°C</td>
</tr>
<tr>
<td>Lead Soldering Temperature (10 sec max)</td>
<td>$T_{slid}$</td>
<td>230 °C</td>
<td></td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. For selections to a supply voltage above ±22 V, contact factory.
2. The following derating factors should be applied above 25 °C
   D package at 7.1 mW/°C.
3. Buffer output current should be limited so as to not exceed package dissipation.
## ELECTRICAL CHARACTERISTICS (Note 4)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Test Conditions</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Offset Voltage</td>
<td>Overtemperature Range</td>
<td>$V_{OS}$</td>
<td>0.4</td>
<td>5.0</td>
<td>5.0</td>
<td>mV</td>
</tr>
<tr>
<td>$\Delta V_{OS}/\Delta T$</td>
<td>Avg. TC of Input Offset Voltage</td>
<td></td>
<td>0.3</td>
<td>5.0</td>
<td>5.0</td>
<td>mV/°C</td>
</tr>
<tr>
<td>$V_{OS}$ Including Diodes</td>
<td>Diode Bias Current ($I_D = 500 \mu A$)</td>
<td></td>
<td>0.5</td>
<td>5.0</td>
<td>5.0</td>
<td>mV</td>
</tr>
<tr>
<td>Input Offset Change</td>
<td>$5.0 \mu A \leq I_{ABC} \leq 500 \mu A$</td>
<td>$V_{OS}$</td>
<td>0.1</td>
<td>0.6</td>
<td>0.6</td>
<td>μA</td>
</tr>
<tr>
<td>Input Offset Current</td>
<td></td>
<td></td>
<td>0.1</td>
<td>0.6</td>
<td>0.6</td>
<td>μA</td>
</tr>
<tr>
<td>$\Delta I_{OS}/\Delta T$</td>
<td>Avg. TC of Input Offset Current</td>
<td></td>
<td>0.001</td>
<td>5.0</td>
<td>5.0</td>
<td>μA/°C</td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>Overtemperature Range</td>
<td>$I_{BIAS}$</td>
<td>0.4</td>
<td>1.0</td>
<td>1.0</td>
<td>μA</td>
</tr>
<tr>
<td>$\Delta I_{B}/\Delta T$</td>
<td>Avg. TC of Input Current</td>
<td></td>
<td>0.01</td>
<td>5.00</td>
<td>5.00</td>
<td>μA/°C</td>
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<tr>
<td>Forward Transconductance</td>
<td></td>
<td>$g_m$</td>
<td>6700</td>
<td>5400</td>
<td>9600</td>
<td>13000</td>
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<td>$g_m$ Tracking</td>
<td></td>
<td></td>
<td>0.3</td>
<td></td>
<td></td>
<td>dB</td>
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<tr>
<td>Peak Output Current</td>
<td></td>
<td>$I_{OUT}$</td>
<td>350</td>
<td>300</td>
<td>500</td>
<td>650</td>
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<tr>
<td>Peak Output Voltage</td>
<td></td>
<td>$V_{OUT}$</td>
<td>+14</td>
<td>12</td>
<td>+14</td>
<td>12</td>
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<tr>
<td>Positive</td>
<td></td>
<td></td>
<td>5.0</td>
<td>350</td>
<td>650</td>
<td>12</td>
</tr>
<tr>
<td>Negative</td>
<td></td>
<td></td>
<td>5.0</td>
<td>300</td>
<td>300</td>
<td>12</td>
</tr>
<tr>
<td>Supply Current</td>
<td>$I_{ABC} = 500 \mu A$, both channels</td>
<td>$I_{CC}$</td>
<td>2.6</td>
<td>4.0</td>
<td>4.0</td>
<td>mA</td>
</tr>
<tr>
<td>$V_{OS}$ Sensitivity</td>
<td>Positive</td>
<td>$\Delta V_{OS}/V^+$</td>
<td>20</td>
<td>20</td>
<td>150</td>
<td>μV/V</td>
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<tr>
<td>Negative</td>
<td>$\Delta V_{OS}/V^-$</td>
<td></td>
<td>20</td>
<td>150</td>
<td>150</td>
<td>μV/V</td>
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<tr>
<td>Common-mode Rejection Ration</td>
<td></td>
<td>CMRR</td>
<td>80</td>
<td>110</td>
<td>110</td>
<td>dB</td>
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<tr>
<td>Common-mode Range</td>
<td></td>
<td></td>
<td>±12</td>
<td>±13.5</td>
<td>±13.5</td>
<td>V</td>
</tr>
<tr>
<td>Crosstalk</td>
<td>Referred to Input (Note 5)</td>
<td></td>
<td>100</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Differential Input Current</td>
<td>$I_{ABC} = 0$, Input $= \pm 4.0$ V</td>
<td>$I_{IN}$</td>
<td>0.02</td>
<td>100</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td>Leakage Current</td>
<td>$I_{ABC} = 0$ (Refer to Test Circuit)</td>
<td></td>
<td>0.2</td>
<td>100</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td>Input Resistance</td>
<td></td>
<td>$R_{IN}$</td>
<td>10</td>
<td>26</td>
<td>26</td>
<td>kΩ</td>
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<tr>
<td>Open-loop Bandwidth</td>
<td>Unity Gain Compensated</td>
<td>$B_W$</td>
<td>2.0</td>
<td></td>
<td></td>
<td>MHz</td>
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<tr>
<td>Slew Rate</td>
<td></td>
<td>$S_R$</td>
<td></td>
<td>50</td>
<td></td>
<td>μV/μs</td>
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<tr>
<td>Buffer Input Current</td>
<td></td>
<td>$I_{NBUFFER}$</td>
<td>0.4</td>
<td>5.0</td>
<td>5.0</td>
<td>μA</td>
</tr>
<tr>
<td>Peak Buffer Output Voltage</td>
<td></td>
<td>$V_{OBUFFER}$</td>
<td>10</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$\Delta V_{BE}$ of Buffer</td>
<td>Refer to Buffer $V_{BE}$ Test Circuit (Note 6)</td>
<td></td>
<td>0.5</td>
<td>5.0</td>
<td>5.0</td>
<td>mV</td>
</tr>
</tbody>
</table>

4. These specifications apply for $V_S = \pm 15$ V, $T_{amb} = 25$ °C, amplifier bias current ($I_{ABC}$) = 500 μA, Pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.
5. These specifications apply for $V_S = \pm 15$ V, $I_{ABC} = 500 \mu A$, $R_{OUT} = 5.0$ kΩ connected from the buffer output to $-V_S$ and the input of the buffer is connected to the transconductance amplifier output.
6. $V_S = \pm 15$, $R_{OUT} = 5.0$ kΩ connected from Buffer output to $-V_S$ and $5.0 \mu A \leq I_{ABC} \leq 500 \mu A$. 
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Figure 12. Amplifier Bias Voltage vs. Amplifier Bias Current

Figure 13. Input and Output Capacitance

Figure 14. Distortion vs. Differential Input Voltage

Figure 15. Voltage vs. Amplifier Bias Current

Figure 16. Noise vs. Frequency

Figure 17. Leakage Current Test Circuit

Figure 18. Differential Input Current Test Circuit

Figure 19. Buffer $V_{BE}$ Test Circuit
CIRCUIT DESCRIPTION

The circuit schematic diagram of one-half of the NE5517, a dual operational transconductance amplifier with linearizing diodes and impedance buffers, is shown in Figure 21.

Transconductance Amplifier

The transistor pair, Q4 and Q5, forms a transconductance stage. The ratio of their collector currents (I⁵ and I⁴, respectively) is defined by the differential input voltage, Vᵢⁿ, which is shown in Equation 1.

\[ Vᵢⁿ = \frac{KT}{q} \ln \frac{I⁵}{I⁴} \quad (eq. 1) \]

Where Vᵢⁿ is the difference of the two input voltages

\[ KT \equiv 26 \text{ mV at room temperature (300 K).} \]

Transistors Q1, Q2 and diode D1 form a current mirror which focuses the sum of current I⁴ and I⁵ to be equal to amplifier bias current I_B:

\[ I_4 + I_5 = I_B \quad (eq. 2) \]

If Vᵢⁿ is small, the ratio of I₅ and I₄ will approach unity and the Taylor series of ln function can be approximated as

\[ \frac{KT}{q} \ln \frac{I⁵}{I⁴} = \frac{KT}{q} \frac{I⁵ - I⁴}{I⁴} \]

and \[ I_5 \approx I_5 = I_B \]

\[ \frac{KT}{q} \ln \frac{I⁵}{I⁴} = \frac{KT}{q} \frac{I⁵ - I⁴}{1/2I_B} = \frac{2KT}{q} \frac{I⁵ - I⁴}{I_B} = Vᵢⁿ \quad (eq. 4) \]

The remaining transistors (Q₆ to Q₁₁) and diodes (D₄ to D₆) form three current mirrors that produce an output current equal to I₅ minus I₄. Thus:

\[ Vᵢⁿ \left( \frac{I_B}{2KT} \right) = I_O \quad (eq. 5) \]

The term \( \left( \frac{I_B}{2KT} \right) \) is then the transconductance of the amplifier and is proportional to I_B.

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**APPLICATIONS**
Linearizing Diodes

For $V_{IN}$ greater than a few millivolts, Equation 3 becomes invalid and the transconductance increases non-linearly. Figure 22 shows how the internal diodes can linearize the transfer function of the operational amplifier. Assume $D_2$ and $D_3$ are biased with current sources and the input signal current is $I_S$. Since $I_4 + I_5 = I_B$ and $I_5 - I_4 = I_0$, that is: $I_4 = (I_B - I_0)$, $I_5 = (I_B + I_0)$

$$I_0 = \frac{I_D}{2} - \frac{I_S}{2} + I_S$$

The only limitation is that the signal current should not exceed $I_D$.

Impedance Buffer

The upper limit of transconductance is defined by the maximum value of $I_B$ (2.0 mA). The lowest value of $I_B$ for which the amplifier will function therefore determines the overall dynamic range. At low values of $I_B$, a buffer with very low input bias current is desired. A Darlington amplifier with constant-current source ($Q_{14}$, $Q_{15}$, $Q_{16}$, $D_7$, $D_8$, and $R_1$) suits the need.

APPLICATIONS

Voltage-Controlled Amplifier

In Figure 23, the voltage divider $R_2$, $R_3$ divides the input-voltage into small values (mV range) so the amplifier operates in a linear manner.

It is:

$$I_{OUT} = -\frac{V_{IN}}{R_2 + R_3} \cdot g_M;$$

$$V_{OUT} = I_{OUT} \cdot R_L;$$

$$A = \frac{V_{OUT}}{V_{IN}} = \frac{R_3}{R_2 + R_3} \cdot g_M \cdot R_L$$

$$g_M = 19.2 \frac{I_{ABC}}{mhos}$$

Since $g_M$ is directly proportional to $I_{ABC}$, the amplification is controlled by the voltage $V_C$ in a simple way.

When $V_C$ is taken relative to $-V_{CC}$ the following formula is valid:

$$I_{ABC} = \frac{(V_C - 1.2V)}{R_1}$$

The 1.2 V is the voltage across two base-emitter baths in the current mirrors. This circuit is the base for many applications of the NE5517.

Figure 22. Linearizing Diode

Figure 23.
Stereo Amplifier With Gain Control

Figure 24 shows a stereo amplifier with variable gain via a control input. Excellent tracking of typical 0.3 dB is easy to achieve. With the potentiometer, RP, the offset can be adjusted. For AC-coupled amplifiers, the potentiometer may be replaced with two 510 Ω resistors.

Modulators

Because the transconductance of an OTA (Operational Transconductance Amplifier) is directly proportional to $I_{ABC}$, the amplification of a signal can be controlled easily. The output current is the product of transconductance×input voltage. The circuit is effective up to approximately 200 kHz. Modulation of 99% is easy to achieve.
Voltage-Controlled Resistor (VCR)

Because an OTA is capable of producing an output current proportional to the input voltage, a voltage variable resistor can be made. Figure 26 shows how this is done. A voltage presented at the RX terminals forces a voltage at the input. This voltage is multiplied by $g_M$ and thereby forces a current through the RX terminals:

$$R_X = \frac{R + RA}{g_M + RA}$$

where $g_M$ is approximately 19.21 $\mu$MHOs at room temperature. Figure 27 shows a Voltage Controlled Resistor using linearizing diodes. This improves the noise performance of the resistor.

Voltage-Controlled Filters

Figure 28 shows a Voltage Controlled Low-Pass Filter. The circuit is a unity gain buffer until $Xc/g_M$ is equal to $R/RA$. Then, the frequency response rolls off at a 6dB per octave with the $-3\ dB$ point being defined by the given equations. Operating in the same manner, a Voltage Controlled High-Pass Filter is shown in Figure 29. Higher order filters can be made using additional amplifiers as shown in Figures 30 and 31.

Voltage-Controlled Oscillators

Figure 32 shows a voltage-controlled triangle-square wave generator. With the indicated values a range from 2.0 Hz to 200 kHz is possible by varying $I_{ABC}$ from 1.0 mA to 10 $\mu$A.

The output amplitude is determined by $I_{OUT} \times R_{OUT}$.

Please notice the differential input voltage is not allowed to be above 5.0 V.

With a slight modification of this circuit you can get the sawtooth pulse generator, as shown in Figure 33.

APPLICATION HINTS

To hold the transconductance $g_M$ within the linear range, $I_{ABC}$ should be chosen not greater than 1.0 mA. The current mirror ratio should be as accurate as possible over the entire current range. A current mirror with only two transistors is not recommended. A suitable current mirror can be built with a PNP transistor array which causes excellent matching and thermal coupling among the transistors. The output current range of the DAC normally reaches from 0 to $-2.0$ mA. In this application, however, the current range is set through $R_{REF} (10 \ k\Omega)$ to 0 to $-1.0$ mA.

$$I_{DACMAX} = 2 \cdot \frac{V_{REF}}{R_{REF}} = 2 \cdot \frac{5V}{10k\Omega} = 1mA$$

$$R_X = \frac{R + RA}{g_M \cdot RA}$$

Figure 26. VCR

Figure 27. VCR with Linearizing Diodes
NOTE:
\[ f_0 = \frac{R_A g_m}{g(R + R_A) 2\pi C} \]

Figure 28. Voltage-Controlled Low-Pass Filter

NOTE:
\[ f_0 = \frac{R_A g_m}{g(R + R_A) 2\pi C} \]

Figure 29. Voltage-Controlled High-Pass Filter

NOTE:
\[ f_0 = \frac{R_A g_m}{(R + R_A) 2\pi C} \]

Figure 30. Butterworth Filter – 2nd Order
NE5517

Figure 31. State Variable Filter

Figure 32. Triangle–Square Wave Generator (VCO)

Figure 33. Sawtooth Pulse VCO

NOTE:

\[ V_{PK} = \frac{(V_C - 0.8) R_1}{R_1 + R_2} \]

\[ T_H = \frac{2V_{PK} C}{I_B} \]

\[ T_L = \frac{2V_{PK} C}{I_C} \]

\[ I_C = \frac{I_{OSC}}{2V_{PK} C} \]

\[ I_C < I_B \]
## ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Temperature Range</th>
<th>Package</th>
<th>Shipping¹</th>
</tr>
</thead>
<tbody>
<tr>
<td>NE5517DR2G</td>
<td>0 to +70 °C</td>
<td>SOIC-16 (Pb-Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
</tbody>
</table>

¹For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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SOIC-16
CASE 751B-05
ISSUE K

SCALE 1:1

NOTEs:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

STYLe: 1:
P1 1. COLLECTOR
2. BASE
3. Emitter
4. NO CONNECTION
5. Emitter
6. BASE
7. Collector
8. Collector
9. BASE
10. Emitter
11. NO CONNECTION
12. Emitter
13. BASE
14. COLLECTOR
15. Emitter
16. COLLECTOR

STYLe: 2:
P1 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. ANODE
13. CATHODE
14. CATHODE
15. ANODE
16. CATHODE

STYLe: 3:
P1 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. COLLECTOR, #3
8. COLLECTOR, #4
9. BASE, #3
10. EMITTER, #3
11. BASE, #2
12. EMITTER, #2
13. BASE, #1
14. EMITTER, #1

STYLe: 4:
P1 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLe: 5:
P1 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. CATHODE
15. CATHODE
16. CATHODE

STYLe: 6:
P1 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLe: 7:
P1 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE N-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. COMMON DRAIN (OUTPUT)
9. SOURCE P-CH
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. CATHODE
15. CATHODE
16. CATHODE

SOLDERING FOOTPRINT

DIMENSIONS: MILLIMETERS

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