NE5517, NE5517A, AU5517

Dual Operational Transconductance Amplifier

The AU5517 and NE5517 contain two current-controlled transconductance amplifiers, each with a differential input and push-pull output. The AU5517/NE5517 offers significant design and performance advantages over similar devices for all types of programmable gain applications. Circuit performance is enhanced through the use of linearizing diodes at the inputs which enable a 10 dB signal-to-noise improvement referenced to 0.5% THD. The AU5517/NE5517 is suited for a wide variety of industrial and consumer applications.

Constant impedance of the buffers on the chip allow general use of the AU5517/NE5517. These buffers are made of Darlington transistors and a biasing network that virtually eliminate the change of offset voltage due to a burst in the bias current I_ABC, hence eliminating the audible noise that could otherwise be heard in high quality audio applications.

Features

- Constant Impedance Buffers
- ΔV_BE of Buffer is Constant with Amplifier I_BIAS Change
- Excellent Matching Between Amplifiers
- Linearizing Diodes
- High Output Signal-to-Noise Ratio
- Pb-Free Packages are Available*

Applications

- Multiplexers
- Timers
- Electronic Music Synthesizers
- Dolby® HX Systems
- Current-Controlled Amplifiers, Filters
- Current-Controlled Oscillators, Impedances

MARKING DIAGRAMS

PIN CONNECTIONS

ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.
<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>I_{ABCa}</td>
<td>Amplifier Bias Input A</td>
</tr>
<tr>
<td>2</td>
<td>D_a</td>
<td>Diode Bias A</td>
</tr>
<tr>
<td>3</td>
<td>+IN_a</td>
<td>Non-inverted Input A</td>
</tr>
<tr>
<td>4</td>
<td>−IN_a</td>
<td>Inverted Input A</td>
</tr>
<tr>
<td>5</td>
<td>VO_a</td>
<td>Output A</td>
</tr>
<tr>
<td>6</td>
<td>V−</td>
<td>Negative Supply</td>
</tr>
<tr>
<td>7</td>
<td>I_{BUFFERa}</td>
<td>Buffer Input A</td>
</tr>
<tr>
<td>8</td>
<td>VO_{BUFFERa}</td>
<td>Buffer Output A</td>
</tr>
<tr>
<td>9</td>
<td>VO_{BUFFERb}</td>
<td>Buffer Output B</td>
</tr>
<tr>
<td>10</td>
<td>I_{BUFFERb}</td>
<td>Buffer Input B</td>
</tr>
<tr>
<td>11</td>
<td>V+</td>
<td>Positive Supply</td>
</tr>
<tr>
<td>12</td>
<td>VO_b</td>
<td>Output B</td>
</tr>
<tr>
<td>13</td>
<td>−IN_b</td>
<td>Inverted Input B</td>
</tr>
<tr>
<td>14</td>
<td>+IN_b</td>
<td>Non-inverted Input B</td>
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<td>15</td>
<td>D_b</td>
<td>Diode Bias B</td>
</tr>
<tr>
<td>16</td>
<td>I_{ABCb}</td>
<td>Amplifier Bias Input B</td>
</tr>
</tbody>
</table>

**Figure 1. Circuit Schematic**
NOTE: V+ of output buffers and amplifiers are internally connected.

Figure 2. Connection Diagram

MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (Note 1)</td>
<td>V_S</td>
<td>44 V_DC or ±22 V</td>
<td></td>
</tr>
<tr>
<td>Power Dissipation, $T_{\text{amb}} = 25$ °C (Still Air) (Note 2)</td>
<td>P_D</td>
<td>1500 mW</td>
<td></td>
</tr>
<tr>
<td>NE5517N, NE5517AN</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NE5517D, AU5517D</td>
<td></td>
<td>1125 mW</td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, Junction–to–Ambient</td>
<td>R_{JA}</td>
<td>140 °C/W</td>
<td></td>
</tr>
<tr>
<td>D Package</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>N Package</td>
<td></td>
<td>94 °C/W</td>
<td></td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>V_{IN}</td>
<td>±5.0 V</td>
<td></td>
</tr>
<tr>
<td>Diode Bias Current</td>
<td>I_D</td>
<td>2.0 mA</td>
<td></td>
</tr>
<tr>
<td>Amplifier Bias Current</td>
<td>I_{ABC}</td>
<td>2.0 mA</td>
<td></td>
</tr>
<tr>
<td>Output Short-Circuit Duration</td>
<td>I_{SC}</td>
<td>Indefinite</td>
<td></td>
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<tr>
<td>Buffer Output Current (Note 3)</td>
<td>I_{OUT}</td>
<td>20 mA</td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>T_{\text{amb}}</td>
<td>0 °C to +70 °C</td>
<td></td>
</tr>
<tr>
<td>NE5517N, NE5517AN</td>
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<td>-40 °C to +125 °C</td>
<td></td>
</tr>
<tr>
<td>AU5517T</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Junction Temperature</td>
<td>T_J</td>
<td>150 °C</td>
<td></td>
</tr>
<tr>
<td>DC Input Voltage</td>
<td>V_{DC}</td>
<td>+V_S to -V_S</td>
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<tr>
<td>Storage Temperature Range</td>
<td>T_{stg}</td>
<td>-65 °C to +150 °C</td>
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<tr>
<td>Lead Soldering Temperature (10 sec max)</td>
<td>T_{sl}</td>
<td>230 °C</td>
<td></td>
</tr>
</tbody>
</table>

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. For selections to a supply voltage above ±22 V, contact factory.
2. The following derating factors should be applied above 25 °C
   N package at 10.6 mW/°C
   D package at 7.1 mW/°C
3. Buffer output current should be limited so as to not exceed package dissipation.
## ELECTRICAL CHARACTERISTICS (Note 4)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Test Conditions</th>
<th>Symbol</th>
<th>AU5517/NE5517</th>
<th>NE5517A</th>
<th>Unit</th>
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<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
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<tr>
<td>Input Offset Voltage</td>
<td>Overtemperature Range</td>
<td>$V_{OS}$</td>
<td>0.4</td>
<td>5.0</td>
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<tr>
<td>$\Delta V_{OS}/\Delta T$</td>
<td>Avg. TC of Input Offset Voltage</td>
<td></td>
<td>0.3</td>
<td>5.0</td>
<td></td>
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<tr>
<td>$V_{OS}$ Including Diodes</td>
<td>Diode Bias Current ($I_D$) = 500 $\mu A$</td>
<td>$V_{OS}$</td>
<td>0.5</td>
<td>5</td>
<td></td>
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<tr>
<td>Input Offset Change</td>
<td></td>
<td>$I_{OS}$</td>
<td>0.1</td>
<td>0.6</td>
<td></td>
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<tr>
<td>$\Delta I_{OS}/\Delta T$</td>
<td>Avg. TC of Input Offset Current</td>
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<td>0.001</td>
<td>0.001</td>
<td></td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>Overtemperature Range</td>
<td>$I_{IBIAS}$</td>
<td>0.4</td>
<td>5</td>
<td>8.0</td>
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<tr>
<td>$\Delta I_{B}/\Delta T$</td>
<td>Avg. TC of Input Current</td>
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<td>0.01</td>
<td>0.01</td>
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<tr>
<td>Forward Transconductance</td>
<td></td>
<td>$g_m$</td>
<td>6700</td>
<td>5400</td>
<td>9600</td>
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<td>$g_m$ Tracking</td>
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<td>0.3</td>
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<tr>
<td>Peak Output Current</td>
<td></td>
<td>$I_{OUT}$</td>
<td>350</td>
<td>300</td>
<td>500</td>
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<tr>
<td>Positive</td>
<td></td>
<td>$V_{OUT}$</td>
<td>+12</td>
<td>-12</td>
<td>+14.2</td>
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<tr>
<td>Negative</td>
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<td></td>
<td></td>
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</tr>
<tr>
<td>Supply Current</td>
<td></td>
<td>$I_{CC}$</td>
<td>2.6</td>
<td></td>
<td>4.0</td>
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<tr>
<td>$V_{OS}$ Sensitivity</td>
<td>Positive</td>
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<td>20</td>
<td>20</td>
<td>150</td>
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<tr>
<td>Negative</td>
<td></td>
<td></td>
<td>20</td>
<td></td>
<td>150</td>
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<td>Common-mode Rejection Ration</td>
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<td>CMRR</td>
<td>80</td>
<td></td>
<td>110</td>
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<td>Common-mode Range</td>
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<td>$\pm 12$</td>
<td>$\pm 13.5$</td>
<td>$\pm 12$</td>
<td>$\pm 13.5$</td>
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<tr>
<td>Crosstalk</td>
<td></td>
<td></td>
<td>100</td>
<td></td>
<td>100</td>
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<tr>
<td>Differential Input Current</td>
<td></td>
<td>$I_{IN}$</td>
<td>0.02</td>
<td></td>
<td>100</td>
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<tr>
<td>Leakage Current</td>
<td></td>
<td>$I_{ABC} = 0$, Input = $\pm 4.0$ V</td>
<td>0.2</td>
<td>100</td>
<td>0.2</td>
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<tr>
<td>Input Resistance</td>
<td></td>
<td>$R_{IN}$</td>
<td>10</td>
<td></td>
<td>26</td>
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<tr>
<td>Open-loop Bandwidth</td>
<td></td>
<td>$B_W$</td>
<td>2.0</td>
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<tr>
<td>Slew Rate</td>
<td></td>
<td>$SR$</td>
<td>50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Buffer Input Current</td>
<td></td>
<td>$I_{INBUFFER}$</td>
<td>0.4</td>
<td>5.0</td>
<td></td>
</tr>
<tr>
<td>Peak Buffer Output Voltage</td>
<td></td>
<td>$V_{OUBUFFER}$</td>
<td>10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\Delta V_{BE}$ of Buffer</td>
<td></td>
<td></td>
<td>0.5</td>
<td>5.0</td>
<td>0.5</td>
</tr>
</tbody>
</table>

4. These specifications apply for $V_S = \pm 15$ V, $T_{amb} = 25^\circ C$, amplifier bias current ($I_{ABC}$) = 500 $\mu A$, Pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.

5. These specifications apply for $V_S = \pm 15$ V, $I_{ABC} = 500$ $\mu A$, $R_{OUT} = 5.0$ k$\Omega$ connected from the buffer output to $-V_S$ and the input of the buffer is connected to the transconductance amplifier output.

6. $V_S = \pm 15$, $R_{OUT} = 5.0$ k$\Omega$ connected from Buffer output to $-V_S$ and 5.0 $\mu A \leq I_{ABC} \leq 500$ $\mu A$.
Figure 3. Input Offset Voltage
Figure 4. Input Bias Current
Figure 5. Input Bias Current
Figure 6. Peak Output Current
Figure 7. Peak Output Voltage and Common-Mode Range
Figure 8. Leakage Current
Figure 9. Input Leakage
Figure 10. Transconductance
Figure 11. Input Resistance
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Figure 12. Amplifier Bias Voltage vs. Amplifier Bias Current

Figure 13. Input and Output Capacitance

Figure 14. Distortion vs. Differential Input Voltage

Figure 15. Voltage vs. Amplifier Bias Current

Figure 16. Noise vs. Frequency

Figure 17. Leakage Current Test Circuit

Figure 18. Differential Input Current Test Circuit

Figure 19. Buffer $V_{BE}$ Test Circuit
**CIRCUIT DESCRIPTION**

The circuit schematic diagram of one-half of the AU5517/NE5517, a dual operational transconductance amplifier with linearizing diodes and impedance buffers, is shown in Figure 21.

**Transconductance Amplifier**

The transistor pair, Q4 and Q5, forms a transconductance stage. The ratio of their collector currents ($I_4$ and $I_5$, respectively) is defined by the differential input voltage, $V_{IN}$, which is shown in Equation 1.

$$V_{IN} = \frac{KT}{q} \ln \frac{I_5}{I_4} \quad (eq. 1)$$

Where $V_{IN}$ is the difference of the two input voltages

$KT \equiv 26$ mV at room temperature (300°k).

Transistors Q1, Q2 and diode D1 form a current mirror which focuses the sum of current $I_4$ and $I_5$ to be equal to amplifier bias current $I_B$:

$$I_4 + I_5 = I_B \quad (eq. 2)$$

If $V_{IN}$ is small, the ratio of $I_5$ and $I_4$ will approach unity and the Taylor series of ln function can be approximated as

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{I_4}$$

and $I_5 \approx I_5 \equiv I_B$

$$\frac{KT}{q} \ln \frac{I_5}{I_4} = \frac{KT}{q} \frac{I_5 - I_4}{I_4} = \frac{2KT}{q} \frac{I_5 - I_4}{I_B} = V_{IN} \quad (eq. 4)$$

The remaining transistors (Q6 to Q11) and diodes (D4 to D6) form three current mirrors that produce an output current equal to $I_5$ minus $I_4$. Thus:

$$V_{IN} \left( \frac{I_B}{2KT} \right) = I_0 \quad (eq. 5)$$

The term $\left( \frac{I_B}{2KT} \right)$ is then the transconductance of the amplifier and is proportional to $I_B$.

---

**Figure 20. Unity Gain Follower**

**Figure 21. Circuit Diagram of NE5517**
Linearizing Diodes

For $V_{IN}$ greater than a few millivolts, Equation 3 becomes invalid and the transconductance increases non-linearly. Figure 22 shows how the internal diodes can linearize the transfer function of the operational amplifier. Assume $D_2$ and $D_3$ are biased with current sources and the input signal current is $I_S$. Since $I_4 + I_5 = I_B$ and $I_5 - I_4 = I_0$, that is: $I_4 = (I_B - I_0)$, $I_5 = (I_B + I_0)$.

\[ I_0 = 2I_S \left( \frac{I_B}{I_D} \right) \]

Figure 22. Linearizing Diode

For the diodes and the input transistors that have identical geometries and are subject to similar voltages and temperatures, the following equation is true:

\[ T_\text{q} \ln \left( \frac{I_D}{I_S} \right) + I_S = \frac{K_T}{q} \ln \left( \frac{1/2(I_B + I_0)}{1/2(I_B - I_0)} \right) \]

(eq. 6)

\[ I_0 = I_S \left( \frac{2I_B}{I_D} \right) \text{ for } |I_S| < \frac{I_D}{2} \]

The only limitation is that the signal current should not exceed $I_D$.

Impedance Buffer

The upper limit of transconductance is defined by the maximum value of $I_B$ (2.0 mA). The lowest value of $I_B$ for which the amplifier will function therefore determines the overall dynamic range. At low values of $I_B$, a buffer with very low input bias current is desired. A Darlington amplifier with constant-current source (Q14, Q15, Q16, D7, D8, and R1) suits the need.

Figures 23. Voltage-Controlled Amplifier

In Figure 23, the voltage divider $R_2$, $R_3$ divides the input-voltage into small values (mV range) so the amplifier operates in a linear manner. It is:

\[ I_{OUT} = -V_{IN} \cdot \frac{R_3}{R_2 + R_3} \cdot g_M; \]

\[ V_{OUT} = I_{OUT} \cdot R_L; \]

\[ A = \frac{V_{OUT}}{V_{IN}} = \frac{R_3}{R_2 + R_3} \cdot g_M \cdot R_L \]

(3) \[ g_M = 19.2 \cdot I_{ABC} \]

($g_M$ in $\mu$hos for $I_{ABC}$ in mA)

Since $g_M$ is directly proportional to $I_{ABC}$, the amplification is controlled by the voltage $V_C$ in a simple way. When $V_C$ is taken relative to $-V_{CC}$ the following formula is valid:

\[ I_{ABC} = \frac{(V_C - 1.2V)}{R_1} \]

The 1.2 V is the voltage across two base-emitter baths in the current mirrors. This circuit is the base for many applications of the AU5517/NE5517.
Stereo Amplifier With Gain Control

Figure 24 shows a stereo amplifier with variable gain via a control input. Excellent tracking of typical 0.3 dB is easy to achieve. With the potentiometer, $R_P$, the offset can be adjusted. For AC-coupled amplifiers, the potentiometer may be replaced with two 510 Ω resistors.

Modulators

Because the transconductance of an OTA (Operational Transconductance Amplifier) is directly proportional to $I_{ABC}$, the amplification of a signal can be controlled easily. The output current is the product of transconductance×input voltage. The circuit is effective up to approximately 200 kHz. Modulation of 99% is easy to achieve.
Voltage-Controlled Resistor (VCR)

Because an OTA is capable of producing an output current proportional to the input voltage, a voltage variable resistor can be made. Figure 26 shows how this is done. A voltage presented at the RX terminals forces a voltage at the input. This voltage is multiplied by \( g_M \) and thereby forces a current through the RX terminals:

\[
R_x = \frac{R + R_A}{g_M + R_A}
\]

where \( g_M \) is approximately 19.21 \( \mu \)MHOs at room temperature. Figure 27 shows a Voltage Controlled Resistor using linearizing diodes. This improves the noise performance of the resistor.

Voltage-Controlled Filters

Figure 28 shows a Voltage Controlled Low-Pass Filter. The circuit is a unity gain buffer until \( \frac{X_C}{g_M} \) is equal to \( \frac{R}{R_A} \). Then, the frequency response rolls off at a 6dB per octave with the −3 dB point being defined by the given equations. Operating in the same manner, a Voltage Controlled High-Pass Filter is shown in Figure 29. Higher order filters can be made using additional amplifiers as shown in Figures 30 and 31.

Voltage-Controlled Oscillators

Figure 32 shows a voltage-controlled triangle-square wave generator. With the indicated values a range from 2.0 Hz to 200 kHz is possible by varying \( I_{ABC} \) from 1.0 mA to 10 \( \mu \)A.

The output amplitude is determined by \( I_{OUT} \times R_{OUT} \). Please notice the differential input voltage is not allowed to be above 5.0 V.

With a slight modification of this circuit you can get the sawtooth pulse generator, as shown in Figure 33.

APPLICATION HINTS

To hold the transconductance \( g_M \) within the linear range, \( I_{ABC} \) should be chosen not greater than 1.0 mA. The current mirror ratio should be as accurate as possible over the entire current range. A current mirror with only two transistors is not recommended. A suitable current mirror can be built with a PNP transistor array which causes excellent matching and thermal coupling among the transistors. The output current range of the DAC normally reaches from 0 to −2.0 mA. In this application, however, the current range is set through \( R_{REF} \) (10 k\( \Omega \)) to 0 to −1.0 mA.

\[
I_{DAC\text{MAX}} = 2 \cdot \frac{V_{REF}}{R_{REF}} = 2 \cdot \frac{5V}{10k\Omega} = 1mA
\]

\[
R_X = \frac{R + R_A}{g_M \cdot R_A}
\]
Figure 28. Voltage-Controlled Low-Pass Filter

Figure 29. Voltage-Controlled High-Pass Filter

Figure 30. Butterworth Filter – 2nd Order
NE5517, NE5517A, AU5517

Figure 31. State Variable Filter

Figure 32. Triangle–Square Wave Generator (VCO)

Figure 33. Sawtooth Pulse VCO
# ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Temperature Range</th>
<th>Package</th>
<th>Shipping¹</th>
</tr>
</thead>
<tbody>
<tr>
<td>AU5517DR2</td>
<td>–40 to +125 °C</td>
<td>SOIC–16</td>
<td>2500 Tape &amp; Reel</td>
</tr>
<tr>
<td>AU5517DR2G</td>
<td></td>
<td>SOIC–16 (Pb–Free)</td>
<td></td>
</tr>
<tr>
<td>NE5517D</td>
<td></td>
<td>SOIC–16</td>
<td>48 Units/Rail</td>
</tr>
<tr>
<td>NE5517DG</td>
<td></td>
<td>SOIC–16 (Pb–Free)</td>
<td></td>
</tr>
<tr>
<td>NE5517DR2</td>
<td>0 to +70 °C</td>
<td>SOIC–16</td>
<td>2500 Tape &amp; Reel</td>
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<tr>
<td>NE5517DR2G</td>
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<td>SOIC–16 (Pb–Free)</td>
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<td>PDIP–16</td>
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<td>NE5517NG</td>
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<td>PDIP–16</td>
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¹For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
**PDIP−16**

**CASE 648−08**

**ISSUE V**

**DATE 22 APR 2015**

**NOTES:**
2. CONTROLLING DIMENSION: INCHES.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

**STYLES:**

**STYLE 1:**
1. PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

**STYLE 2:**
1. PIN 1. COMMON DRAIN
2. COMMON DRAIN
3. COMMON DRAIN
4. COMMON DRAIN
5. COMMON DRAIN
6. COMMON DRAIN
7. COMMON DRAIN
8. COMMON DRAIN
9. GATE
10. GATE
11. GATE
12. GATE
13. SOURCE
14. SOURCE
15. SOURCE
16. SOURCE

**MARKING DIAGRAM**

- XXXXXXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot " *", may or may not be present.

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NOTE:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. Emitter
4. NO CONNECTION
5. BASE
6. Emitter
7. BASE
8. Emitter
9. BASE
10. Emitter
11. NO CONNECTION
12. Emitter
13. BASE
14. Emitter
15. BASE
16. Emitter

STYLE 2:
PIN 1. CONTACTOR
2. CARD
3. Emitter
4. NO CONNECTION
5. BASE
6. Emitter
7. BASE
8. Emitter
9. BASE
10. Emitter
11. NO CONNECTION
12. Emitter
13. BASE
14. Emitter
15. BASE
16. Emitter

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. COLLECTOR, #3
8. COLLECTOR, #4
9. BASE, #4
10. Emitter
11. NO CONNECTION
12. Emitter
13. BASE
14. Emitter
15. BASE
16. Emitter

STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. ANODE
11. NO CONNECTION
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. ANODE
11. NO CONNECTION
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE