

# NDD03N80Z

## N-Channel Power MOSFET

800 V, 4.5  $\Omega$

### Features

- ESD Diode-Protected Gate
- 100% Avalanche Tested
- 100% Rg Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V <sub>DSS</sub>	800	V
Continuous Drain Current R <sub>θJC</sub>	I <sub>D</sub>	2.9	A
Continuous Drain Current R <sub>θJC</sub> , T <sub>A</sub> = 100°C	I <sub>D</sub>	1.9	A
Pulsed Drain Current, V <sub>GS</sub> @ 10 V	I <sub>DM</sub>	12	A
Power Dissipation R <sub>θJC</sub>	P <sub>D</sub>	96	W
Gate-to-Source Voltage	V <sub>GS</sub>	±30	V
Single Pulse Avalanche Energy, I <sub>D</sub> = 2.5 A	E <sub>AS</sub>	100	mJ
ESD (HBM) (JESD22-A114)	V <sub>esd</sub>	2300	V
RMS Isolation Voltage (t = 0.3 sec., R.H. ≤ 30%, T <sub>A</sub> = 25°C)	V <sub>ISO</sub>	4500	V
Peak Diode Recovery (Note 1)	dv/dt	4.5	V/ns
Continuous Source Current (Body Diode)	I <sub>S</sub>	3.3	A
Maximum Temperature for Soldering Leads	T <sub>L</sub>	260	°C
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. I<sub>S</sub> = 3.3 A, di/dt ≤ 100 A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, T<sub>J</sub> = +150°C

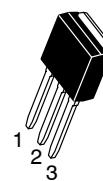
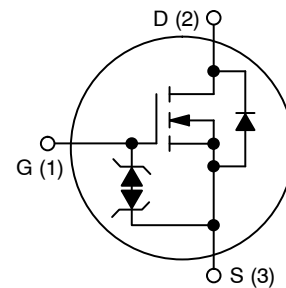


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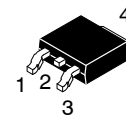
<http://onsemi.com>

V <sub>(BR)DSS</sub>	R <sub>DS(ON) MAX</sub>
800 V	4.5 $\Omega$ @ 10 V

### N-Channel



NDD03N80Z-1G  
IPAK  
CASE 369D



NDD03N80ZT4G  
DPAK  
CASE 369AA

### MARKING AND ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

# NDD03N80Z

## THERMAL RESISTANCE

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	1.3	°C/W
Junction-to-Ambient Steady State	$R_{\theta JA}$	33 96	

2. Insertion mounted
3. Surface mounted on FR4 board using 1" sq. pad size (Cu area = 1.127" sq [2 oz] including traces).

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	800			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	Reference to $25^\circ\text{C}$ , $I_D = 1\text{ mA}$		870		mV/°C
Drain-to-Source Leakage Current	$I_{DSS}$	$V_{DS} = 800\text{ V}, V_{GS} = 0\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		50	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$

### ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_D = 50\text{ }\mu\text{A}$	3.0	4.1	4.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	Reference to $25^\circ\text{C}$ , $I_D = 50\text{ }\mu\text{A}$		11		mV/°C
Static Drain-to-Source On Resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{ V}, I_D = 1.2\text{ A}$		3.7	4.5	$\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS} = 15\text{ V}, I_D = 1.2\text{ A}$		2.1		S

### DYNAMIC CHARACTERISTICS

Input Capacitance (Note 5)	$C_{iss}$	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		440		pF
Output Capacitance (Note 5)	$C_{oss}$			52		
Reverse Transfer Capacitance (Note 5)	$C_{rss}$			9.0		
Total Gate Charge (Note 5)	$Q_g$	$V_{DS} = 400\text{ V}, I_D = 3.3\text{ A}, V_{GS} = 10\text{ V}$		17		nC
Gate-to-Source Charge (Note 5)	$Q_{gs}$			3.5		
Gate-to-Drain ("Miller") Charge (Note 5)	$Q_{gd}$			9.1		
Plateau Voltage	$V_{GP}$			6.5		
Gate Resistance	$R_g$			5.5		$\Omega$

### RESISTIVE SWITCHING CHARACTERISTICS (Note 6)

Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 400\text{ V}, I_D = 3.3\text{ A}, V_{GS} = 10\text{ V}, R_G = 0\text{ }\Omega$		9.0		ns
Rise Time	$t_r$			7.0		
Turn-off Delay Time	$t_{d(off)}$			17		
Fall Time	$t_f$			9.0		

### SOURCE-DRAIN DIODE CHARACTERISTICS

Diode Forward Voltage	$V_{SD}$	$I_S = 3.0\text{ A}, V_{GS} = 0\text{ V}$	$T_J = 25^\circ\text{C}$		0.9	1.6	V
			$T_J = 100^\circ\text{C}$		0.8		
Reverse Recovery Time	$t_{rr}$	$V_{GS} = 0\text{ V}, V_{DD} = 30\text{ V}, I_S = 3.3\text{ A}, d_i/d_t = 100\text{ A}/\mu\text{s}$			360		ns
Charge Time	$t_a$				81		
Discharge Time	$t_b$				280		
Reverse Recovery Charge	$Q_{rr}$				1.3		

4. Pulse Width  $\leq 380\text{ }\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
5. Guaranteed by design.
6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

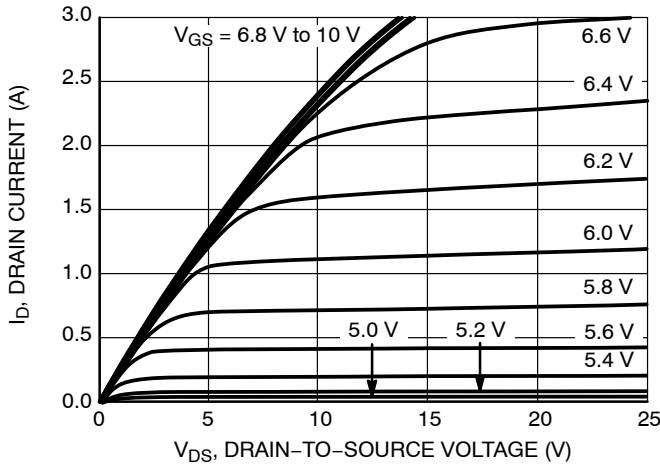


Figure 1. On-Region Characteristics

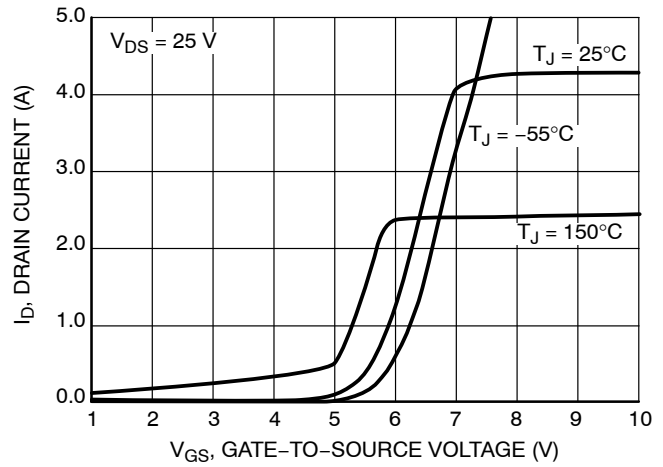


Figure 2. Transfer Characteristics

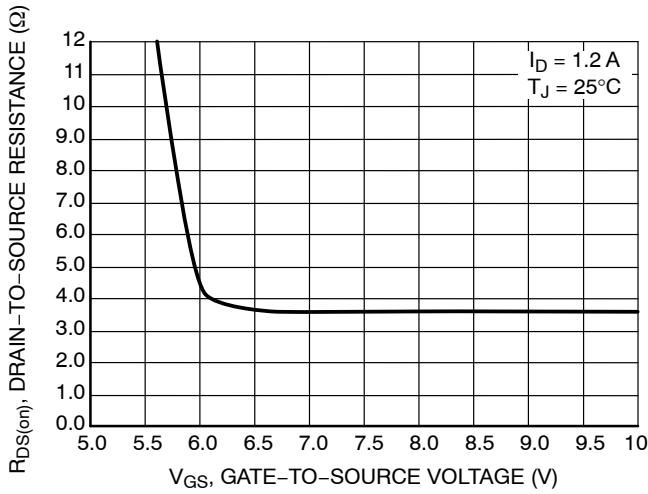


Figure 3. On-Region versus Gate-to-Source Voltage

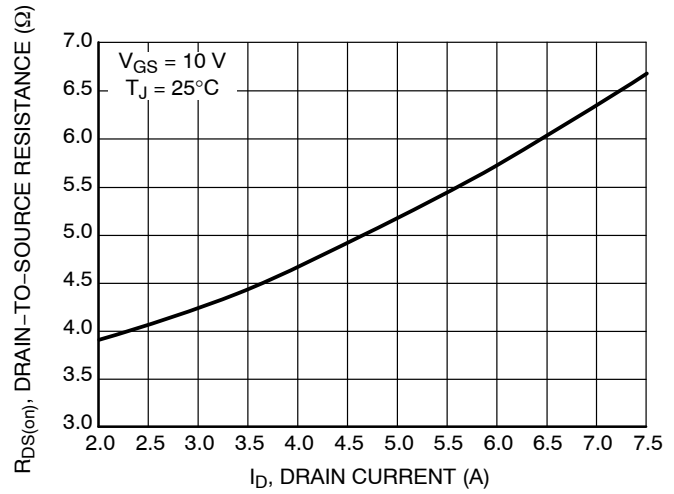


Figure 4. On-Resistance versus Drain Current and Gate Voltage

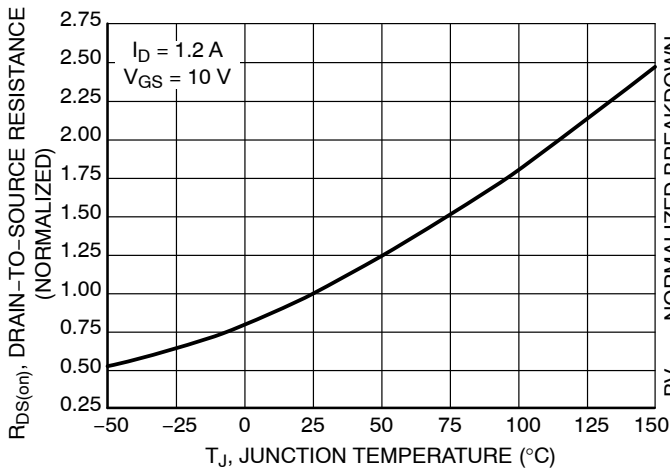


Figure 5. On-Resistance Variation with Temperature

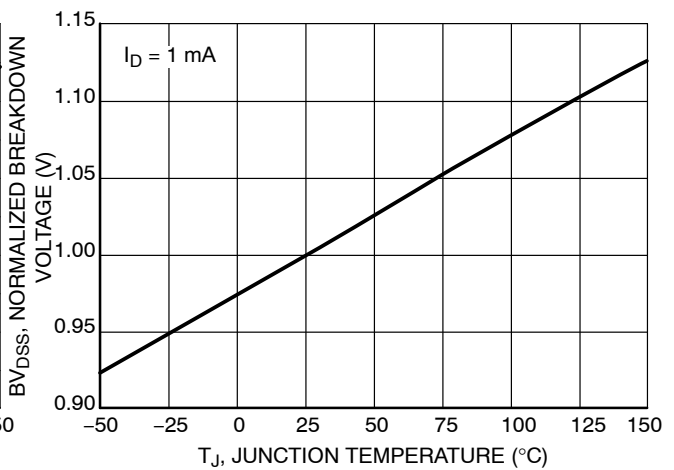


Figure 6. BV<sub>DSS</sub> Variation with Temperature

TYPICAL CHARACTERISTICS

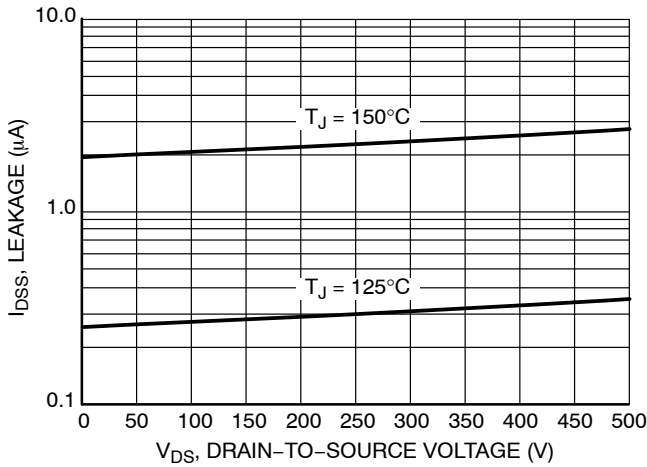


Figure 7. Drain-to-Source Leakage Current versus Voltage

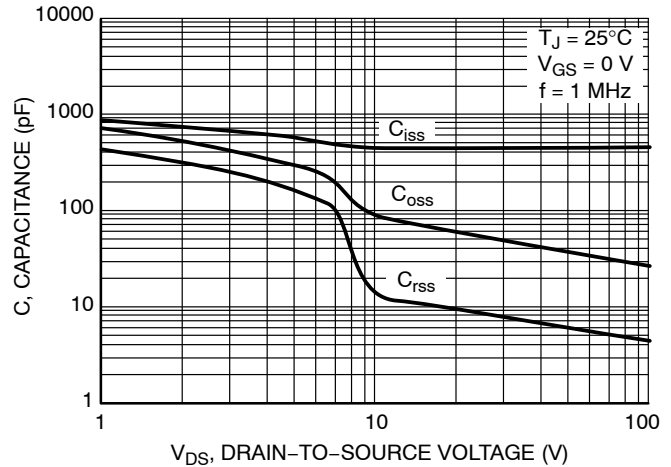


Figure 8. Capacitance Variation

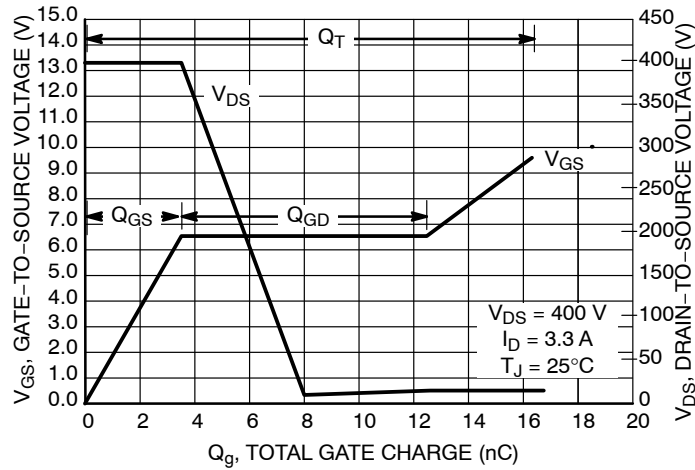


Figure 9. Gate-to-Source Voltage and Drain-to-Source Voltage versus Total Charge

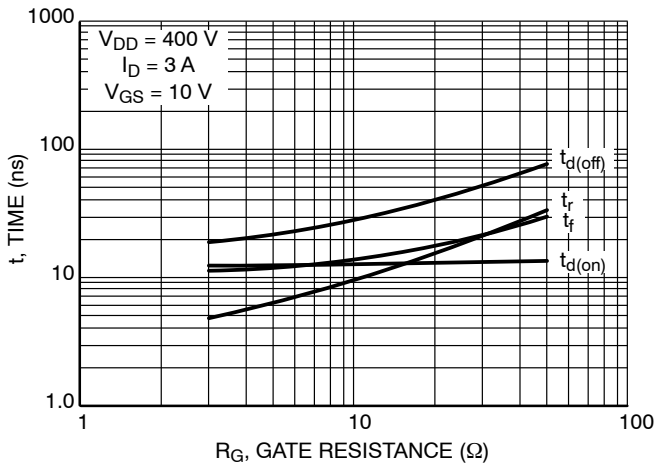


Figure 10. Resistive Switching Time Variation versus Gate Resistance

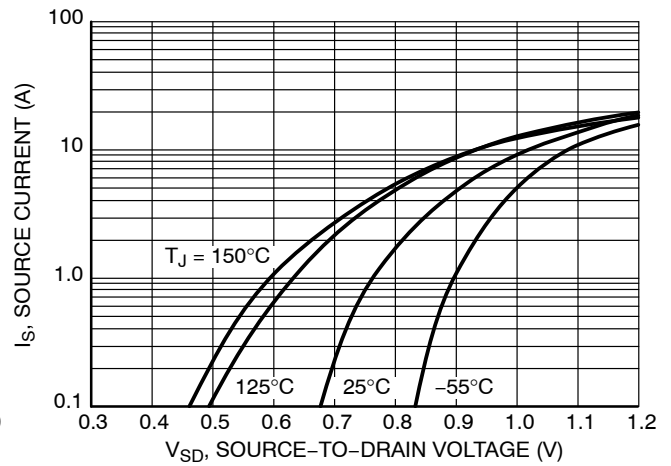
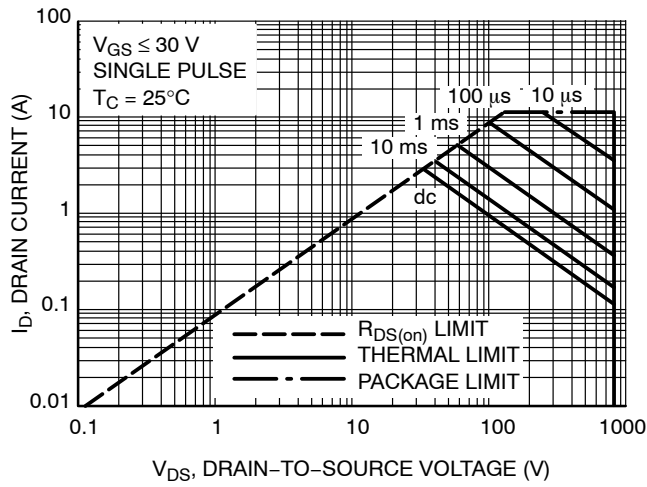


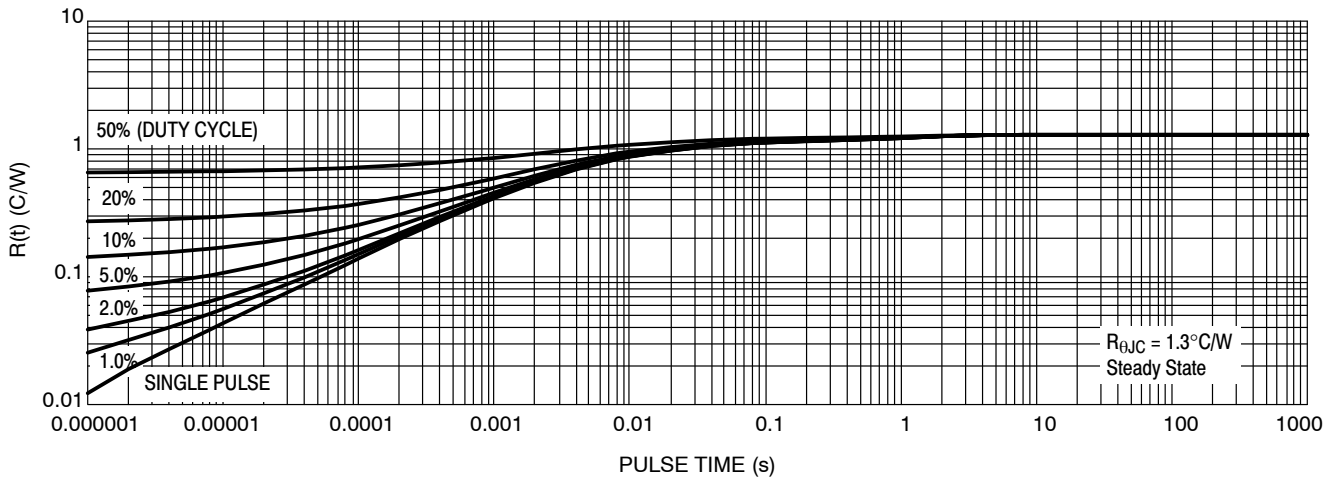
Figure 11. Diode Forward Voltage versus Current

# NDD03N80Z

## TYPICAL CHARACTERISTICS



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**



**Figure 13. Thermal Impedance (Junction-to-Case)**

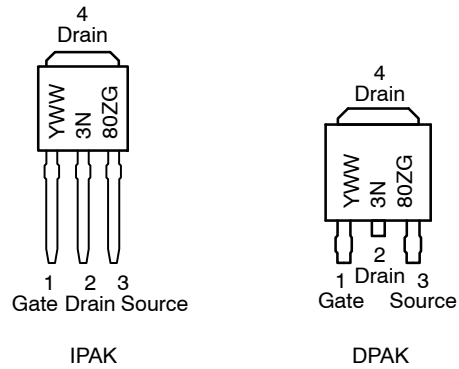
# NDD03N80Z

**Table 1. ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
NDD03N80Z-1G	IPAK (Pb-Free, Halogen-Free)	75 Units / Rail
NDD03N80ZT4G	DPAK (Pb-Free, Halogen-Free)	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## MARKING DIAGRAMS

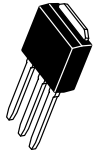


- A = Location Code
- Y = Year
- WW = Work Week
- G, H = Pb-Free, Halogen-Free Package

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

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### IPAK CASE 369D-01 ISSUE C

DATE 15 DEC 2010

SCALE 1:1



- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- |  |   |  |  |
|--|---|--|--|
| <p>STYLE 1:<br/>PIN 1. BASE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p>STYLE 2:<br/>PIN 1. GATE<br/>2. DRAIN<br/>3. SOURCE<br/>4. DRAIN</p> | <p>STYLE 3:<br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p>      | <p>STYLE 4:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. GATE<br/>4. ANODE</p> |
| <p>STYLE 5:<br/>PIN 1. GATE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p>         | <p>STYLE 6:<br/>PIN 1. MT1<br/>2. MT2<br/>3. GATE<br/>4. MT2</p>        | <p>STYLE 7:<br/>PIN 1. GATE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> |  |

### MARKING DIAGRAMS



- xxxxxxxxx = Device Code  
A = Assembly Location  
IL = Wafer Lot  
Y = Year  
WW = Work Week

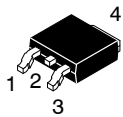
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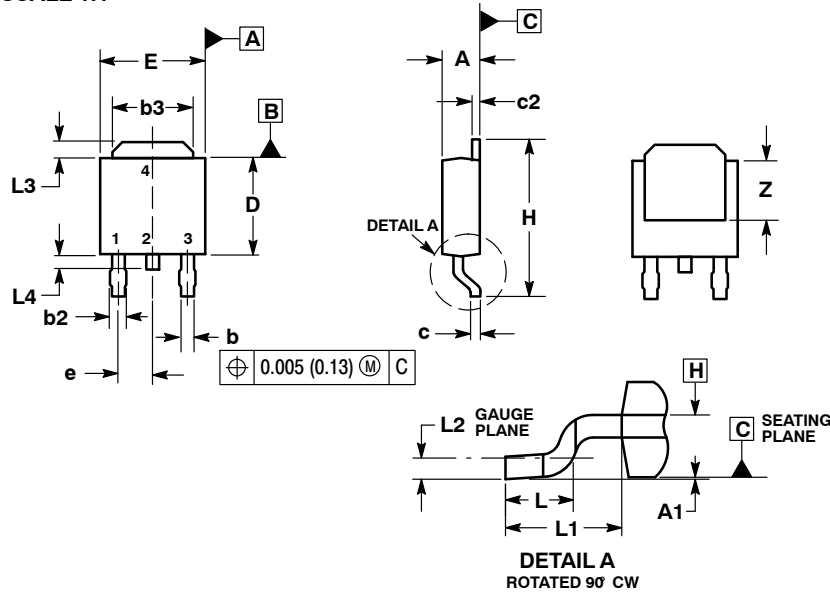
# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1



### DPAK (SINGLE GAUGE)

#### CASE 369AA-01

#### ISSUE B

DATE 03 JUN 2010

**NOTES:**

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: INCHES.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

- |   |  |   |   |
|---|--|---|---|
| <p><b>STYLE 1:</b><br/>PIN 1. BASE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p><b>STYLE 2:</b><br/>PIN 1. GATE<br/>2. DRAIN<br/>3. SOURCE<br/>4. DRAIN</p> | <p><b>STYLE 3:</b><br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p>      | <p><b>STYLE 4:</b><br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. GATE<br/>4. ANODE</p> |
| <p><b>STYLE 5:</b><br/>PIN 1. GATE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p>         | <p><b>STYLE 6:</b><br/>PIN 1. MT1<br/>2. MT2<br/>3. GATE<br/>4. MT2</p>        | <p><b>STYLE 7:</b><br/>PIN 1. GATE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> |   |

### GENERIC MARKING DIAGRAM\*



IC Discrete

- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.

### SOLDERING FOOTPRINT\*



SCALE 3:1 (mm/inches)

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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