NCV8855

Quad-Output Automotive System Power Supply IC with Integrated High-Side 2A Switch

The NCV8855 is a multiple output controller / regulator IC with an integrated high−side load switch. The NCV8855 addresses automotive radio system and instrument cluster power supply requirements. In addition to the high−side load switch, the NCV8855 includes a switch−mode power supply (SMPS) buck controller, a 2.5 A SMPS buck regulator and two low dropout (LDO) linear regulator controllers. The NCV8855 in combination with the ultra−low quiescent current NCV861x IC forms an eight−output automotive radio or instrument cluster power solution. The NCV8855 has an internally set switching frequency of 170 kHz, with a SYNC pin for external frequency synchronization.

The NCV8855 is intended to supply power to various loads, such as a tuner, CD logic, audio processor and CD / tape control within a car radio. The high−side switch can be used for a CD / tape mechanism or switching an electrically−powered antenna or display unit. In an instrument cluster application, the NCV8855 can be used to power graphics display, flash memory and CAN transceivers. In addition, the high−side switch can be used to limit power to a TFT display during a battery over−voltage condition.

Features

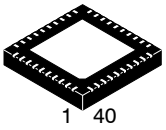
- < 1 μA Shutdown Current
- Meets ES−XW7T−1A278−AB Test Pulse G – Loaded Conditions
- V_{IN} Operating Range 9.0 to 18.0 V
- 1 SMPS Controller with Adjustable Current Limit
- 1 SMPS Regulator with Internal 300 mΩ NMOS Switch
- 2 LDO Controllers with Current Limit and Short Circuit Protection
- 1 High−side Load Switch with Internal 300 mΩ NMOS FET
- Adjustable Output Voltage for All Controllers / Regulators
- 800 mV, ±1% Reference Voltage
- System Enable Pin
- Single Enable Pin for Both LDO Controllers
- Independent Enable for High−side Load Switch
- Thermal Shutdown with Thermal Warning Indicator
- This is a Pb−Free Device

Applications

- Automotive Radio
- Instrument Cluster, Driver Information System (DIS)

ON Semiconductor®

http://onsemi.com



40 PIN QFN, 6x6
MN SUFFIX
CASE 488AR

MARKING DIAGRAM

A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCV8855BMNR2G	QFN−40 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

TYPICAL APPLICATION SCHEMATIC SHOWING DETAILED BLOCK DIAGRAM

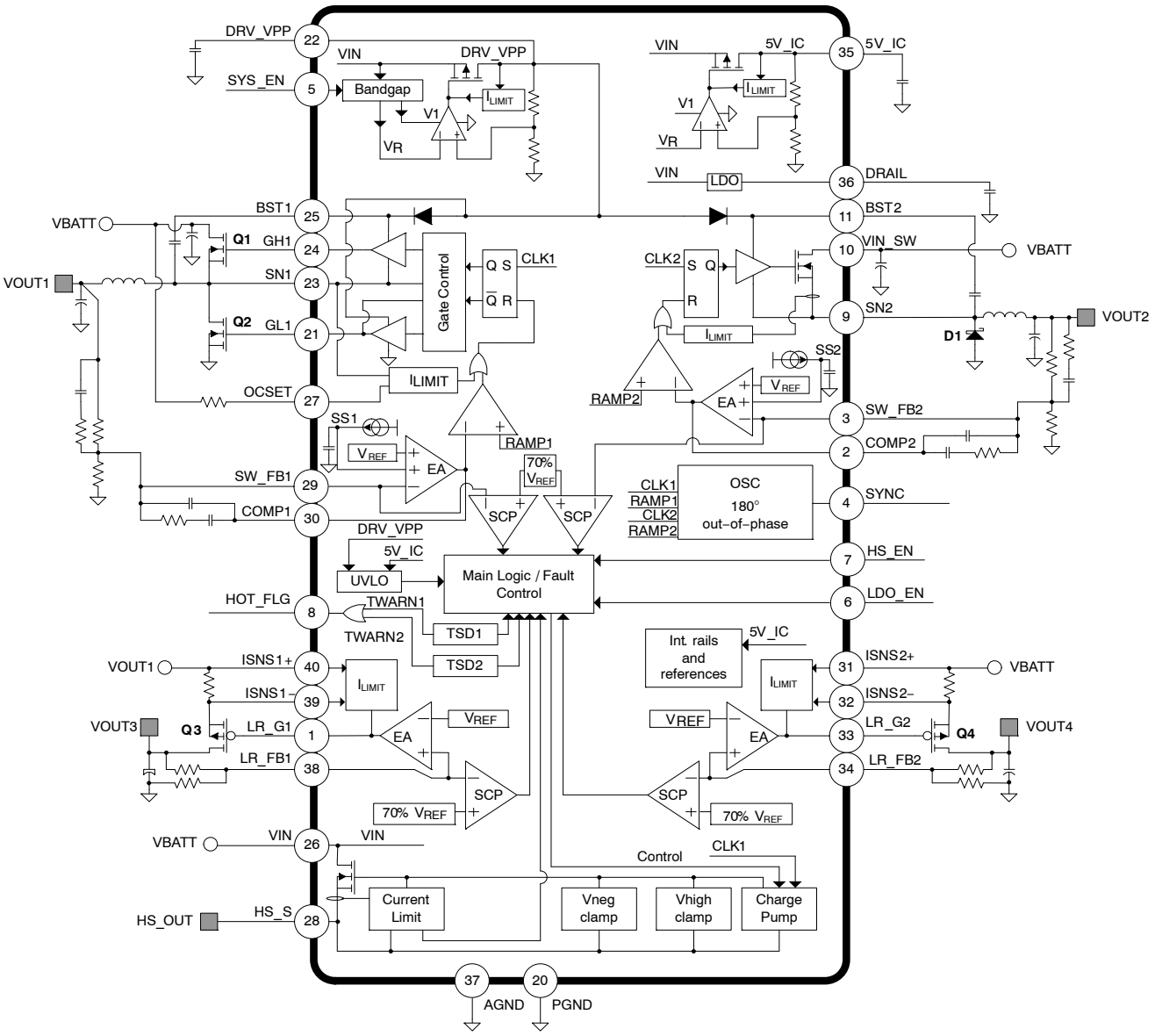


Figure 1. Application Schematic / Block Diagram

Components	Part Number	Value	Manufacturer
D1	MBRS4201T3	200 V, 4 A, Schottky, 0.61 V Vf, SMC	ON Semiconductor
Q1, Q2	NTD24N06	60 V, N type MOSFET, 32 mΩ , DPAK	ON Semiconductor
Q3, Q4	NTD20P06LT4G	−60V, P type MOSFET, 130 mΩ, DPAK	ON Semiconductor

PIN FUNCTION DESCRIPTIONS

Pin No.	Symbol	Description
5	SYS_EN	Main enable pin for the IC. A logic high on this pin will enable the part. Leaving this pin floating or driving it to ground will place the IC in shutdown mode.
6	LDO_EN	Enable pin for both LDO controllers. A logic high on this pin will enable both LDO controllers. If this pin is left floating, an internal pull down keeps the LDOs disabled.
7	HS_EN	Enable pin for the high−side load switch. A logic high on this pin will enable the HSS. If this pin is left floating, an internal pull down keeps the HSS disabled.
8	HOT_FLG	Thermal warning indicator. This pin provides an early warning signal of an impending thermal shutdown.
22	DRV_VPP	Output of the internal 7.2 V linear regulator. Bypass this pin with 1 μF to ground.
35	5V_IC	Output of the internal 5 V linear regulator. Bypass this pin with 0.1 μF to ground.
36	DRAIL	Output of the internal 4.2 V linear regulator. Bypass this pin with 0.1 μF to ground.
4	SYNC	Synchronization pin. Use this pin to synchronize the internal oscillator to an external clock. If synchronization is not used, connect this pin to AGND.
37	AGND	Analog ground. Reference point for internal signals.
SWITCH−MODE POWER SUPPLY 1 (SMPS1) PIN CONNECTIONS		
27	OCSET	Overcurrent set pin, used to set the current limit threshold. A resistor connected from this pin and the upper MOSFET Drain sets the current limit protection level.
29	SW_FB1	Output voltage feedback pin. Connect a resistor divider network to VOUT1 to set the desired output voltage.
30	COMP1	This pin is the output of the error amplifier and the non-inverting input of the PWM comparator. Use this pin in conjunction with the SW_FB1 pin to compensate the voltage-mode control feedback loop.
25	BST1	This pin is the supply rail for the upper N−Channel MOSFET. An internal bootstrap diode brings DRV_VPP to this pin. Connect a ceramic capacitor (C_{BST1}) between this pin and the SN1 pin. A typical value for C_{BST1} is 0.1 μF.
24	GH1	GH1 is the output pin of the internal upper N−Channel MOSFET gate driver. Keep the trace from this pin to the gate of the upper MOSFET as short as possible to achieve the best turn−on and turn−off performance and to reduce electro−magnetic emissions.
23	SN1	This pin is the return path of the upper floating gate driver. Connect this pin to the source of the upper MOSFET. This pin is also used to sense the current flowing through the upper MOSFETs.
21	GL1	GL1 is the output pin of the synchronous rectifier gate driver. Connect this pin to the lower N−channel MOSFET.
20	PGND	This pin is the return path for SMPS1 lower MOSFET driver current. Connect this pin to the source of the lower MOSFET.
PINS NOT INTERNALLY CONNECTED TO SILICON		
EP	−	Exposed pad of QFN package. Connect to printed circuit board ground to improve thermal performance.
12 thru 19		These pins can be left floating or tied to ground to improve thermal performance.
SWITCH−MODE POWER SUPPLY 2 (SMPS2) PIN CONNECTIONS		
10	VIN_SW	This pin is the supply rail for the internal upper N−Channel MOSFET. Bypass this pin with a local ceramic capacitor. Additional bulk capacitance may be required based off output requirements. Refer to application section for more information.
3	SW_FB2	Output voltage feedback pin. Connect a resistor divider network to VOUT2 to set the desired output voltage.
2	COMP2	This pin is the output of the error amplifier and the non−inverting input of the PWM comparator. Use this pin in conjunction with the SW_FB2 pin to compensate the voltage−controlled feedback loop.
11	BST2	This pin is the supply rail for the internal upper N−Channel MOSFET. An internal bootstrap diode brings DRV_VPP to this pin. Connect a ceramic capacitor (C_{BST2}) between this pin and the SN2 pin. A typical value for C_{BST2} is 0.1 μF.
9	SN2	Source output of the internal upper N−channel MOSFET.

PIN FUNCTION DESCRIPTIONS

Pin No.	Symbol	Description
LOW DROPOUT LINEAR REGULATOR CONTROLLER 1 (LDO1) PIN CONNECTIONS		
38	LR_FB1	LDO controller output voltage feedback pin. Connect a resistor divider network to VOUT3 to set the desired output voltage.
1	LR_G1	Error amplifier output of the LDO controller. Connect to gate of P−Channel MOSFET pass element.
40	ISNS1+	Current sense positive input. Connect this pin to the supply side of the current sense resistor. This pin also serves as the supply rail for the linear regulator controller. A local bypass capacitor with a value of 0.1 μF to 1 μF is recommended.
39	ISNS1−	Current sense negative input. When using a current sense resistor, connect this pin to the pass element side of the current sense resistor. If current limit is not used, connect this pin to the supply rail of the pass element.
LOW DROPOUT LINEAR REGULATOR CONTROLLER 2 (LDO2) PIN CONNECTIONS		
34	LR_FB2	LDO controller output voltage feedback pin. Connect a resistor divider network to VOUT3 to set the desired output voltage.
33	LR_G2	Error amplifier output of the LDO controller. Connect to gate of P−Channel MOSFET pass element.
31	ISNS2+	Current sense positive input. Connect this pin to the supply side of the current sense resistor. This pin also serves as the supply rail for the linear regulator controller. A local bypass capacitor with a value of 0.1 μF to 1 μF is recommended.
32	ISNS2−	Current sense negative input. When using a current sense resistor, connect this pin to the pass element side of the current sense resistor. If current limit is not used, connect this pin to the supply rail of the pass element.
HIGH−SIDE LOAD SWITCH (HSS) PIN CONNECTIONS		
26	VIN	This pin is the supply rail for the internal high−side load switch, DRV_VPP and 5V_IC. Bypass this pin with a 1 μF ceramic capacitor.
28	HS_S	Source node output of the internal high−side N−Channel MOSFET load switch.

MAXIMUM RATINGS (Voltages are with respect to AGND unless noted otherwise)

Pin Name	Value	Unit
Max dc voltage (GH1, BST1, SN1, SN2, BST2, HS_S)	−0.3 to 30	V
Negative Transient (t < 50 ns) (SN1, SN2)	−2	V
Max dc voltage: 5V_IC	6	V
Max dc voltage: DRV_VPP	9	V
Max dc voltage (BST1 & GH1w/respect to SN1, GL1, BST2 w/respect to SN2)	−0.3 to 15	V
Max dc voltage (OCSET, ISNS1+, ISNS1−, LR_G1, VIN, VIN_SW, ISNS2+, ISNS2−, LR_G2)	−0.3 to 40	V
Peak Transient (ES−XW7T−1A278−AB Test Pulse G − Loaded Conditions) (OCSET, ISNS1+, ISNS1−, LR_G1, VIN, VIN_SW, ISNS2+, ISNS2−, LR_G2)	−0.3 to 45	V
Max dc voltage (SW_FB1, COMP1, LR_FB1, LDO_EN, HOT_FLG, SW_FB2, COMP2, LR_FB2, HS_EN, SYS_EN, SYNC)	−0.3 to 7	V
Max dc voltage: PGND	−0.3 to 0.3	V
Maximum Operating Junction Temperature Range, T_J	−40 to 150	°C
Maximum Storage Temperature Range, T_{STG}	−55 to +150	°C
Peak Reflow Soldering Temperature: Pb−Free 60 to 150 seconds at 217°C	260 peak	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ATTRIBUTES

Description	Symbol	Value	Unit
Thermal Characteristic $R_{\theta JA}$ generated from 1 sq in / 1 oz copper 1 sided PCB	$R_{\theta JA}$	36	°C/W
	$R_{\theta JC}$	3	°C/W
ESD Capability Human Body Model (SN1, SN2) Human Body Model (All Others) Machine Model		 1 2 150	 kV kV V
Moisture Sensitivity Level	MSL	1	

RECOMMENDED OPERATING CONDITIONS

Description	Value
VBATT range (refer to Figure 1)	9 V to 18 V
Ambient Temperature range	−40°C to 105°C

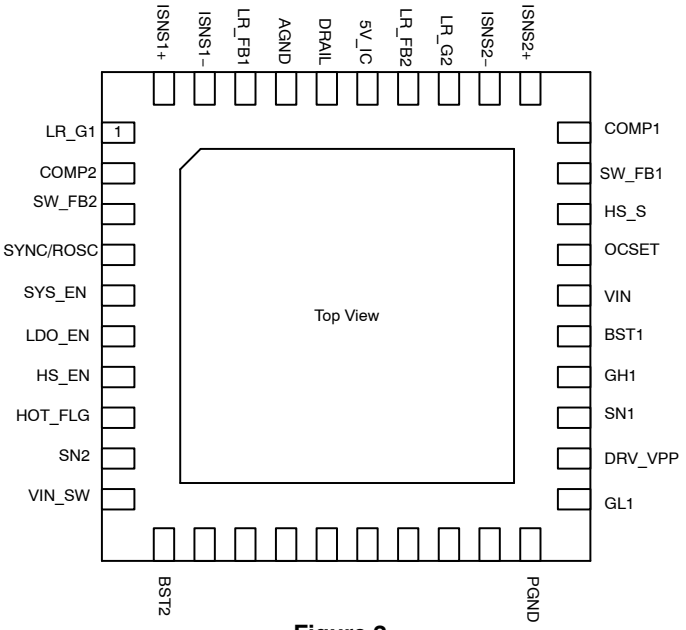


Figure 2.

ELECTRICAL CHARACTERISTICS ($V_{IN\_SW} = V_{IN} = V_{ISNS1+} = V_{ISNS1-} = V_{ISNS2+} = V_{ISNS2-}$ = 13.2 V, SYS_EN = LDO_EN = HS_EN = 5 V, VOUT3 = 3.3 V, VOUT4 = 8.5 V, IOUT[1:4] = 0 A) Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 150°C unless noted otherwise. Min/Max values are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SUPPLY VOLTAGES AND SYSTEM SPECIFICATION						
Supply Current and Operating Voltage Range						
VIN_SW quiescent current		No Switching, V_{SW_FB2} = 1V, SN2 = PGND1, T_J = 25°C[1]		175		μA
VIN_SW shutdown current		SYS_EN = 0 V, T_J = 25°C		100	500	nA
High VIN detect voltage	V_{OVP}	VIN rising	18	18.5	19	V
High VIN detect hysteresis		VIN falling	0.2	0.6	1	
VIN quiescent current		T_J = 25°C		4		mA
VIN shutdown current		SYS_EN = 0 V, T_J = 25°C		100	500	nA

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SUPPLY VOLTAGES AND SYSTEM SPECIFICATION						
Internal Voltage Reference						
Internal voltage reference range	V_{REF}	T_J = 25°C −40°C ≤ T_J ≤ 150°C	0.792 0.784	0.8	0.808 0.816	V
Internal Linear Regulator 5 V Supply Rail						
5V_IC UVLO threshold voltage		V_{5V_IC} rising	4.00	4.35	4.70	V
5V_IC UVLO hysteresis		V_{5V_IC} falling	100	150	300	mV
Voltage range		No load	4.8	5	5.2	V
Current limit			10	21	50	mA
Load regulation		1mA ≤ I_{5V_IC} ≤ 10 mA			50	mV
Line regulation		I_{5V_IC} = 5 mA, 9 V ≤ VIN ≤ 18 V			100	mV
Internal DRV_VPP Supply Rail						
DRV_VPP UVLO threshold voltage		V_{DRV_VPP} rising	4.00	4.35	4.70	V
DRV_VPP UVLO hysteresis		V_{DRV_VPP} falling	100	150	300	mV
Voltage range	V_{DRV_VPP}	No load	6.9	7.1	7.3	V
Current limit			30	67	110	mA
Load regulation		1 mA ≤ I_{DRV_VPP} ≤ 25 mA			50	mV
Line regulation		I_{DRV_VPP} = 1 mA, 9 V ≤ VIN ≤ 18 V			200	mV
Dropout voltage		I_{DRV_VPP} = 25 mA, ΔV_{DRV_VPP} = 2 %			400	mV
Oscillator						
Oscillator frequency	f_{SW}		154.7	170	185.3	kHz
SYNC						
Logic high					2.0	V
Logic low			0.8			V
Pull down current		V_{SYNC} = 5 V V_{SYNC} = 0.8 V	 2	5 5	10	μA
Leakage current		SYS_EN = 0 V, V_{SYNC} = 5 V		100	500	nA
Clock synchronization range			190		255	kHz
Synchronization delay to SMPS1		From falling SYNC edge	200		400	ns
Synchronization delay to SMPS2		From rising SYNC edge	200		400	ns
Minimum SYNC pulse width (HIGH)		SMPS1 synchronizing			50	ns
Minimum SYNC pulse width (LOW)		SMPS2 synchronizing			50	ns
Thermal Monitoring (T_{MON_HSS}, High−side junction temperature monitor)						
Thermal warning temperature	T_{WARN1}		140	150	160	°C
T_{WARN1} hysteresis			10		20	°C
Thermal shutdown temperature	TSD1		160	170	180	°C
Delta junction temperature (TSD1−T_{WARN1})			10	20	30	°C
Thermal Monitoring (T_{MON_SW}, SMPS2 internal MOSFET temperature monitor)						
Thermal warning temperature	T_{WARN2}		140	150	160	°C

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SUPPLY VOLTAGES AND SYSTEM SPECIFICATION						
Thermal Monitoring (T_{MON_SW}, SMPS2 internal MOSFET temperature monitor)						
T_{WARN2} hysteresis			10		20	°C
Thermal shutdown temperature	TSD2		160	170	180	°C
Delta junction temperature (TSD2−T_{WARN2})			10	20	30	°C
HOT_FLG						
Voltage low threshold		T_J > TWARN[x], 1 kΩ pullup to 5 V			0.4	V
Leakage current		1 kΩ pull−up to 5 V, T_J = 25°C		100	500	nA
Sink capability		V_{HOT_FLG} = 0.8 V	4.6			mA
System Enable						
Logic high			2.0			V
Logic low					0.8	V
Pull down resistance		T_J = 25°C		500		kΩ
High−Side Enable						
HS_EN logic high					2.0	V
HS_EN logic low			0.8			V
Pull down current		V_{HS_EN} = 5 V V_{HS_EN} = 0.8 V	 2	5 5	10	μA
Leakage current	I_{HS_EN}	SYS_EN = 0 V, V_{HS_EN} = 5 V		100	500	nA
LDO Enable						
Logic high					2.0	V
Logic low			0.8			V
Pull down current		V_{LDO_EN} = 5 V V_{LDO_EN} = 0.8 V	 2	5 5	10	μA
Leakage current	I_{LDO_EN}	SYS_EN = 0 V, V_{LDO_EN} = 5 V		100	500	nA
SWITCH−MODE POWER SUPPLY CONTROLLER (SMPS1, VOUT1) SPECIFICATIONS						
Over Current Protection						
OCSET current sink		R_{OCSET} = 10 kΩ connected to 13.2 V	45	55	65	μA
OCSET leakage current		SYS_EN = 0 V, V_{OCSET} = 13.2 V, T_J = 25°C		100	500	nA
OCSET comparator differential range		(Note 1)	50		750	mV
OCSET comparator common−mode range		(Note 1)	4.0		19	V
Current limit response time		From rising edge of SN1	100	200	275	ns
Short circuit threshold voltage	SCTH1	V_{SW_FB1} % of V_{REF}	75	80	85	%
Short circuit protection startup delay		From SYS_EN rising edge, % of t_{SS1}, SW_FB1 = 0.5 V, (Note 2)	100	125	150	%
Internal Soft−Start						
Soft−start time	t_{SS1}		3	5	7	ms

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SWITCH−MODE POWER SUPPLY CONTROLLER (SMPS1, VOUT1) SPECIFICATIONS						
Error Amplifier						
Dc gain		(Note 1)	70	85		dB
Gain−bandwidth product		(Note 1)	8	10		MHz
SW_FB1 input bias current		SW_FB1 = 0.8 V			100	nA
Input offset voltage		(Note 1)			800	μV
Slew rate		C_{COMP1} = 50 pF, ±1 mA dc load Slew rate within ramp voltage levels (Note 1)	6	8		V/μs
COMP1 source current		V_{COMP1} = 2.2 V	1.5		8	mA
		V_{COMP1} = 3.2 V	1.6		8	mA
COMP1 sink current		V_{COMP1} = 2.2 V	1.1		8	mA
		V_{COMP1} = 1.1 V	0.7		8	mA
Minimum COMP1 voltage		I_{COMP1} = 500 μA			1.05	V
Maximum COMP1 voltage		I_{COMP1} = 2 mA	3.3			V
Ramp maximum voltage			2.8	3.0	3.2	V
Ramp minimum voltage			1.1	1.2	1.3	V
Ramp voltage amplitude	V_{RAMP1}		1.6	1.8	2.0	V
Duty Cycle Limitations						
Minimum off time	$t_{MINOFF1}$	GH1 falling to GL1 rising	80	140	200	ns
Minimum pulse width	t_{MINON1}	GH1 rising to GH1 falling	120	250	300	ns
Gate Driver						
GH1 source current		$V_{GH1} - V_{SN1}$ = 4 V, T_J = 25°C		1.5		A
GH1 sink current		$V_{GH1} - V_{SN1}$ = 2 V, T_J = 25°C		1.5		A
GL1 source current		V_{GL1} − PGND = 4 V, T_J = 25°C		1.5		A
GL1 sink current		V_{GL1} − PGND = 1 V, T_J = 25°C		1.5		A
SN1 falling to GL1 rising, non−overlap time	t_{NOLT}			30	70	ns
GL1 falling to GH1 rising, non−overlap time				30	70	ns
SN1 falling non−overlap threshold voltage			1.0	1.8	3.0	V
GL1 falling non−overlap threshold voltage				2		V
SN1 falling override timer			50	100	150	ns
SWITCH−MODE POWER SUPPLY REGULATOR (SMPS2, VOUT2) SPECIFICATIONS						
Over Current Protection						
Internal current limit			2.5	3.05	4.2	A
Current limit blanking time			100		200	ns
Short circuit threshold voltage	SCTH2	V_{SW_FB2} % of V_{REF}	75	85	95	%
Short circuit protection startup delay		From SYS_EN rising edge, % of t_{SS2}, SW_FB2 = 0.5 V	100	125	150	%

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SWITCH−MODE POWER SUPPLY REGULATOR (SMPS2, VOUT2) SPECIFICATIONS						
Internal Soft−start						
Soft−start time	t_{SS2}	SYNC floating	3	5	7	ms
Error Amplifier						
Dc gain		(Note 1)	70	85		dB
Gain−bandwidth product		(Note 1)	8	10		MHz
SW_FB2 input bias current		SW_FB2 = 0.8 V		100	500	nA
Input offset voltage					800	μV
Slew rate		C_{COMP2} = 50 pF, ±1 mA dc load Slew rate within ramp voltage levels (Note 1)	6	8		V/μs
COMP2 source current		V_{COMP2} = 2.2 V	1.5		8	mA
		V_{COMP2} = 3.2 V	1.6		8	mA
COMP2 sink current		V_{COMP2} = 2.2 V	1.1		8	mA
		V_{COMP2} = 1.1 V	0.7		8	mA
Minimum COMP2 voltage		I_{COMP2} = 500 μA			1.05	V
Maximum COMP2 voltage		I_{COMP2} = 2 mA	3.3			V
Ramp maximum voltage			2.8	3.0	3.2	V
Ramp minimum voltage			1.1	1.2	1.3	V
Ramp voltage amplitude	V_{RAMP2}		1.6	1.8	2.0	V
Duty Cycle Limitations						
Minimum off time	$t_{MINOFF2}$	SN2 falling to SN2 rising	80	140	200	ns
Minimum pulse width	t_{MINON2}	SN2 rising to SN2 falling,	120	250	300	ns
Switching MOSFET						
N−channel MOSFET $R_{DS(on)}$		T_J = 25°C, Guaranteed at Probe		300	360	mΩ
Turn−on time		SN2 → 0 V to 13.2 V, IOUT = 1 A (inductive load), T_J = 25°C		30		ns
Turn−off time		SN2 → 13.2 V to 0 V, IOUT = 1 A (inductive load), T_J = 25°C		30		ns
LOW DROPOUT LINEAR REGULATOR CONTROLLER (LDO1, VOUT3) SPECIFICATIONS						
Output Voltage Regulation						
Output voltage accuracy		V_{LR_FB1} tied to VOUT3 directly, NTD20P06L pass device	−2		2	%
Output voltage line regulation		IOUT3 = 10 mA, 4.5 V ≤ V_{ISNS1+} ≤ 5.5 V, NTD20P06L pass device	−0.25	0.01	0.25	%
Output voltage load regulation		1 mA ≤ IOUT3 ≤ 500 mA, V_{ISNS1+} = 5 V, NTD20P06L pass device	−0.5	0.2	0.5	%
Output load capacitance range	C_{OUT3}	(Note 1)	10		100	μF
Output load capacitance ESR range		(Note 1)	0.01		5	Ω
Power supply ripple rejection	PSRR1	NTD20P06L pass device (Note 1)		60		dB
Current Limit						
Current limit threshold voltage	V_{SNS1}	$V_{ISNS1+} - V_{ISNS1-}$	90	110	130	mV

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LOW DROPOUT LINEAR REGULATOR CONTROLLER (LDO1, VOUT3) SPECIFICATIONS						
Current Limit						
ISNS1+ leakage current	I_{ISNS1+}	SYS_EN = 0, T_J = 25°C, V_{ISNS1+} = 13.2 V		100	500	nA
ISNS1− leakage current	I_{ISNS1-}	SYS_EN = 0, T_J = 25°C, V_{ISNS1-} = 13.2 V		100	500	nA
Short circuit threshold voltage		V_{LR_FB1} % of V_{REF}	60	70	80	%
Short circuit blanking time		From rising edge of LDO_EN	10	12	14	ms
Error Amplifier						
Feedback bias current		LR_FB1 = 0.5 V		100	500	nA
Maximum $\|V_{GS}\|$		2 mA, internally clamped	10	11.7	13.5	V
LOW DROPOUT LINEAR REGULATOR CONTROLLER (LDO2, VOUT4) SPECIFICATIONS						
Output Voltage Regulation						
Output voltage accuracy		V_{LR_FB2} tied to VOUT4 directly, NTD20P06L pass device	− 2		2	%
Output voltage line regulation		IOUT4 = 10 mA, 9 V ≤ V_{ISNS2+} ≤ 18 V, NTD20P06L pass device	−0.25	0.01	0.25	%
Output voltage load regulation		1 mA ≤ IOUT4 ≤ 500 mA, NTD20P06L pass device	−0.5	0.2	0.5	%
Output load capacitance range	C_{OUT4}	(Note 1)	10		100	μF
Output load capacitance ESR range		(Note 1)	0.01		5	Ω
Power supply ripple rejection	PSRR2	NTD20P06L pass device (Note 1)		60		dB
Current Limit						
Current limit threshold voltage	V_{SNS2}	$V_{ISNS2+} - V_{ISNS2-}$	90	110	130	mV
ISNS2+ leakage current	I_{ISNS2+}	SYS_EN = 0, T_J = 25°C, V_{ISNS2+} = 13.2 V		100	500	nA
ISNS2− leakage current	I_{ISNS2-}	SYS_EN = 0, T_J = 25°C, V_{ISNS2-} = 13.2 V		100	500	nA
Short circuit threshold voltage		V_{LR_FB2} % of V_{REF}	60	70	80	%
Short circuit blanking time		From rising edge of LDO_EN	10	12	14	ms
Error Amplifier						
Feedback bias current		LR_FB2 = 0.5 V		100	500	nA
Maximum $\|V_{GS}\|$		2 mA, internally clamped	10	11.7	13.5	V
High−side Load Switch (HSS)						
Current Limit						
Peak current limit	I_{HSSLIM}		2.00	2.80	3.64	A
Short circuit timeout	t_{SCP}		1.300	1.506	1.800	ms
Short circuit threshold voltage	$V_{SCP(HS\_S)}$		4.0	4.5	5.0	V
Current overload threshold voltage	V_{DS}	$V_{IN} - V_{HS\_S}$	3.3	3.95	4.6	V
Current overload timeout			2.600	3.012	3.600	ms
Voltage Clamp						
Source output positive clamping voltage	V_{CLAMP+}	1 mA ≤ I_{HS_S} ≤ 2 A V_{CLAMP+} ≤ V_{IN} ≤ V_{OVP}	15.4	16.0	16.6	V
Source output negative clamping voltage	V_{CLAMP-}	I_{LOADSW} = 50 mA	−1.6			V

1. Guaranteed by design, not fully tested in production.
2. Indirectly guaranteed by test coverage of other parameters.

ELECTRICAL CHARACTERISTICS (V_{IN_SW} = V_{IN} = V_{ISNS1+} = V_{ISNS1-} = V_{ISNS2+} = V_{ISNS2-} = 13.2 V, SYS_EN = LDO_EN = HS_EN = 5 V, VOUT3 = 3.3 V, VOUT4 = 8.5 V, IOUT[1:4] = 0 A) Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 150°C unless noted otherwise. Min/Max values are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High−side Load Switch (HSS)						
MOSFET						
HSS $R_{DS(on)}$		$V_{GS(HSS)}$ = 8 V		233	442	mΩ
HSS dropout voltage		I_{HS_S} = 1 A		233	442	mV
Turn On/Off						
Turn on time (resistive load)		R_{HS_S} = 6.6 Ω, 90% VIN	40	80	120	μs
Turn off time		R_{HS_S} = 6.6 Ω, 10% VIN	50	125	200	μs

1. Guaranteed by design, not fully tested in production.
2. Indirectly guaranteed by test coverage of other parameters.

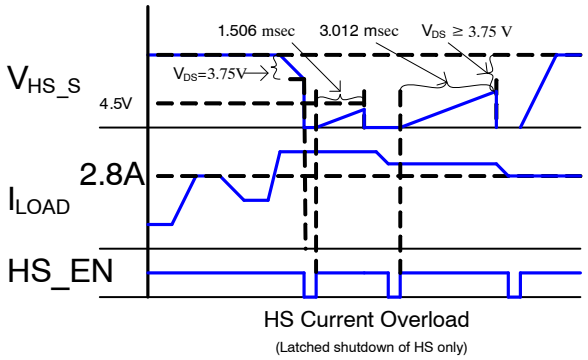


Figure 3.

TYPICAL PERFORMANCE CHARACTERISTICS

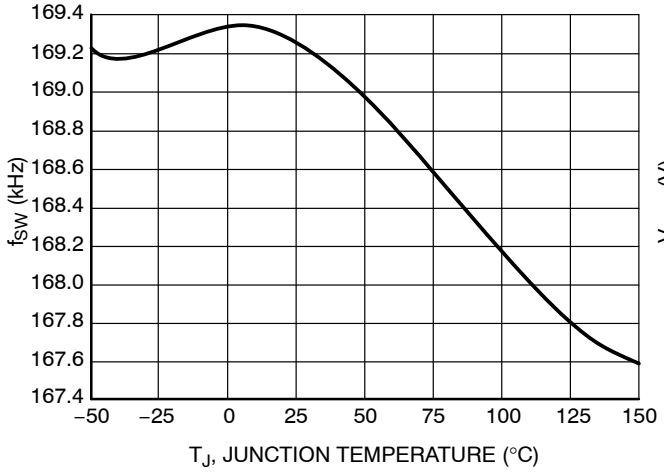


Figure 4. Switching Frequency vs. Junction Temperature

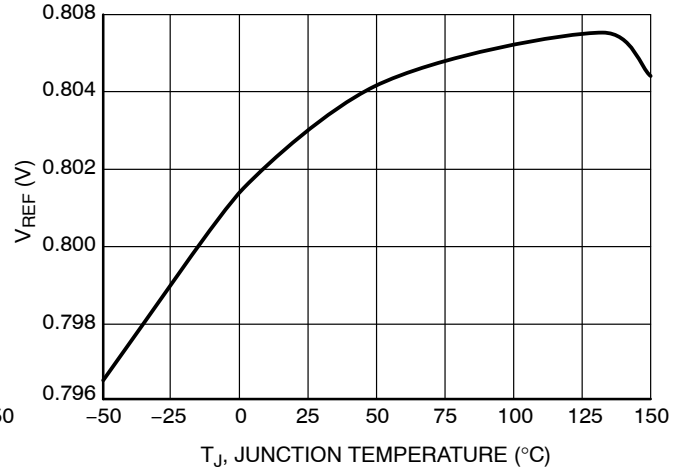


Figure 5. Reference Voltage vs. Junction Temperature

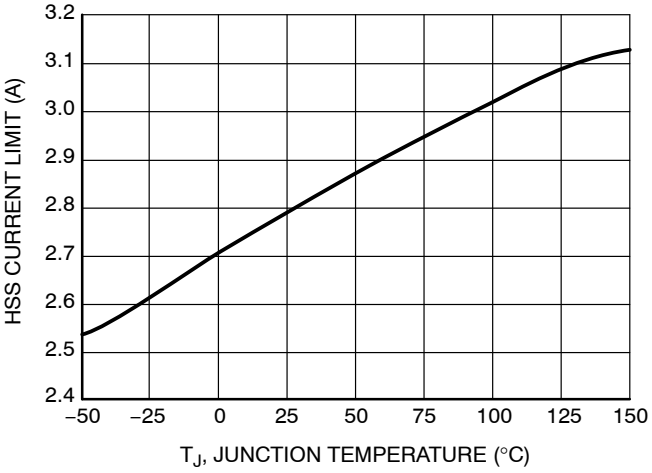


Figure 6. HSS Current Limit vs. Junction Temperature

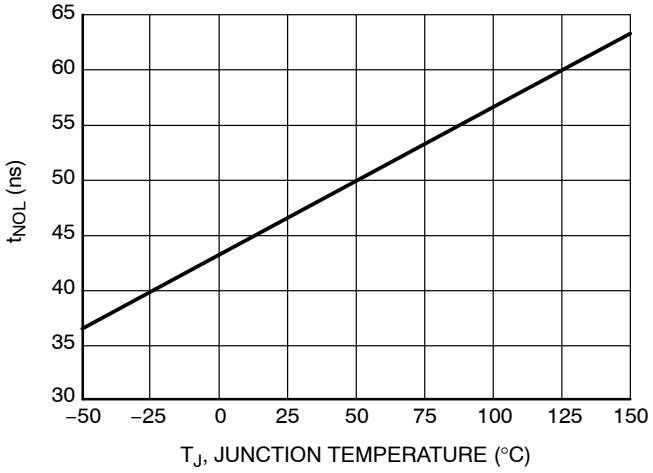


Figure 7. SMPS1 Non−Overlap Time vs. Junction Temperature

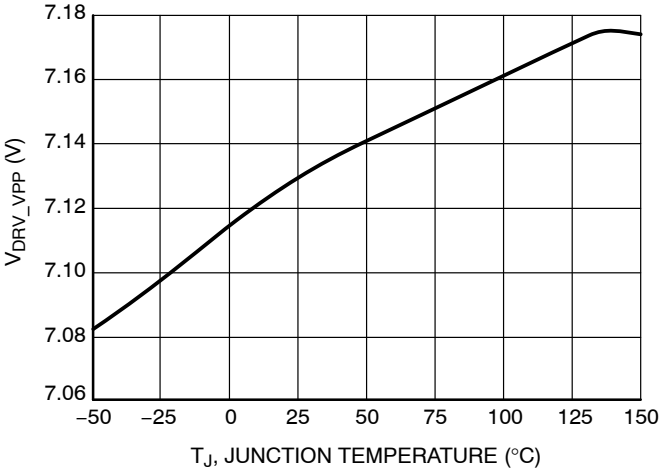


Figure 8. Drive Voltage vs. Junction Temperature

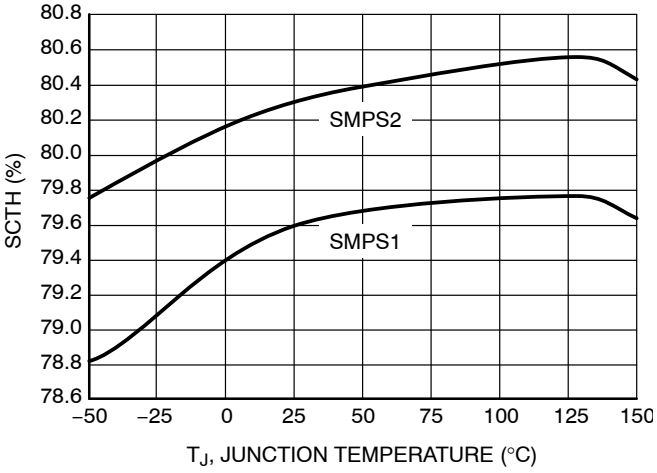


Figure 9. Short Circuit Threshold vs. Junction Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

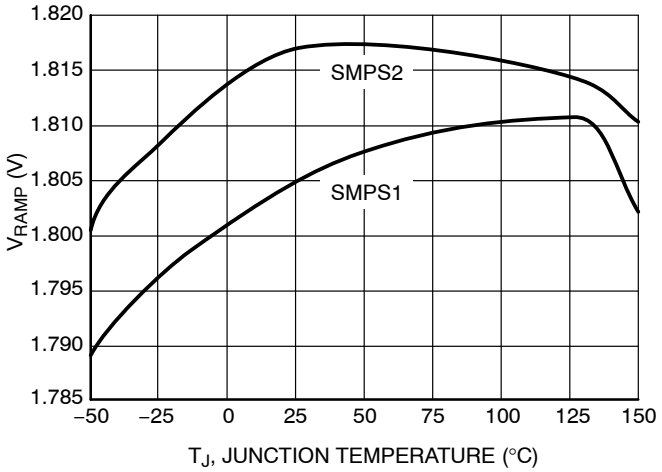


Figure 10. Ramp Amplitude vs. Junction Temperature

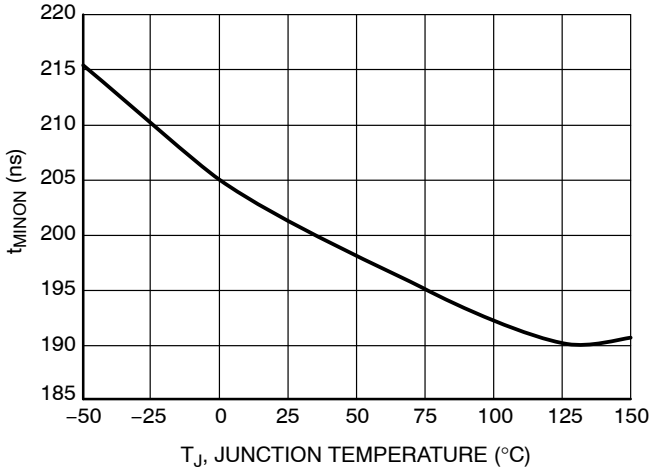


Figure 11. Minimum On Time vs. Junction Temperature

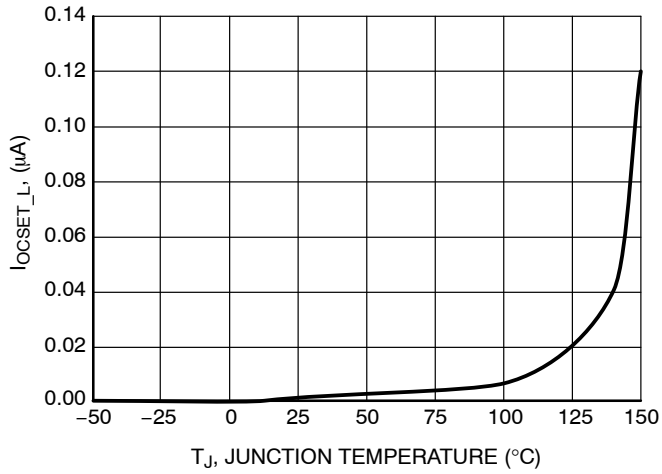


Figure 12. OCSET Leakage Current vs. Junction Temperature

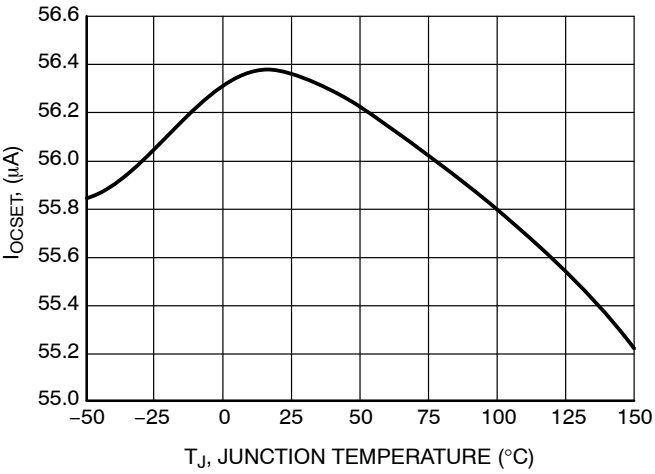


Figure 13. OCSET Current Sink vs. Junction Temperature

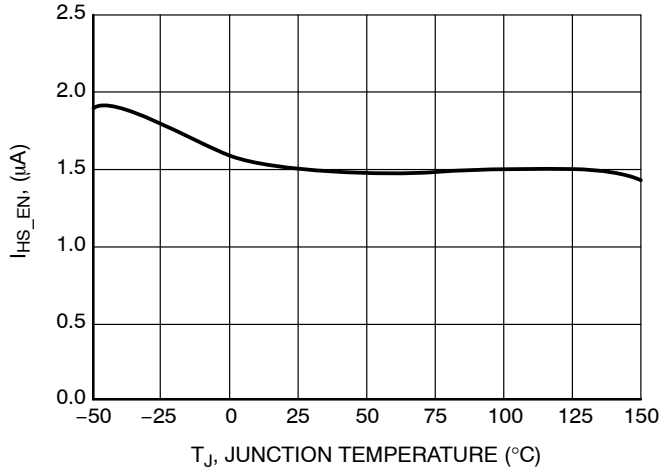


Figure 14. HS EN Leakage Current vs. Junction Temperature

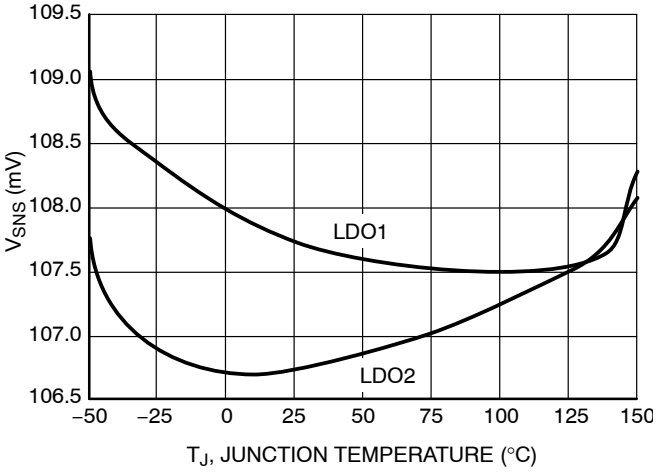


Figure 15. LDO Current Limit vs. Junction Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

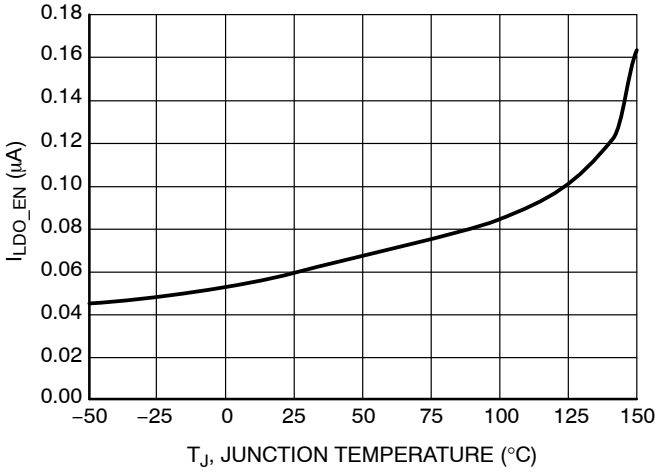


Figure 16. LDO EN Leakage Current vs. Junction Temperature

THEORY OF OPERATION

Device Description

The NCV8855 is a multiple output controller / regulator IC with an integrated high−side load switch. The NCV8855 will address automotive radio system and instrument cluster power supply requirements. In addition to the high−side load switch, the NCV8855 comprise a switch−mode power supply (SMPS) buck controller, a 2 A SMPS buck regulator, and two low dropout linear regulator controllers (LDO). The NCV8855 in combination with the ultra−low Iq NCV861x IC forms an eight output automotive radio or instrument cluster power solution.

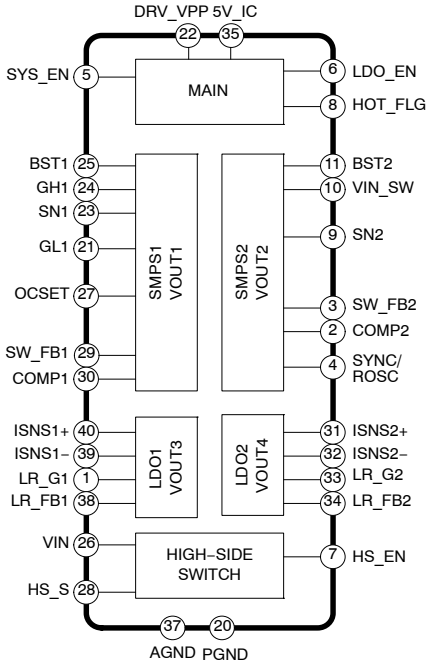


Figure 17.

The NCV8855 has an internally set switching frequency of 170 kHz and provides an SYNC pin for external frequency synchronization. The NCV8855 is designed to operate within the range of 9 V to 18 V. The switch−mode power supplies are voltage−mode controlled and the LDO controllers drive P−channel MOSFETs as pass devices.

System Enable (SYS_EN)

The system enable (SYS_EN) pin is used to start device operation or place it in low quiescent shutdown. Driving this pin high will allow the two main internal voltage rails (DRV_VPP and 5V_IC) to power up. These voltage rails require external bypassing and have independent UVLO trip points. Both rails must be operational in order for the IC to function. After exceeding its UVLO threshold, the IC will power up the switch−mode power supplies with a soft−start. Conversely, a logic−low on the pin will power down the DRV_VPP and 5V_IC rails and place the IC in an ultra−low current shutdown state.

Linear Regulator Enable (LDO_EN)

The low−dropout linear regulators (LDOs) have a dedicated enable pin. This pin controls the startup and shutdown of the LDOs. The SYS_EN pin must be logic high for this pin to function. It is possible to drive this pin high coincidentally with SYS_EN, but the LDO outputs will not startup until DRV_VPP and 5V_IC have increased above its UVLO thresholds.

High−Side Switch Enable (HS_EN)

The high−side switch enable controls only the high−side switch. Similar to LDO_EN, the SYS_EN pin must be logic high for this pin to function. The voltage level on all enable pins have been designed to work with 3.3 V or 5 V logic.

IC Power (VIN, VIN_SW, DRV_VPP, 5V_IC)

There are many input voltage rails for the NCV8855. The main power supply input for the IC is VIN. The DRV_VPP, 5V_IC and the high−side switch drain are all driven from V_{IN}. The DRV_VPP voltage rail is the power rail for SMPS1 & SMPS2's gate driver circuits. The 5V_IC voltage rail is the main supply for the IC. The VIN_SW rail is the supply rail for SMPS2's internal upper MOSFET. VIN_SW is directly tied to the drain of the N−channel MOSFET.

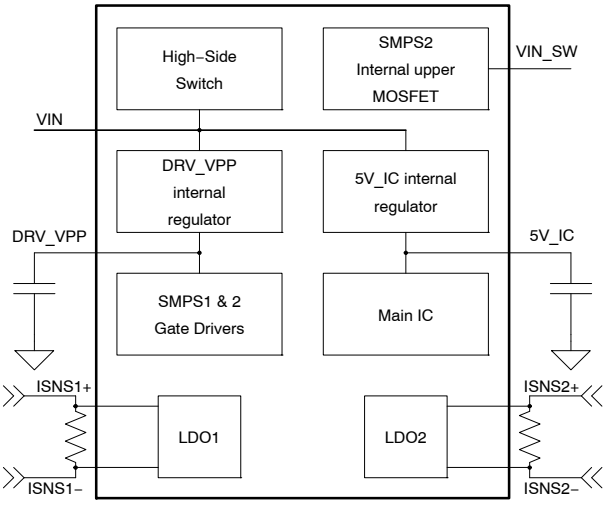


Figure 18.

Two additional inputs rails are ISNS1+ and ISNS2+. These inputs not only serve as the positive reference for the current sense circuit, but also serve as the supply rail for the LDO error amplifier.

Startup and Shutdown Behavior

The startup sequence primary depends on the system configuration. However, in every case, enable SYS_EN first. The SYNC pin must not be held at logic high before SYS_EN is enabled. Below shows typical startup and

shutdown behavior when VOUT3 is derived from VOUT1 (as shown in Figure 1).

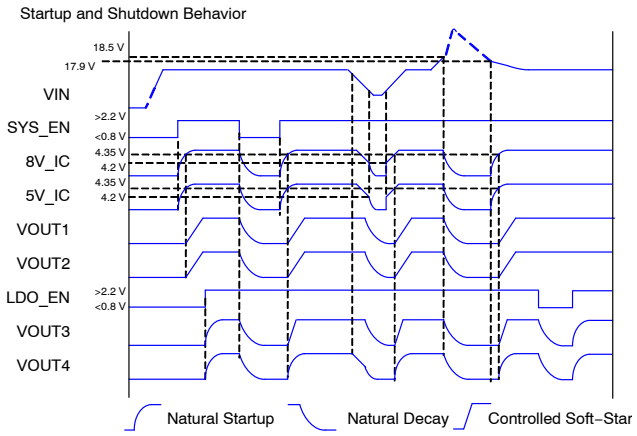


Figure 19.

In addition to the enable pins, the IC features an automatic shutdown during a high battery condition. When VIN exceeds 18.5 V (typ) the IC will shutdown all outputs. When V_{IN} falls below 17.9 V (typ), the IC will go through a typical start up and resume normal operation.

Out−of−Phase Synchronization

By default, the turn−on of SMPS2 is delayed by half the switching cycle, which corresponds to 180° phase delay. Advantages of out−of−phase synchronization are many. Interleaving the current pulses at the input reduces the input RMS current. This reduction minimizes the input filter requirement, allowing the use of smaller components, hence a more cost effective solution. In addition, since peak current is reduced, emitted EMI is also reduced.

Synchronizing (SYNC)

Synchronizing the NCV8855 to an external frequency is achieved by providing a 10 to 90% duty cycle clock to the SNYC pin. The rising edge of the clock signal will immediately reset the internal RAMP of SMPS2 and begin a new pulse for SMPS2. Conversely, the falling edge of the clock signal will immediately reset the internal RAMP of SMPS1 and begin a new pulse for SMPS1. The first rising edge of the external clock signal may cause a momentary phase diversion between SMPS1 and SMPS2, but will lock into desired phase on the subsequent falling edge. During start up, the SYNC pin must not be held at a logic high.

Thermal Warning (HOT_FLG) and Thermal Shutdown

There are two thermal sensors in the NCV8855 devices. If any of these two exceeds the warning threshold, the HOT_FLG will assert low. In addition, if thermal monitor 1 (T_{MON_HSS}) exceeds the warning threshold, the high−side switch current limit will fold back to 1.4 A (typ). If T_{MON_HSS} exceeds its TSD point, the high−side switch will latch off while the other device functions will continue to operate. A HS_EN or SYS_EN toggle will be required to re−start the high−side switch in the case of a T_{MON_HSS} TSD event.

If thermal monitor 2 (T_{MON_SW}) exceeds it TSD point, the entire chip (regardless of the state of T_{MON_HSS}) will latch off, and a SYS_EN toggle will be required to restart.

Overcurrent Protection (SMPS1)

Overcurrent protection for SMPS1 is implemented via $V_{DS(on)}$ sensing of the upper MOSFET. At the beginning of each switching cycle, after a short blanking time, the voltage is sampled across the upper MOSFET and compared to the threshold set by R_{OCSET}.

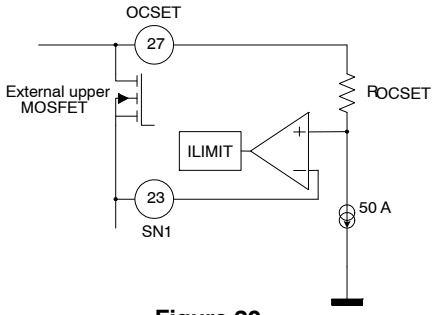


Figure 20.

If this comparator is tripped, then the pulse is immediately halted. This operation repeats every cycle until the overcurrent condition is removed.

The over−current limit can be calculated with the following equation:

$$I_{LIMIT} = \frac{R_{OCSET} \times I_{OCSET}}{R_{DS(on)}} \qquad \text{(eq. 1)}$$

where, I_{OCSET} is 50 μA (typ.). To calculate the R_{OCSET} value, the maximum $R_{DS(on)}$ (at temperature) and the minimum value of I_{OCSET} must be used. In addition to this, the following relationship should be met:

$$I_{LIMIT} \geq IOUT1_{(MAX)} + \frac{I_{pk-pk}}{2} \qquad \text{(eq. 2)}$$

where $IOUT1_{(MAX)}$ is the maximum dc current allowed, and $I_{pk-pk}/2$ is the peak ripple current above the dc value. This will insure that undesirable trigger of the over−current protection is avoided.

To protect in the case of a short circuit event, a comparator monitoring the feedback voltage is incorporated. If the output voltage goes below 70% of nominal after start−up, the part is latched off, requiring SYS_EN to be toggled to restart the part.

The over current protection circuitry is active upon startup (short circuit protection is not). During soft−start, under normal conditions, the current limit circuit should not trip. However, with large output capacitance, the current limit circuit may determine the output voltage rise time instead of the soft−start circuit. To ensure that the output voltage is

controlled by the soft−start circuit make $dt_{limit} \leq T_{SS1}$, where T_{SS1} is the soft−start time and dt_{limit} is equal to:

$$\frac{COUT1 * VOUT1}{I_{LIMIT}} \quad \text{(eq. 3)}$$

Overcurrent Protection (SMPS2)

The current limit for SMPS2 is internally set at 3.05 A (typ). The operation is similar to SMPS1 in that it immediately ends the pulse upon overcurrent detection. This repeats every cycle until the overcurrent condition is removed. Similar to SMPS1, the over current protection circuitry is active upon startup.

As with SMPS1, short circuit protection is implemented with a comparator monitoring the feedback. If the output voltage goes below 70% of nominal after start−up, the part is latched off, requiring SYS_EN to be toggled to restart the part.

Overcurrent Protection (LDO1 and LDO2)

There are two overcurrent protection circuits incorporated; one provides a current limit feature, the other provides a short circuit protection feature. Under normal operation, the current is sensed through a sense resistor connected to ISNS[x]+ and ISNS[x]− and limited by the equation:

$$I_{LIMIT(LDO)} = \frac{V_{SNS[x]}}{R_{SNS[x]}} \quad \text{(eq. 4)}$$

where, $R_{SNS[x]}$ is the sense resistor for LDO1 and LDO2, and $V_{SNS[x]}$ is the current limit threshold. To calculate $R_{SNS[x]}$, the minimum $V_{SNS[x]}$ value and the maximum operating current should be used.

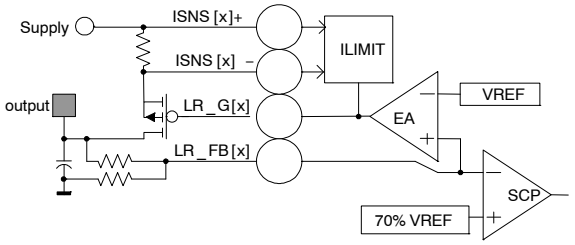


Figure 21.

To thermally protect the pass device during a short circuit event, a comparator monitoring the feedback voltage is incorporated. If the output voltage goes below 70% of nominal (typ), the LDO will latch off. This is an independent operation, meaning, a short circuit on one LDO does not affect the operation of the other, nor does it affect the SMPS or high−side switch. An LDO_EN toggle is required to re−start an LDO if it latched off due to a short circuit event.

In addition, the current limit should be chosen such that the output voltage will rise to greater than 70% of the final VOUT within 2.74 ms in order to keep the short−circuit circuit from falsely tripping.

Overcurrent Protection (High−Side Load Switch)

There are two primary protection features of the internal high−side 2.8 A (typ.) current limit. The first protection involves a short circuit condition during startup, and the second involves an overload condition after startup.

During startup, if the output does not exceed 4.5 V (typ.) in 1.5 ms (typ.), the device is considered to be in a “hard” short circuit condition, and is latched off. In addition, if the device does not exceed VIN − 3.75 V (typ.) in 3 ms (typ), the device is considered to be in a “soft” short circuit condition, and is latched off. Furthermore, if V_{HS_S} goes below VIN − 3.75 V (typ), during normal operation, for more than 3 ms (typ), the device is considered to be in a “soft” short circuit condition, and is latched off. Once the high−side switch has been latched off, a HS_EN toggle will be required to reset it.

Overvoltage Clamp (High−Side Load Switch)

The source output of the high−side switch is clamped during a high battery condition. This protects any load connected to the source from seeing a double battery or load dump condition. If the input rises above 16 V (typ), the internal gate of the high−side switch will be pulled low to keep the source from rising. The high−side switch will operate in this linear mode until the input voltage exceeds 18.5 V (typ) at which point the entire IC will shutdown.

APPLICATION INFORMATION

Setting the Output Voltage

To set the output voltage of any of the controllers or regulators, use the following equation:

$$V_{OUT[x]} = V_{REF}\left(1 + \frac{R1}{R2}\right) \quad \text{(eq. 5)}$$

where, R1 is the resistor that is connected from VOUT[x] to the feedback pin of its respective channel and R2 is connected from that feedback pin to ground. To reduce the effect of input offset current error, it is customary to calculate R1 with R2 equal to 1 kΩ.

LDO1 and LDO2 Pass Device Selection

The LDO controllers have been optimized to give the best performance with the NTD20P06L p−channel MOSFET. While other p−channel MOSFET can be used, specifications in the electrical table are guaranteed only with the NTD20P06L, and using a different MOSFET may require external compensation to stabilize the output. The NTD20P06L can be used as the pass device for both controllers, and is rated with a −60 V max V_{DS}. This device comes in two different packages allowing great flexibility

when designing the thermal solution. The IPAK package can be attached to the radio's metal enclosure or it can be attached to an independent heatsink. If output current demands are low, then a DPAK package can be used for a surface mount solution.

LDO Output Capacitor Selection

The LDO controllers have been optimize and compensated to work with a variety of output capacitors. Aluminum electrolytic capacitors with an ESR up to 5 Ω to ceramic capacitors with an ESR down to 10 mΩ can be used. Depending on load requirements, the output capacitor can range from 10 μF to as much as 100 μF. There are many capacitor vendors which supply automotive rated parts that fall within these ranges. For example, the Nichicon UD or PM type capacitors are suited well for the LDO controllers and automotive radio application. Values outside of these ranges can be used, but may require external compensation.

SMPS1 MOSFET Selection

SMPS1 has integrated MOSFET drivers optimized for driving N−channel MOSFETs in a synchronous buck configuration. The lower MOSFET driver is designed to drive a ground−referenced low $R_{DS(on)}$ n−channel MOSFET. The supply rail for the lower driver is internally connected to DRV_VPP and the PGND pin is it's ground reference. The upper MOSFET driver is a floating gate driver designed to drive low $R_{DS(on)}$ n−channel MOSFETs. A bootstrap circuit referenced to SN1 as shown in figure 1 develops the supply rail for the upper MOSFET driver.

The driver circuitry includes non−overlap protection. The non−overlap protection prevents both Q1 (upper MOSFET) and Q2 (lower MOSFET) from being on at the same time, and minimizes the associated off times.

This helps reduce power losses in the switching elements. The non−overlap protection circuit accomplishes this by controlling the delay from Q1's turn−off to Q2's turn−on, and from Q2's turn−off to Q1's turn on by monitoring the voltage at the SN1 and GL1 pins. When the internal PWM signal goes low, GH1 will go low, turning Q1 off. However, before Q2 can turn on, the non−overlap protection circuit waits for the voltage at the SN1 pin to fall below 1.8 V. Once SN1 falls below the 1.8 V threshold, GL1 will go high, turning Q2 on. However, if SN1 does not fall below 1 V in 100 ns, the safety timer circuit will override the normal control scheme and drive GL1 high. This will help insure that if Q1 fails to turn off it will not produce an over−voltage at the output.

Similarly, to prevent cross conduction during Q2's turn−off and Q1's turn−on, the non−overlap circuit monitors the voltage at the gate of Q2 through the GL1 pin. When the internal PWM signal goes high, GL1 will go low turning Q2 off. However, before Q1 can turn on, the non−overlap protection circuit waits for the voltage at GL1 to drop below 2 V. Once this has occurred, GH1 will go high, turning Q1 on.

For the DRV_VPP supply, a local bypass capacitor is not only required for stability, but also to reduce noise and supply peak currents during operation. Use a 1 to 4.7 μF, low ESR capacitor. Multilayer ceramic chip (MLCC) capacitors provide the best combination of low ESR and small size. This capacitor must be referenced to PGND. The bootstrap circuit comprises a charge storage capacitor (C_{BST1}) and the internal bootstrap diode. Typical C_{BST1} values range from 100 nF to 1 μF. The average forward current can be estimated by the following equation:

$$I_{BST1} = Q_{GATE} \times FSW \quad \text{(eq. 6)}$$

where, Q_{GATE} is the total gate charge. The average forward current through the internal diode should not exceed its rated maximum of 12 mA. This puts a limitation on the MOSFETs used at a particular switching frequency.

The power dissipation for the internal MOSFET drivers can be calculated using the following equation:

$$Pd_{SMPS1\_drv} = Pd_{GH1\_drv} + Pd_{GL1\_drv} \quad \text{(eq. 7)}$$

$$Pd_{GH1\_drv} = Q_{GH1} \times V_{GH1} \times FSW \quad \text{(eq. 8)}$$

$$Pd_{GL1\_drv} = C_{GL1} \times \left(V_{GL1}\right)^2 \times FSW \quad \text{(eq. 9)}$$

where, Q_{GH1} is the total gate charge of the upper MOSFET, C_{GL1} is the total input capacitance of the lower MOSFET, $V_{GH1} = V_{GL1} = 7.2$ V (typ.) which is the DRV_VPP output voltage.

One method to improve the IC power dissipation is to diode−or the 8 V SMPS output to the DRV_VPP pin. This will override the internal regulator and the IC will run from the SMPS output. Doing this will incrementally increase the gate drivers power dissipation, but will reduce the loss associated with the DRV_VPP running from battery.

For example, if the DRV_VPP is operating at 12 mA from a 14.4 V battery to power SMPS1's gate driver circuit, the power dissipation from this will be 90 mW. In addition, with a 20 nC GH1 change and a 1.8 nF GL1 capacitance, the gate driver loss will be 80 mW. This is a total of 170 mW of power dissipation due to running the gate drivers at 340 kHz. However, if there was a diode−or to the DRV_VPP from the 8 V output of one of the SMPSs, then the DRV_VPP LDO losses are eliminated, and the total power dissipation from running the SMPS1 gate drivers reduce to 95 mW. The improvement gets better when accounting for SMPS2's gate driver loss. This savings can prove to be beneficial in fast FSW and high current applications.

There are two recommended n−channel MOSFET for SMPS1, the NTD24N06, which has a 60 V max VDS, and the NTD5407N, which has a 40 V max VDS. Determining which MOSFET to use is predicated by the load dump requirements. The same device can be used for the upper and lower MOSFET. The benefit of this is reduced cost due to economies of scale.

SMPS2 Diode Selection

The diode in SMPS2 provides the inductor current path when the power switch turns off. This is known as the non−synchronous diode or commutation diode. The peak reverse voltage is equal to the maximum operating input voltage. The peak conducting current is determined by the internal current limit. The average current can be calculated from:

$$I_{D(avg)} = IOUT2\left(1 - \frac{VOUT2}{VIN\_SW}\right) \quad \text{(eq. 10)}$$

However, the worse case diode average current occurs during a short circuit condition. For a diode to survive an indefinite short circuit condition, the current rating of the diode should be equal to the maximum current limit which is 3.6 A. Thus the MBRS4201T3 is the diode of choice.

Inductor Selection

Both mechanical and electrical considerations influence the selection of an output inductor. From a mechanical perspective, smaller inductor values generally correspond to smaller physical size. Since the inductor is often one of the largest components in SMPS system, a minimum inductor value is particularly important in space−constrained applications. From an electrical perspective, smaller inductor values correspond to faster transient response. The maximum current slew rate through the output inductor for a buck regulator is given by:

$$\text{Inductor Slew Rate} = \frac{dI_L}{dt} = \frac{V_L}{L} \quad \text{(eq. 11)}$$

Where I_L is the inductor current, L is the output inductance, and V_L is the voltage drop across the inductor. This equation indicates that larger inductor values limit the regulator's ability to slew current through the output inductor in response to output load transients. Consequently, output capacitors must supply (or store) sufficient charge to maintain regulation while the inductor current "catches up" to the load. This results in larger values of output capacitance to maintain tight output voltage regulation.

In contrast, smaller values of inductance increase the regulator's maximum achievable slew rate and decrease the necessary capacitance, at the expense of higher ripple current.

In continuous conduction mode, the peak−to−peak ripple current is calculated using the following equation:

$$I_{PP} = FSW\frac{VOUT}{L}\left(1 - \frac{VOUT}{VBATT}\right) \quad \text{(eq. 12)}$$

From this equation it is clear that the ripple current increases as L decreases, emphasizing the trade−off between dynamic response and ripple current.

For most applications, the inductor value falls in the range between 2.2 μH and 22 μH. There are many magnetic component vendors providing standard product

lines suitable for SMPS1 and SMPS2's requirements. TDK offers the RLF12545−PF series inductors, which are recommended for the automotive radio application.

SMPS Output Capacitor Selection

The output capacitor is a basic component for the fast response of the power supply. In fact, during load transient, for first few microseconds they supply the current to the load. The controller recognizes the load transient and proceeds to increase the duty cycle to its maximum. Neglecting the effect of the ESL, the output voltage has a first drop due to the ESR of the bulk capacitor(s).

$$\Delta VOUT_{(ESR)} = \Delta IOUT \times ESR \quad \text{(eq. 13)}$$

A lower ESR produces a lower ΔV during load transient. In addition, a lower ESR produces a lower output voltage ripple.

The voltage drop due to the output capacitor discharge can be approximated using the following equation:

$$\Delta VOUT_{(discharge)} = \frac{(\Delta IOUT)^2 \times L}{2 \times COUT \times \left(VIN_{(min)} \times D_{MAX} - VOUT\right)} \quad \text{(eq. 14)}$$

where, D_{MAX} is the maximum duty cycle value, which is 90%. Although the ESR effect is not in phase with the discharging of the output voltage, $\Delta VOUT_{(ESR)}$ can be added to $\Delta VOUT_{(discharge)}$ to give a rough indication of the maximum ΔVOUT during a transient condition. Simulation can also help determine the maximum ΔVOUT; however, it will ultimately have to be verified with the actual load since the ESL effect is dependent on layout and the actual load's di/dt.

SMPS Input Capacitor Selection

The primary consideration for selecting the input capacitor is input RMS current. However, since there are two SMPS running out−of−phase with each other, calculating the input RMS current can be complicated. The graphs below shows how the input RMS current is affected by differing phase angles between SMPS1 and SMPS2. The plot below was generated with VOUT1 at 5 V with a load of 2 A and an output inductor value of 10 μH, and VOUT2 at 8 V with a load of 4 A and an output inductor value of 10 μH.

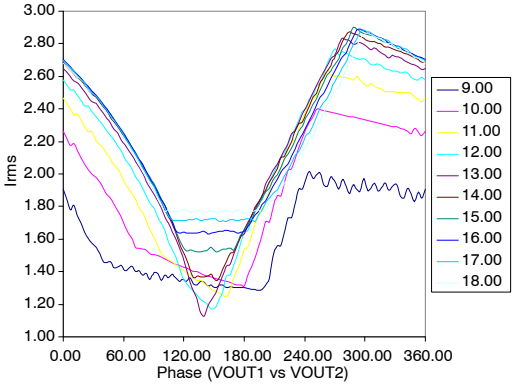


Figure 22. Irms vs Phase

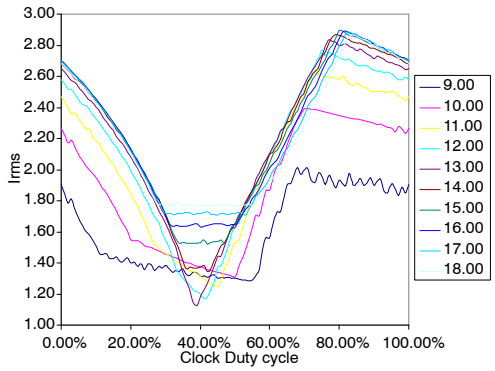


Figure 23. Irms vs Phase

Here it is shown that the “sweet spot” phase angle (where the input RMS current is the lowest) happens at the same location (in terms of phase relationship) regardless of input voltage. Thus, once the output voltages are known, a sweet spot can be determined. After determining the sweet spot, the input capacitors can be chosen accordingly to handle the RMS current.

The purpose of interleaving the two SMPS is to eliminate any overlapping of there input currents. This will reduce the overall input RMS current. Since the outputs are running at different voltages, they will have different duty cycles, and thus running with 180° phase difference does not necessarily guarantee an optimal input RMS current reduction. The figures below describe, graphically, this point.

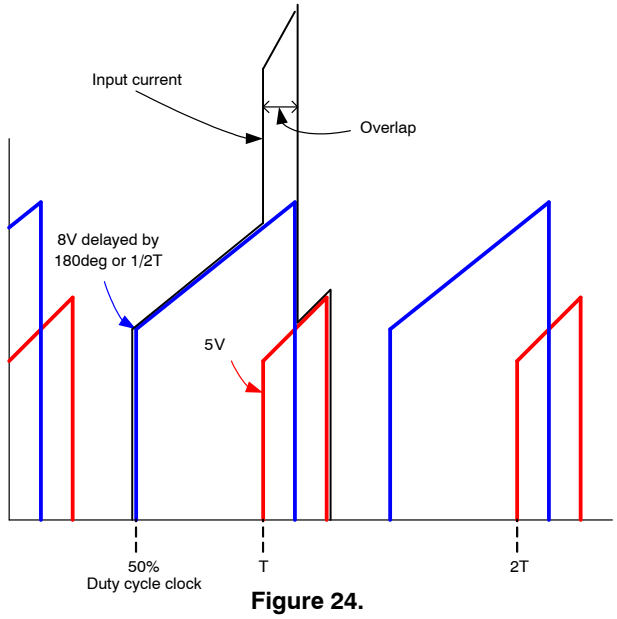


Figure 24.

Since the 8 V rail has a wider pulse, with a 50% internal clock duty cycle, there will be some amount of input current overlapping which will produce a less than ideal RMS current. The following figure shows an optimized duty cycle where there is no overlapping.

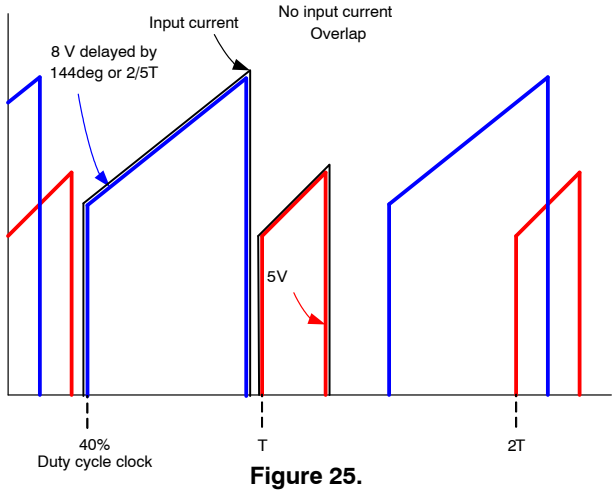


Figure 25.

To achieve this optimization, the SYNC function on the NCV8855 will have to be used with a 40% duty cycle clock. However, when looking at the worst−case input RMS (which occurs at high battery) a 40% duty cycle clock will yield the same input RMS current as a 50% duty cycle clock. Thus, the only true benefit of this optimization occurs when a narrow input voltage range is assured. Therefore, a 50% duty cycle clock is always recommended.

SMPS Compensation

The NCV8855 utilizes voltage mode control. The control loop regulates V_{OUT} by sampling V_{OUT} and controlling the duty cycle. Inherent with all voltage−mode control loops is a compensation network.

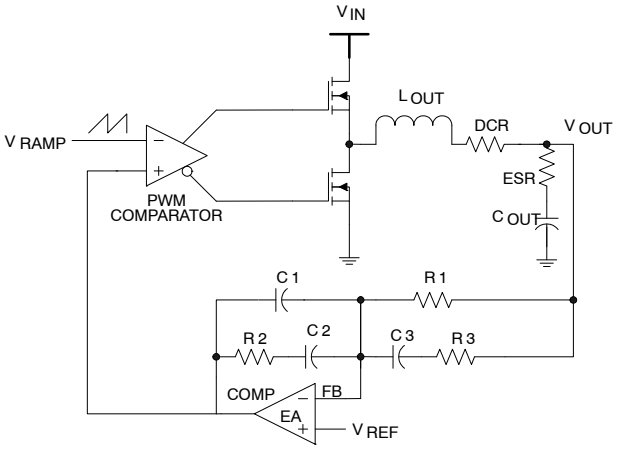


Figure 26.

The compensation network consists in the internal error amplifier and the impedance networks Z_{IN} (R1, R3 and C3) and Z_{FB} (R2, C1 and C2). The compensation network has to provide a closed loop transfer function with the highest 0 dB crossing frequency to have fast response and the highest gain in dc conditions to minimize the load regulation. A stable

control loop has a gain crossing with −20 dB/decade slope and a phase margin greater than 45°.

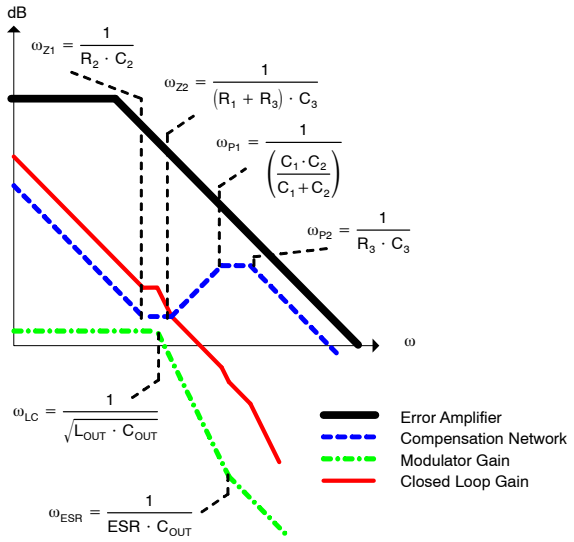


Figure 27.

To reiterate, there are 3 primary goals to compensating. Goal 1 is to have a high a unity gain bandwidth (UGB) that is greater than 1/10 the switching frequency, but less than 1/2 the switching frequency. UGB is also known as the crossover frequency. This is the point where the closed loop gain = 0 dB or a gain of 1. In the plot above, the UGB is the point where the red line crosses the Ω axis. Goal 2 is to have the closed loop gain cross 0 dB with a −20 dB/decade slope also known as a −1 slope. Goal 3 is to achieve over 45° of phase margin when the gain crosses 0 dB.

These are just goals. Sometimes the crossover frequency is reduced below 1/10 FSW in order to meet goal 3. Conversely, some designs will push the crossover frequency as high as it can (as long as it is below 1/2 FSW) with a reduce phase margin of 30° in order to get a faster transient response. The only two absolutes are that the crossover frequency cannot exceed 1/2 FSW and the phase margin has to be greater than 0° at crossover. However, a SMPS operating towards these absolutes will experience sever ringing before it dampens out.

To achieve the above goals, the following guidelines should be adopted.

- Place wZ1 at half the resonance of wLC
- Place wZ2 at or around wLC
- Place wP1 at wESR
- Place wP2 at half the switching frequency

Performing these calculations will take some amount of iterations and bench testing to verify results. However, ON Semiconductor has developed a tool to speed up the design process tremendously with great ease and accuracy. This tool can be downloaded by following the below link.
http://www.onsemi.com/pub/Collateral/COMPCALC.ZIP

AUTOMOTIVE RADIO SYSTEM BLOCK DIAGRAM EXAMPLE NCV8855 WITH NCV8612

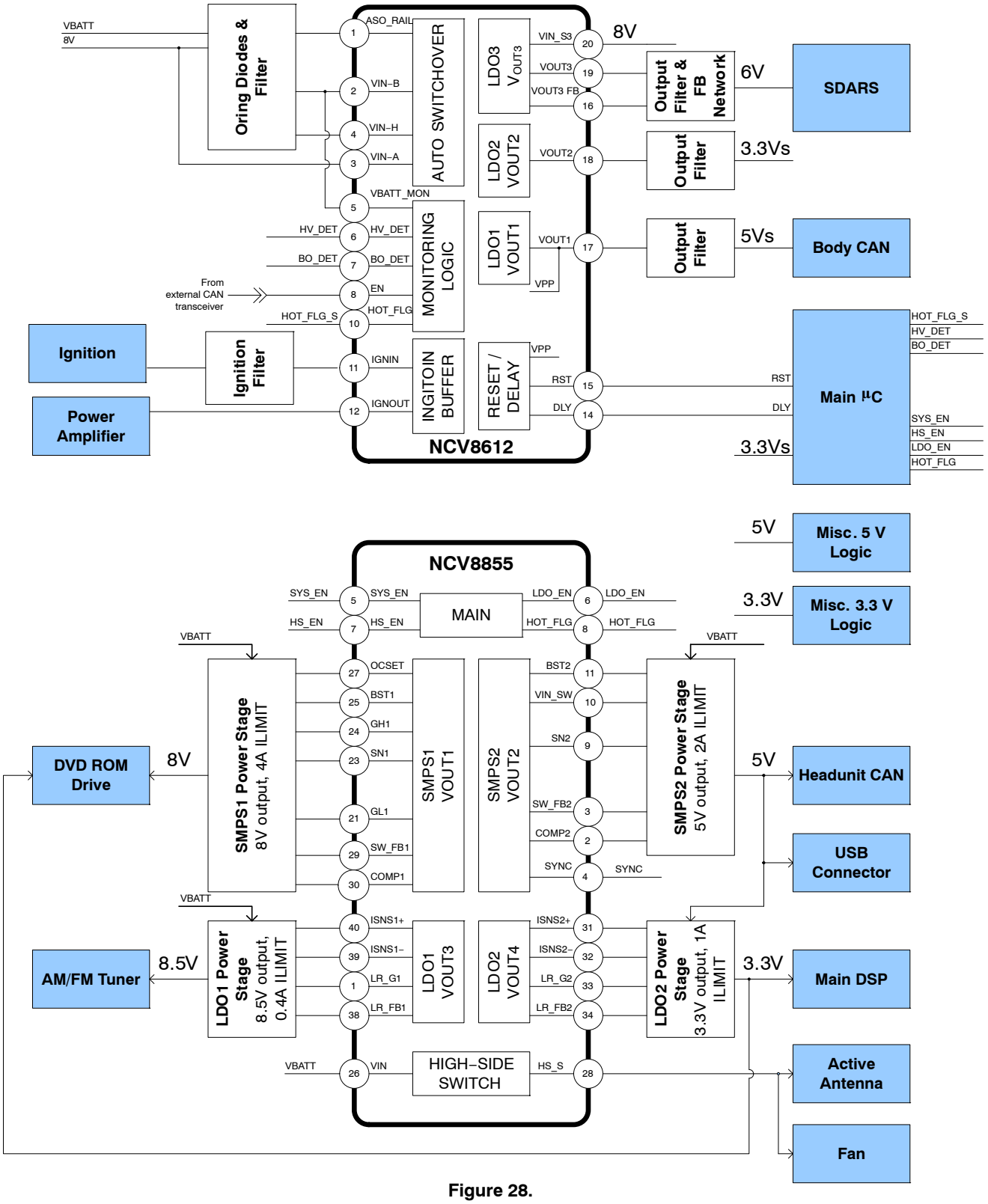


Figure 28.

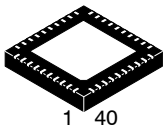
NOTE: Not all pins are shown above.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

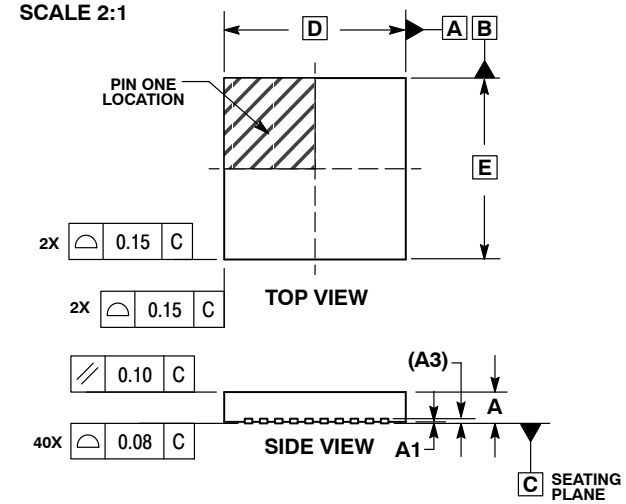
ON Semiconductor®

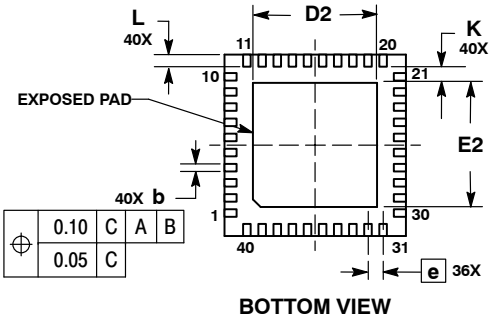
QFN40 6x6, 0.5P
CASE 488AR−01
ISSUE A

DATE 18 APR 2007



SCALE 2:1





BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

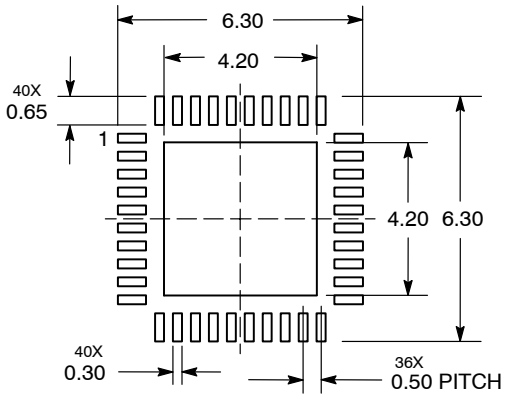
	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	6.00 BSC	
D2	4.00	4.20
E	6.00 BSC	
E2	4.00	4.20
e	0.50 BSC	
L	0.30	0.50
K	0.20	−−−

GENERIC MARKING DIAGRAM*

XXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**QFN40, 6 x 6 x 0.85, 0.5 MM PITCH**	**PAGE 1 OF 1**

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