NCV8674

Linear Regulator - Low Dropout, Very Low I_q

The NCV8674 is a precision 5.0 V or 12 V fixed output, low dropout integrated voltage regulator with an output current capability of 350 mA. Careful management of light load current consumption, combined with a low leakage process, achieve a typical quiescent current of 30 μA.

The output voltage is accurate within ±2.0%, and maximum dropout voltage is 600 mV at full rated load current.

It is internally protected against input supply reversal, output overcurrent faults, and excess die temperature. No external components are required to enable these features.

Features

- 5.0 V and 12 V Output Voltage Options
- ±2.0% Output Accuracy, Over Full Temperature Range
- 40 μA Maximum Quiescent Current at I_{OUT} = 100 μA
- 600 mV Maximum Dropout Voltage at 350 mA Load Current
- Wide Input Voltage Operating Range of 5.5 V to 45 V
- Internal Fault Protection
  - −42 V Reverse Voltage
  - Short Circuit/Overcurrent
  - Thermal Overload
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes
- AEC−Q100 Qualified
- EMC Compliant
- This is a Pb−Free Device

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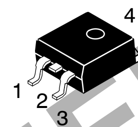
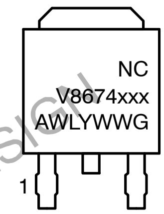
MARKING DIAGRAMS



D²PAK
DS SUFFIX
CASE 936



xxx	=	50 (5.0 V Option)
	=	120 (12 V Option)
A	=	Assembly Location
WL	=	Wafer Lot
Y	=	Year
WW	=	Work Week
G	=	Pb−Free Package

PIN CONNECTIONS

PIN	FUNCTION
1	V_{IN}
2, TAB	GND
3	V_{OUT}

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

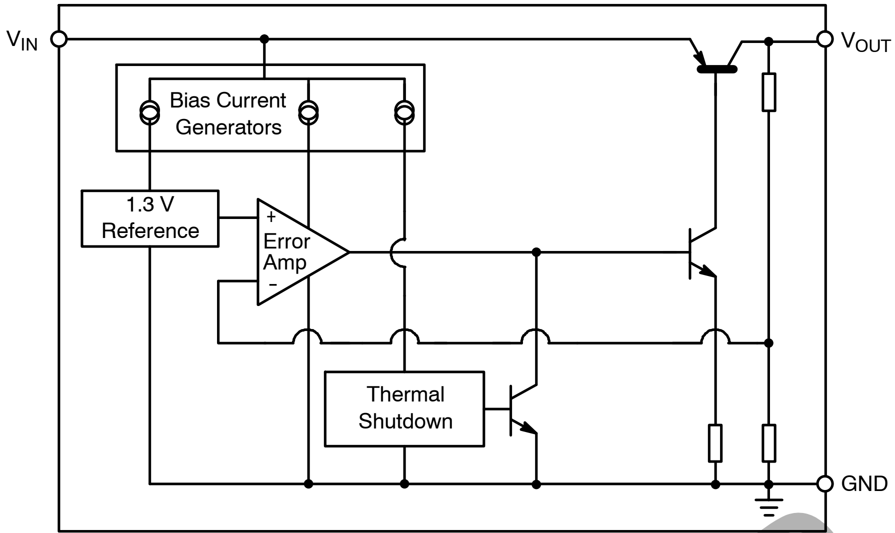


Figure 1. Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Function
1	V_{IN}	Unregulated input voltage; (V_{OUT} + 0.5 V) to 45 V.
2	GND	Ground; substrate.
3	V_{OUT}	Regulated output voltage; collector of the internal PNP pass transistor.
TAB	GND	Ground; substrate and best thermal connection to the die.

OPERATING RANGE

Pin Symbol, Parameter	Symbol	Min	Max	Unit
V_{IN}, DC Input Operating Voltage	V_{IN}	V_{OUT} + 0.5 V	+45	V
Junction Temperature Operating Range	T_J	−40	+150	°C

MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
V_{IN}, DC Voltage	V_{IN}	−42	+45	V
V_{OUT}, DC Voltage	V_{OUT}	−0.3	+16	V
Storage Temperature	T_{stg}	−55	+150	°C
ESD Capability, Human Body Model (Note 1)	V_{ESDHB}	4000	–	V
ESD Capability, Machine Model (Note 1)	V_{ESDMIM}	200	–	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series incorporates ESD protection and is tested by the following methods:
   ESD HBM tested per AEC−Q100−002 (EIA/JESD22−A 114C)
   ESD MM tested per AEC−Q100−003 (EIA/JESD22−A 115C)

Thermal Resistance

Parameter	Symbol	Min	Max	Unit
Junction−to−Ambient (Note 2)	$R_{\theta JA}$	–	40	°C/W
Junction−to−Case	$R_{\theta JC}$	–	4.0	°C/W

2. 1 oz., 1 in^2 copper area.

LEAD SOLDERING TEMPERATURE & MSL

Rating	Symbol	Min	Max	Unit
Lead Temperature Soldering – Reflow (SMD Styles Only), Lead Free (Note 3)	T_{sld}	–	265 pk	°C
Moisture Sensitivity Level	MSL	1		–

3. Lead Free, 60 sec – 150 sec above 217°C, 40 sec max at peak.

ELECTRICAL CHARACTERISTICS (V_{IN} = 13.5 V, Tj = −40°C to +150°C, unless otherwise noted.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage 5 V Option 12 V Option	V_{OUT}	0.1 mA ≤ I_{OUT} ≤ 350 mA (Note 4) (V_{OUT} + 1 V) ≤ V_{IN} ≤ 28 V	 4.90 11.76	 5.00 12.00	 5.10 12.24	V
Line Regulation 5 V Option 12 V Option	ΔV_{OUT} vs. V_{IN}	I_{OUT} = 5.0 mA (V_{OUT} + 1 V) ≤ V_{IN} ≤ 28 V	 −25 −60	 5.0 12	 +25 +60	mV
Load Regulation 5 V Option 12 V Option	ΔV_{OUT} vs. I_{OUT}	1.0 mA ≤ I_{OUT} ≤ 350 mA (Note 4)	 −35 −84	 5.0 12	 +35 +84	mV
Dropout Voltage	V_{IN}−V_{OUT}	I_{OUT} = 100 mA (Notes 4 & 5) I_{OUT} = 350 mA (Notes 4 & 5)	– –	175 300	500 600	mV
Quiescent Current 5 V Option 12 V Option 5 V Option 12 V Option	I_q	I_{OUT} = 100 μA T_J = 25°C T_J = 25°C T_J = −40°C to +85°C T_J = −40°C to +85°C	 – – – –	 27 31 30 34	 35 39 38 42	μA
Active Ground Current 5 V Option 12 V Option 5 V Option 12 V Option	$I_{G(ON)}$	 I_{OUT} = 50 mA (Note 4) I_{OUT} = 50 mA (Note 4) I_{OUT} = 350 mA (Note 4) I_{OUT} = 350 mA (Note 4)	 – – – –	 1.1 1.1 18 21	 3.0 3.0 27 40	mA
Power Supply Rejection	PSRR	V_{RIPPLE} = 0.5 V_{P-P}, F = 100 Hz	–	67	–	dB
Output Capacitor for Stability	C_{OUT} ESR	I_{OUT} = 0.1 mA to 350 mA (Note 4)	22 –	– –	– 7.0	μF Ω

PROTECTION

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Limit 5 V Option 12 V Option	$I_{OUT(LIM)}$	 V_{OUT} = 4.5 V (Note 4) V_{OUT} = 10.8 V (Note 4)	 350 350	 – –	 – –	mA
Short Circuit Current Limit	$I_{OUT(SC)}$	V_{OUT} = 0 V (Note 4)	100	600	–	mA
Thermal Shutdown Threshold	T_{TSD}	(Note 6)	150	–	200	°C

4. Use pulse loading to limit power dissipation.
5. Dropout voltage = (V_{IN} − V_{OUT}), measured when the output voltage has dropped 100 mV relative to the nominal value obtained with V_{IN} = 13.5 V.
6. Not tested in production. Limits are guaranteed by design.

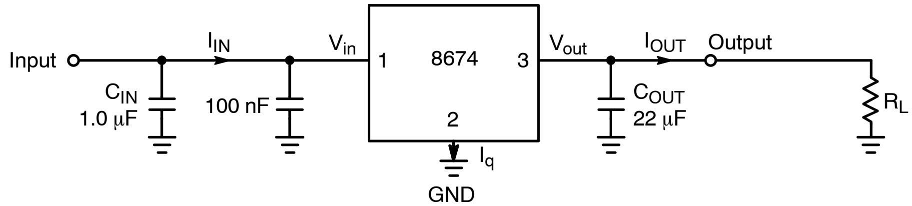


Figure 2. Measurement Circuit

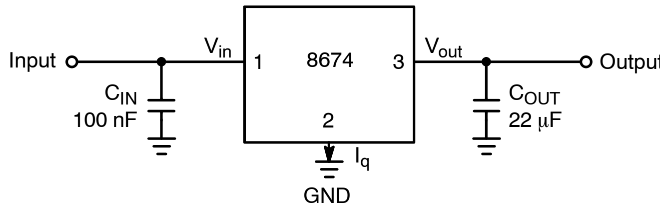


Figure 3. Applications Circuit

TYPICAL CHARACTERISTIC CURVES – 5 V OPTION

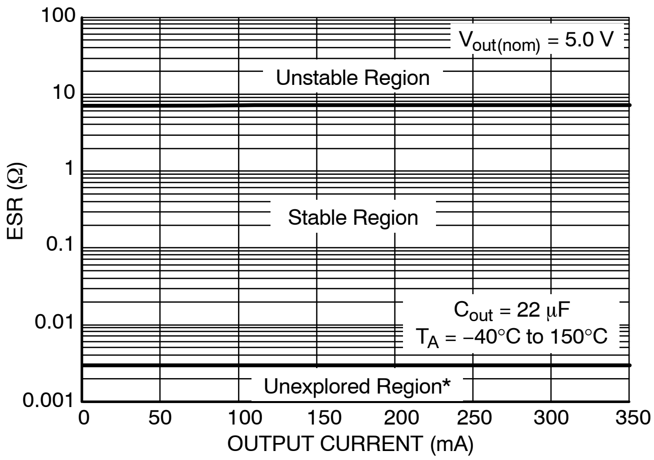


Figure 4. ESR Stability Region vs. Output Current

*The min specified ESR is based on Murata's capacitor GRM31CR60J226KE19 used in measurement. The true min ESR limit might be lower than shown.

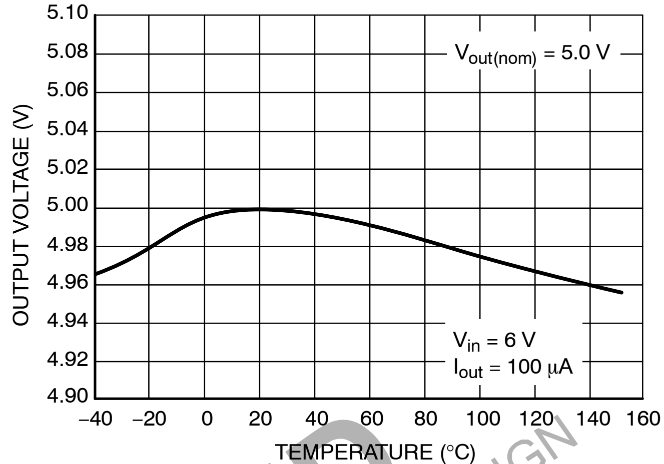


Figure 5. Output Voltage vs. Temperature

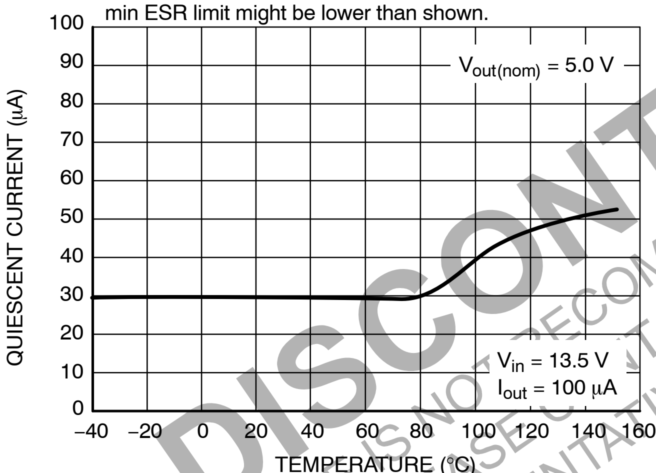


Figure 6. Quiescent Current vs. Temperature

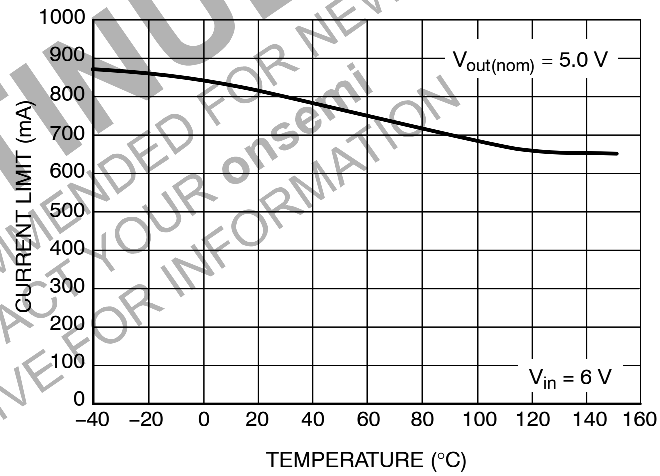


Figure 7. Current Limit vs. Temperature

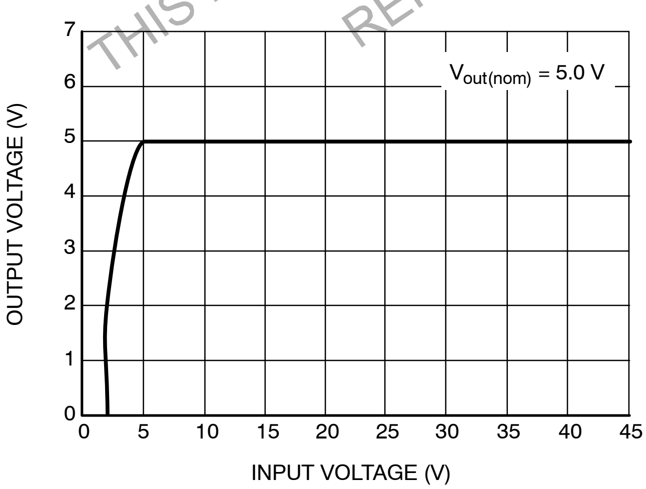


Figure 8. Output Voltage vs. Input Voltage

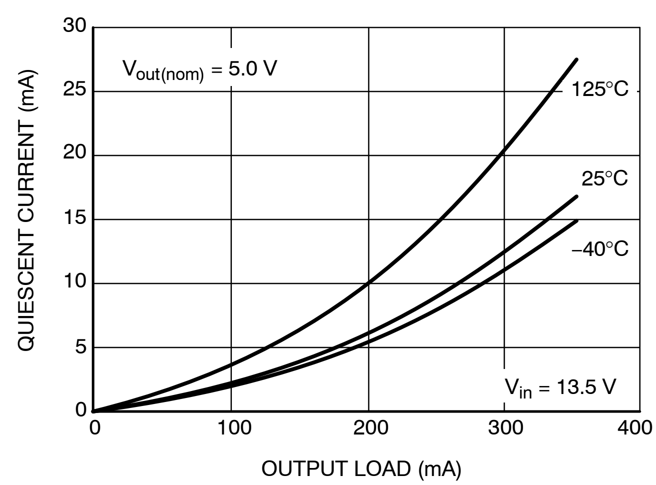


Figure 9. Quiescent Current vs. Output Load

TYPICAL CHARACTERISTIC CURVES – 5 V OPTION

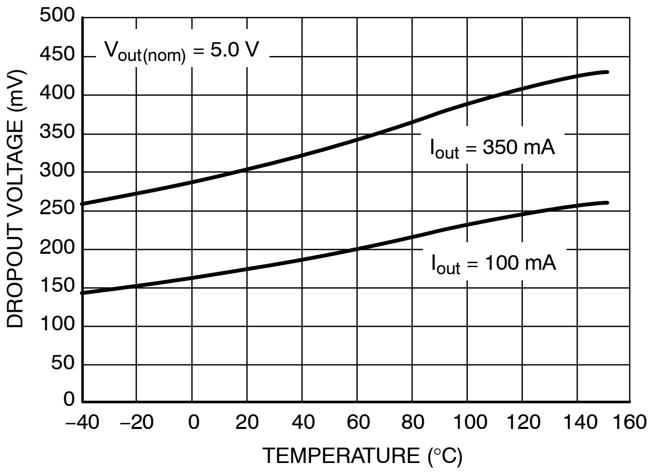


Figure 10. Dropout Voltage vs. Temperature

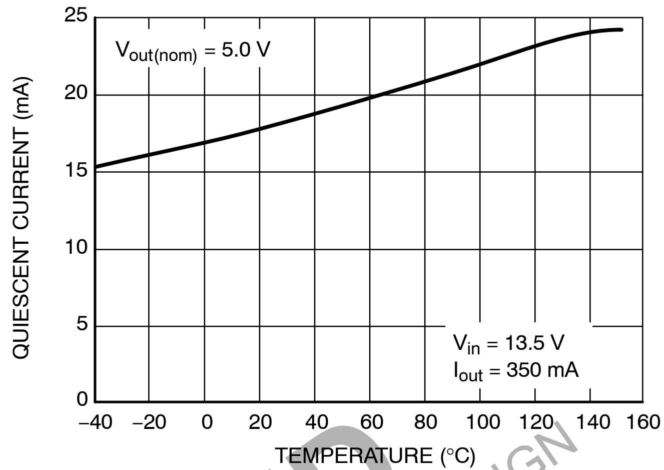


Figure 11. Quiescent Current vs. Temperature – 350 mA Load

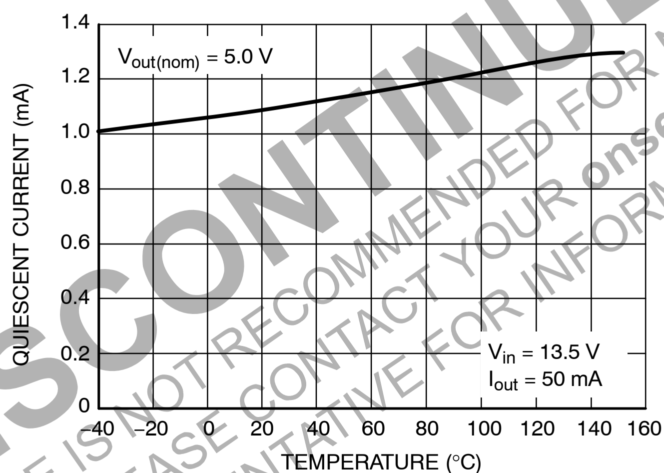


Figure 12. Quiescent Current vs. Temperature – 50 mA Load

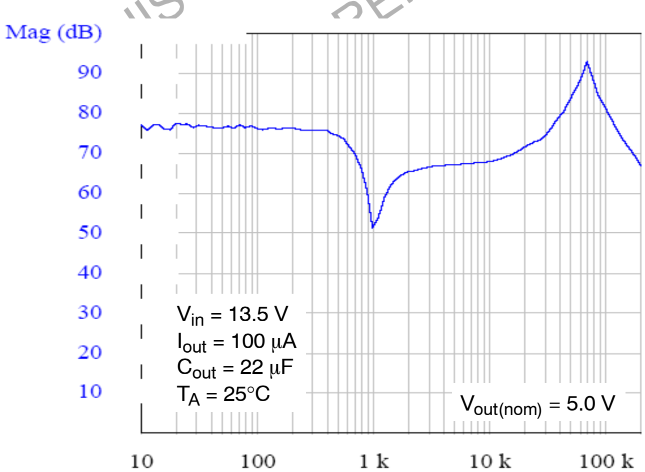


Figure 13. Power Supply Rejection – 100 μA

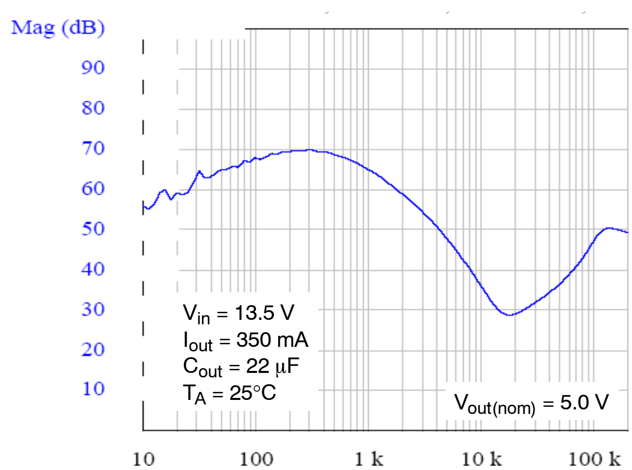


Figure 14. Power Supply Rejection – 350 mA

TYPICAL CHARACTERISTIC CURVES – 12 V OPTION

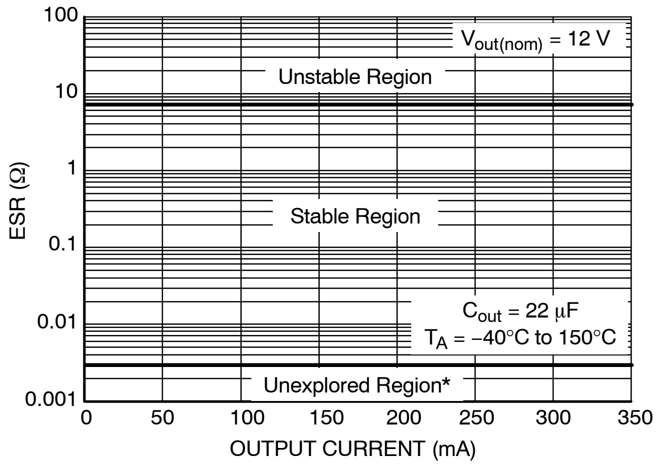


Figure 15. ESR Stability Region vs. Output Current

*The min specified ESR is based on Murata's capacitor GRM32ER71C226ME18 used in measurement. The true min ESR limit might be lower than shown.

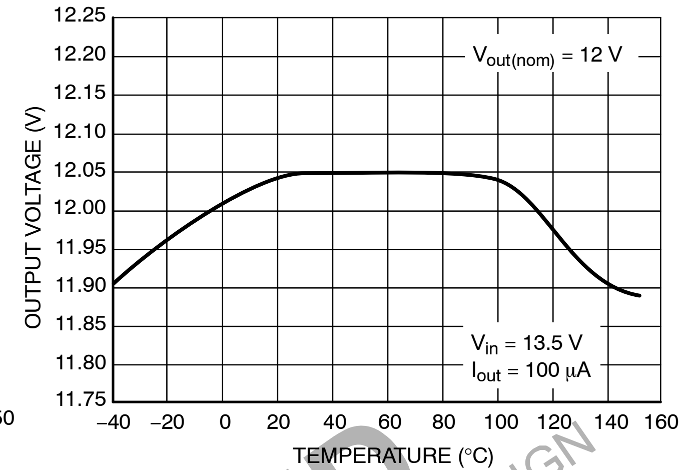


Figure 16. Output Voltage vs. Temperature

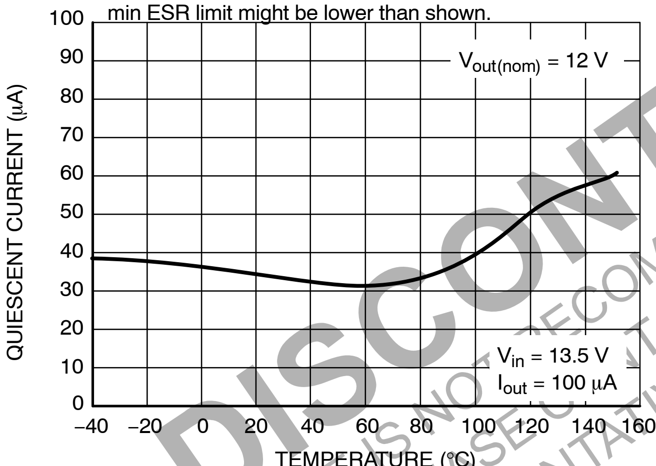


Figure 17. Quiescent Current vs. Temperature

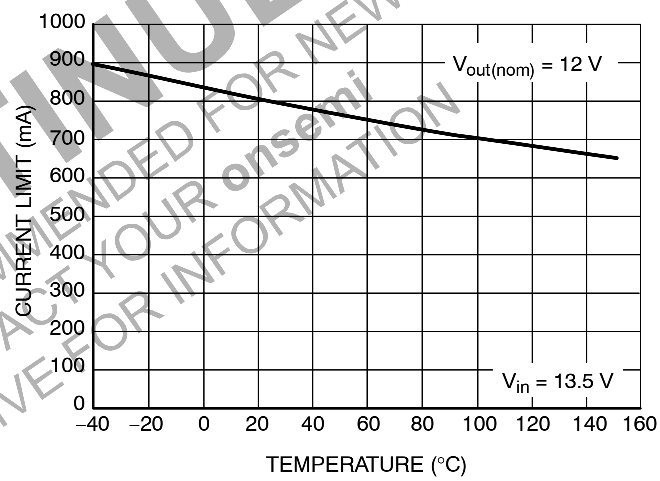


Figure 18. Current Limit vs. Temperature

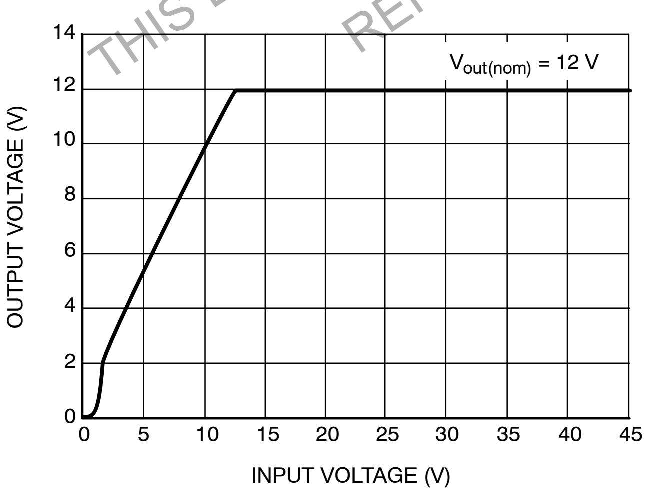


Figure 19. Output Voltage vs. Input Voltage

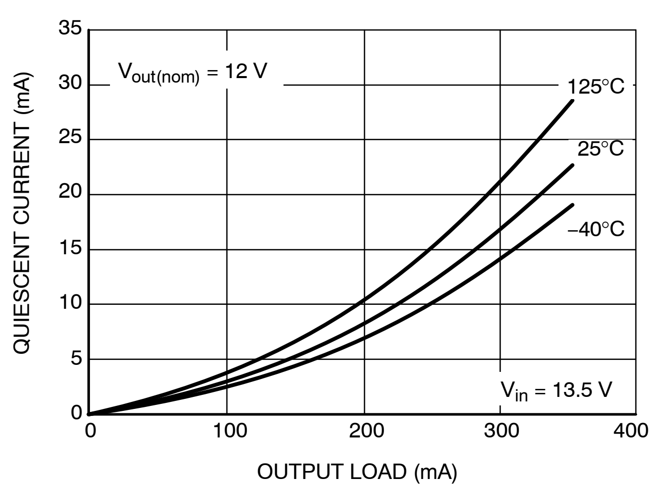


Figure 20. Quiescent Current vs. Output Load

TYPICAL CHARACTERISTIC CURVES – 12 V OPTION

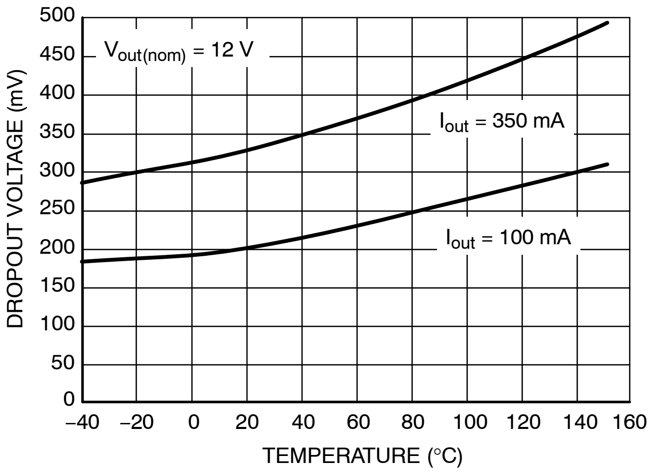


Figure 21. Dropout Voltage vs. Temperature

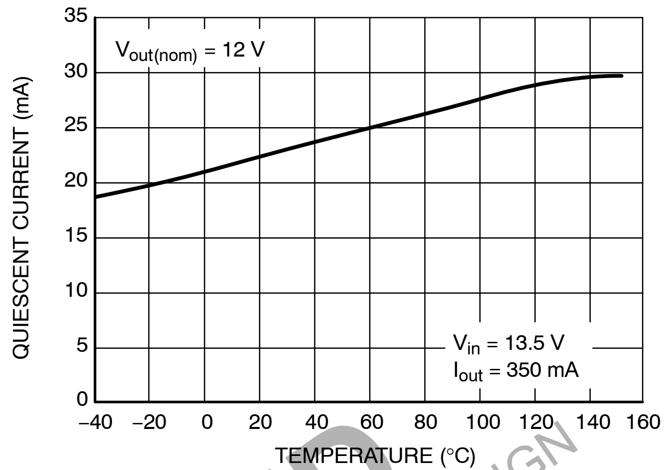


Figure 22. Quiescent Current vs. Temperature – 350 mA Load

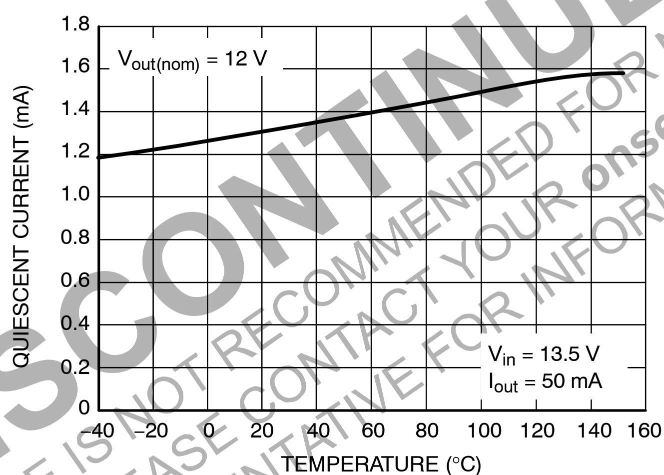


Figure 23. Quiescent Current vs. Temperature – 50 mA Load

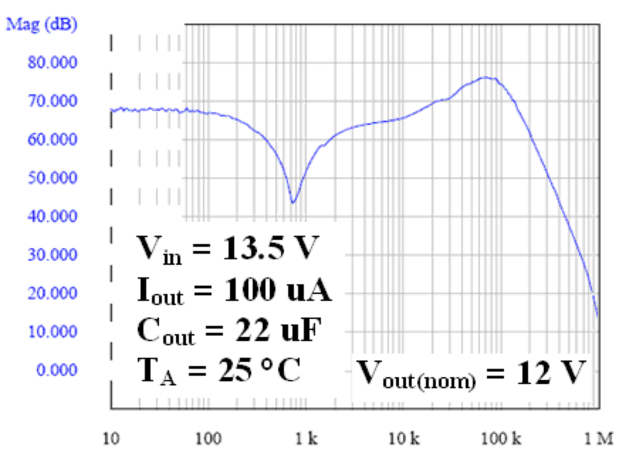


Figure 24. Power Supply Rejection – 100 μA

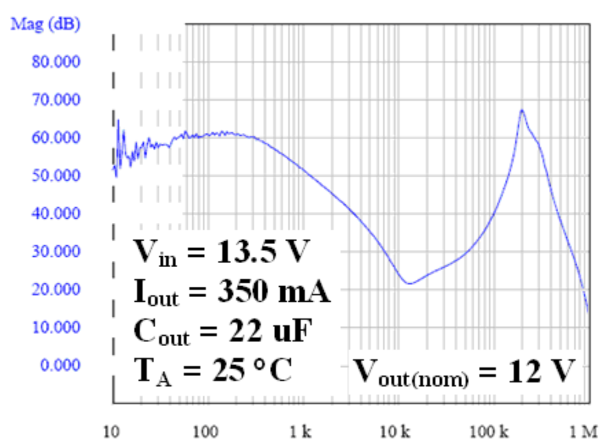


Figure 25. Power Supply Rejection – 350 mA

Circuit Description

The NCV8674 is a precision trimmed 5.0 V or 12 V fixed output regulator. Careful management of light load consumption combined with a low leakage process results in a typical quiescent current of 30 μA. The device has current capability of 350 mA, with 600 mV of dropout voltage at full rated load current. The regulation is provided by a PNP pass transistor controlled by an error amplifier with a bandgap reference. The regulator is protected by both current limit and short circuit protection. Thermal shutdown occurs above 150°C to protect the IC during overloads and extreme ambient temperatures.

Regulator

The error amplifier compares the reference voltage to a sample of the output voltage (V_{out}) and drives the base of a PNP series pass transistor by a buffer. The reference is a bandgap design to give it a temperature−stable output. Saturation control of the PNP is a function of the load current and input voltage. Over saturation of the output power device is prevented, and quiescent current in the ground pin is minimized. The NCV8674 is equipped with foldback current protection. This protection is designed to reduce the current limit during an overcurrent situation.

Regulator Stability Considerations

The input capacitor C_{IN} in Figure 2 is necessary for compensating input line reactance. Possible oscillations caused by input inductance and input capacitance can be damped by using a resistor of approximately 1 Ω in series with C_{IN}. The output or compensation capacitor, C_{OUT} helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. The capacitor value and type should be based on cost, availability, size and temperature constraints. Tantalum, aluminum electrolytic, film, or ceramic capacitors are all acceptable solutions, however, attention must be paid to ESR constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information. The value for the output capacitor C_{OUT} shown in Figure 2 should work for most applications; however, it is not necessarily the optimized solution. Stability is guaranteed at values $C_{OUT} \geq 22$ μF and ESR ≤ 7.0 Ω, within the operating temperature range. Actual limits are shown in a graph in the Typical Characteristics section.

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 2) is:

$$P_{D(max)} = [V_{IN(max)} - V_{OUT(min)}] \cdot I_{OUT(max)} + V_{IN(max)} \cdot I_q \quad \text{(eq. 1)}$$

Where:

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT(min)}$ is the minimum output voltage,

$I_{OUT(max)}$ is the maximum output current for the application, and I_q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of $P_{D(Max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = \frac{150^{o}C - T_A}{P_D} \quad \text{(eq. 2)}$$

The value of $R_{\theta JA}$ can then be compared with those in thermal resistance versus copper area graph (Figure 26). Those designs with cooling area corresponding to $R_{\theta JA}$'s less than the calculated value in Equation 2 will keep the die temperature below 150°C. The current flow and voltages are shown in the Measurement Circuit Diagram.

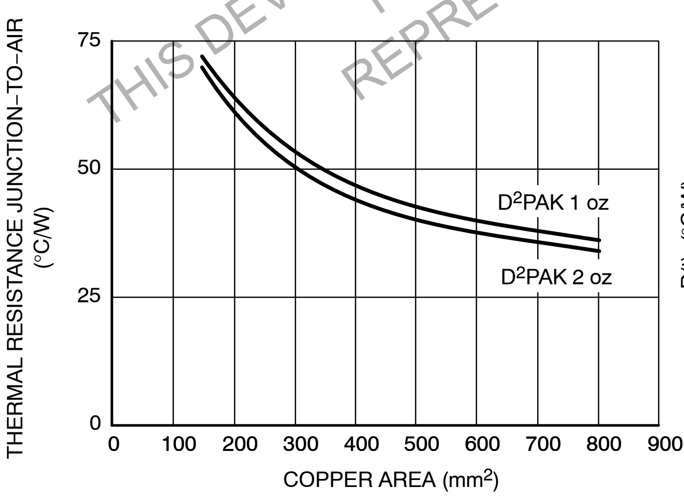


Figure 26.

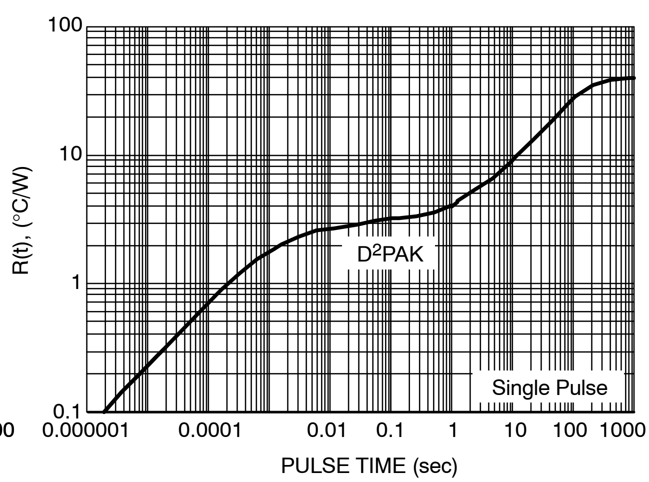
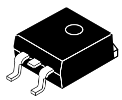


Figure 27. NCV8674 @ PCB Cu Area 650 mm^2 PCB Cu thk 1 oz

ORDERING INFORMATION

Device	Marking	Package	Shipping†
NCV8674DS50G	V867450	D^2PAK (Pb−Free)	50 Units / Rail
NCV8674DS50R4G	V867450	D^2PAK (Pb−Free)	800 / Tape & Reel
NCV8674DS120G	V8674120	D^2PAK (Pb−Free)	50 Units / Rail
NCV8674DS120R4G	V8674120	D^2PAK (Pb−Free)	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

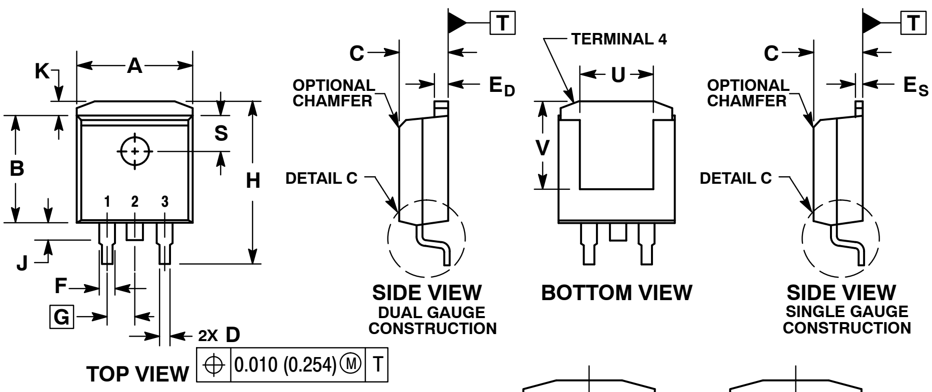


SCALE 1:1

D2PAK

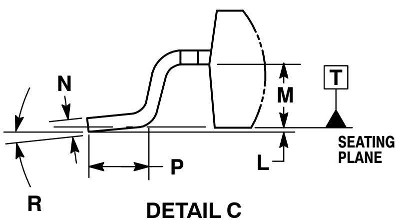
CASE 936−03
ISSUE E

DATE 29 SEP 2015

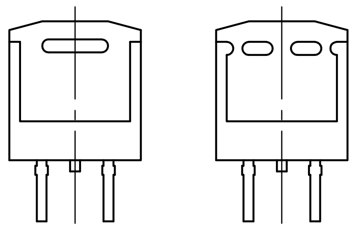


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCHES.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.
6. SINGLE GAUGE DESIGN WILL BE SHIPPED AFTER FPCN EXPIRATION IN OCTOBER 2011.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.386	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
E_D	0.045	0.055	1.143	1.397
E_S	0.018	0.026	0.457	0.660
F	0.051 REF		1.295 REF	
G	0.100 BSC		2.540 BSC	
H	0.539	0.579	13.691	14.707
J	0.125 MAX		3.175 MAX	
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	0°	8°	0°	8°
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	

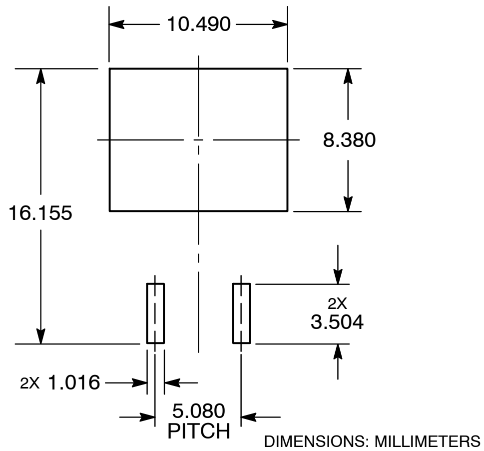


DETAIL C



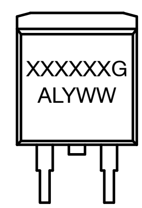
BOTTOM VIEW
OPTIONAL CONSTRUCTIONS

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**D2PAK**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
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onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales