

# NCV8512

## 5.0 V Micropower 150 mA LDO Linear Regulator with DELAY, Adjustable RESET, and Monitor FLAG

The NCV8512 is a 5.0 V precision micropower voltage regulator. The output current capability is 150 mA.

The output voltage is accurate within  $\pm 2.0\%$  with a maximum dropout voltage of 0.6 V at 150 mA. Low quiescent current is a feature drawing only 130  $\mu\text{A}$  with a 100  $\mu\text{A}$  load. This part is ideal for any and all battery operated microprocessor equipment.

Microprocessor control logic includes an active  $\overline{\text{RESET}}$  (with DELAY), and a FLAG monitor which can be used to provide an early warning signal to the microprocessor of a potential impending  $\overline{\text{RESET}}$  signal. The use of the FLAG monitor allows the microprocessor to finish any signal processing before the  $\overline{\text{RESET}}$  shuts the microprocessor down.

The active  $\overline{\text{RESET}}$  circuit operates correctly at an output voltage as low as 1.0 V. The  $\overline{\text{RESET}}$  function is activated during the power up sequence or during normal operation if the output voltage drops outside the regulation limits.

The reset threshold voltage can be decreased by the connection of an external resistor divider to  $R_{\text{ADJ}}$  lead.

The regulator is protected against reverse battery, short circuit, and thermal overload conditions. The device can withstand load dump transients making it suitable for use in automotive environments.

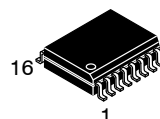
### Features

- 5.0 V  $\pm 2.0\%$  Output
- Low 130  $\mu\text{A}$  Quiescent Current
- Active  $\overline{\text{RESET}}$
- Adjustable Reset
- 150 mA Output Current Capability
- Fault Protection
  - +60 V Peak Transient Voltage
  - -15 V Reverse Voltage
  - Short Circuit
  - Thermal Overload
- Early Warning through  $\overline{\text{FLAG}}$ /MON Leads
- Thermally Enhanced in SOW-16 Exposed Pad
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes
- AEC Qualified
- PPAP Capable
- These are Pb-Free Devices



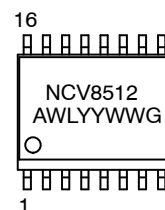
ON Semiconductor®

<http://onsemi.com>



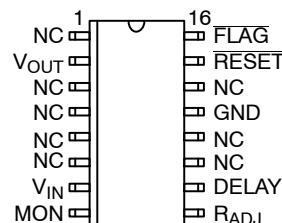
SOIC 16 LEAD  
WIDE BODY  
EXPOSED PAD  
PW SUFFIX  
CASE 751AG

### MARKING DIAGRAM



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Device

### PIN CONNECTIONS\*



\*Pin connections for reference only.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

## NCV8512

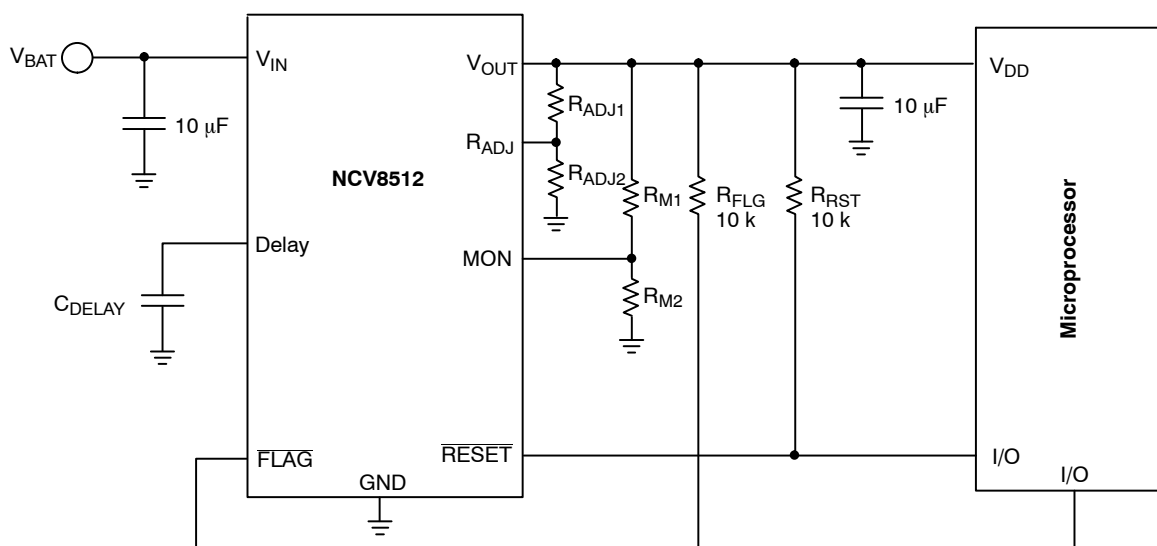


Figure 1. Application Diagram

### MAXIMUM RATINGS†

Rating	Value	Unit
V <sub>IN</sub> (DC)	–15 to 45	V
Peak Transient Voltage (46 V Load Dump @ V <sub>IN</sub> = 14 V). Voltage with respect to ground.	60	V
Operating Voltage	45	V
V <sub>OUT</sub> (DC)	16	V
Voltage Range (RESET, FLAG)	–0.3 to 10	V
Input Voltage Range (MON)	–0.3 to 10	V
V <sub>DELAY</sub>	–0.3 to 4.0	V
V <sub>RADJ</sub>	–0.3 to 10	V
ESD Susceptibility (Human Body Model)	2.0	kV
Junction Temperature, T <sub>J</sub>	–40 to +150	°C
Storage Temperature, T <sub>S</sub>	–55 to 150	°C
Package Thermal Resistance, SOW–16 E Pad: Junction–to–Case, R <sub>θJC</sub> Junction–to–Ambient, R <sub>θJA</sub>	16 57	°C/W
Lead Temperature Soldering:	Reflow: (SMD styles only) (Notes 1, 2, and 3)	265 peak
Moisture Sensitivity Level at 260°C	1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

† During the voltage range which exceeds the maximum tested voltage of V<sub>IN</sub>, operation is assured, but not specified. Wider limits may apply. Thermal dissipation must be observed closely.

- 60 second maximum above 217°C.
- 5°C/+0°C allowable conditions.
- Per IPC/JEDEC J–STD–020C.

# NCV8512

## ELECTRICAL CHARACTERISTICS ( $I_{OUT} = 1.0 \text{ mA}$ , $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ ; $6.0 \text{ V} < V_{IN} < 26 \text{ V}$ ; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
----------------	-----------------	-----	-----	-----	------

### OUTPUT STAGE

Output Voltage	$9.0 \text{ V} < V_{IN} < 16 \text{ V}$ , $100 \mu\text{A} \leq I_{OUT} \leq 150 \text{ mA}$	4.90	5.0	5.10	V
	$6.0 \text{ V} < V_{IN} < 26 \text{ V}$ , $100 \mu\text{A} \leq I_{OUT} \leq 150 \text{ mA}$	4.85	5.0	5.15	V
Dropout Voltage ( $V_{IN} - V_{OUT}$ )	$I_{OUT} = 150 \text{ mA}$	–	400	600	mV
	$I_{OUT} = 1.0 \text{ mA}$	–	100	150	mV
Load Regulation	$V_{IN} = 14 \text{ V}$ , $5.0 \text{ mA} \leq I_{OUT} \leq 150 \text{ mA}$	-30	5.0	30	mV
Line Regulation	$[V_{OUT}(\text{typ}) + 1.0] < V_{IN} < 26 \text{ V}$ , $I_{OUT} = 1.0 \text{ mA}$	–	15	60	mV
Quiescent Current, ( $I_Q$ ) Active Mode	$I_{OUT} = 100 \mu\text{A}$ , $V_{IN} = 12 \text{ V}$ , Delay = 3.0 V, MON = 3.0 V	–	130	200	$\mu\text{A}$
	$I_{OUT} = 75 \text{ mA}$ , $V_{IN} = 14 \text{ V}$ , Delay = 3.0 V, MON = 3.0 V	–	4.0	6.0	mA
	$I_{OUT} \leq 150 \text{ mA}$ , $V_{IN} = 14 \text{ V}$ , Delay = 3.0 V, MON = 3.0 V	–	12	19	mA
Current Limit	–	151	300	–	mA
Short Circuit Output Current	$V_{OUT} = 0 \text{ V}$	40	190	–	mA
Thermal Shutdown	(Guaranteed by Design)	150	180	–	$^{\circ}\text{C}$

### RESET FUNCTION (RESET)

RESET Threshold HIGH ( $V_{RH}$ ) LOW ( $V_{RL}$ )	$V_{OUT}$ Increasing	4.55	4.70	$0.98 \times V_{OUT}$	V
	$V_{OUT}$ Decreasing	4.50	4.60	$0.97 \times V_{OUT}$	V
Output Voltage Low ( $V_{RLO}$ )	$1.0 \text{ V} \leq V_{OUT} \leq V_{RL}$ , $R_{RESET} = 10 \text{ k}$	–	0.1	0.4	V
Delay Switching Threshold ( $V_{DT}$ )	–	1.4	1.8	2.2	V
Lower Delay Switching Threshold ( $V_{LD}$ )	–	0.3	0.45	0.6	V
Reset Delay Low Voltage	$V_{OUT} < \text{RESET Threshold Low}(\text{min})$	–	–	0.1	V
Delay Charge Current	DELAY = 1.0 V, $V_{OUT} > V_{RH}$	6.0	9.0	15	$\mu\text{A}$
Delay Discharge Current	DELAY = 1.0 V, $V_{OUT} = 1.5 \text{ V}$	5.0	–	–	mA
Reset Adjust Switching Voltage ( $V_{R(ADJ)}$ )	–	1.23	1.31	1.39	V

### FLAG/MONITOR

Monitor Threshold	Increasing and Decreasing	1.10	1.20	1.31	V
Hysteresis	–	20	50	100	mV
Input Current	MON = 2.0 V	–0.5	0.1	0.5	$\mu\text{A}$
Output Saturation Voltage	MON = 0 V, $I_{FLAG} = 1.0 \text{ mA}$	–	0.1	0.4	V

# PACKAGE PIN DESCRIPTION

Package Pin Number	Pin Symbol	Function
SOW-16 Exposed Pad		
1, 3-6, 11, 12, 14	NC	No connection.
2	V <sub>OUT</sub>	±2.0%, 150 mA output.
7	V <sub>IN</sub>	Input Voltage.
8	MON	Monitor. Input for early warning comparator. If not needed connect to V <sub>OUT</sub> .
9	R <sub>ADJ</sub>	Reset Adjust. If not needed connect to ground.
10	DELAY	Timing capacitor for RESET function.
13	GND	Ground. All GND leads must be connected to Ground.
15	RESET	Active reset (accurate to V <sub>OUT</sub> ≥ 1.0 V).
16	FLAG	Open collector output from early warning comparator.

## TYPICAL PERFORMANCE CHARACTERISTICS

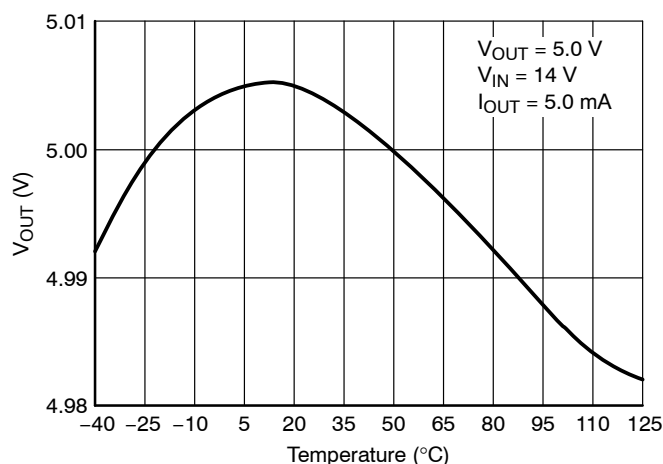


Figure 2. Output Voltage vs. Temperature

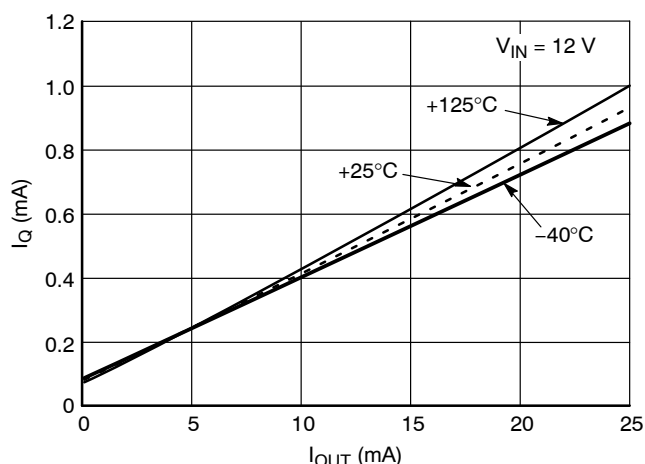


Figure 3. Quiescent Current vs. Output Current

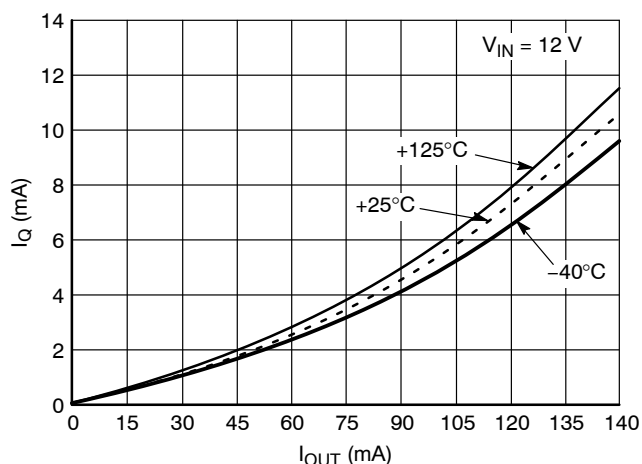


Figure 4. Quiescent Current vs. Output Current

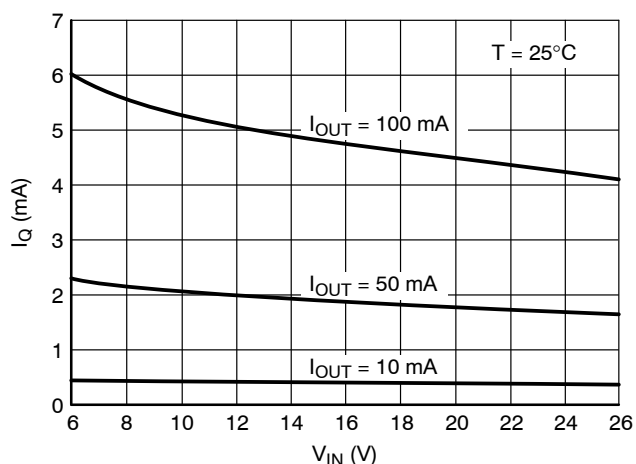


Figure 5. Quiescent Current vs. Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

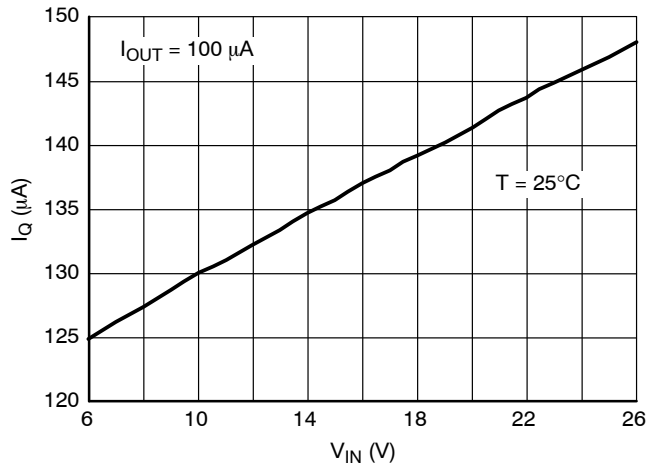


Figure 6. Quiescent Current vs. Input Voltage

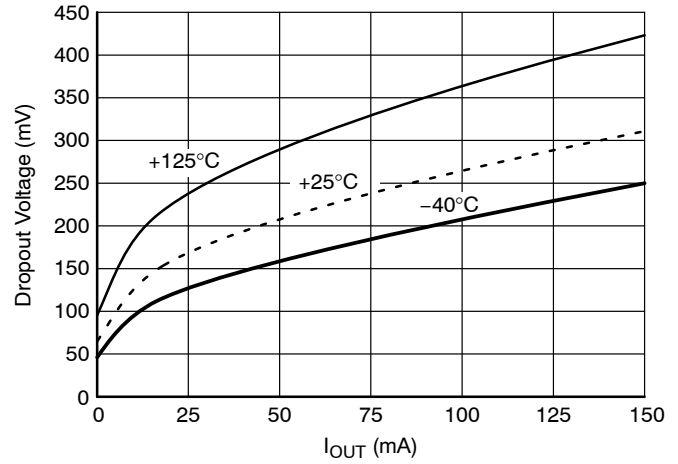


Figure 7. Dropout Voltage vs. Output Current

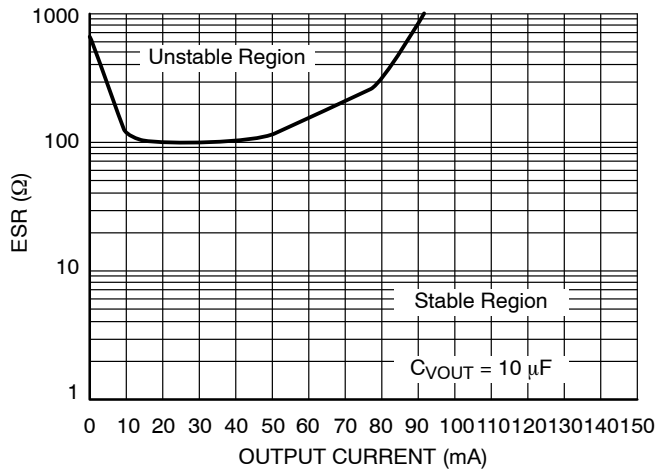


Figure 8. Output Capacitor ESR

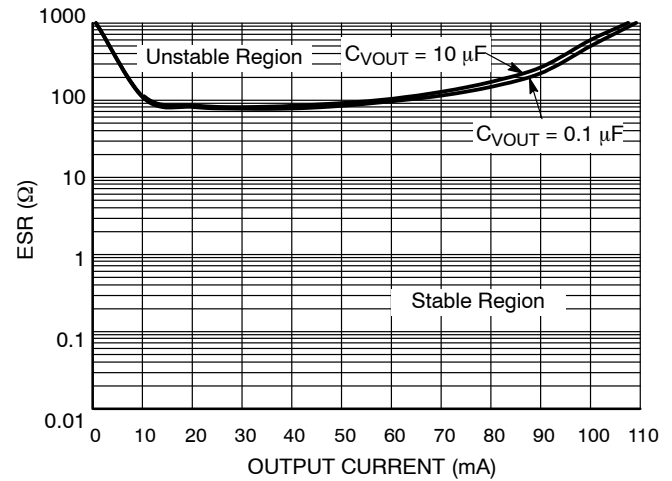


Figure 9. Output Stability with Output Capacitor Change

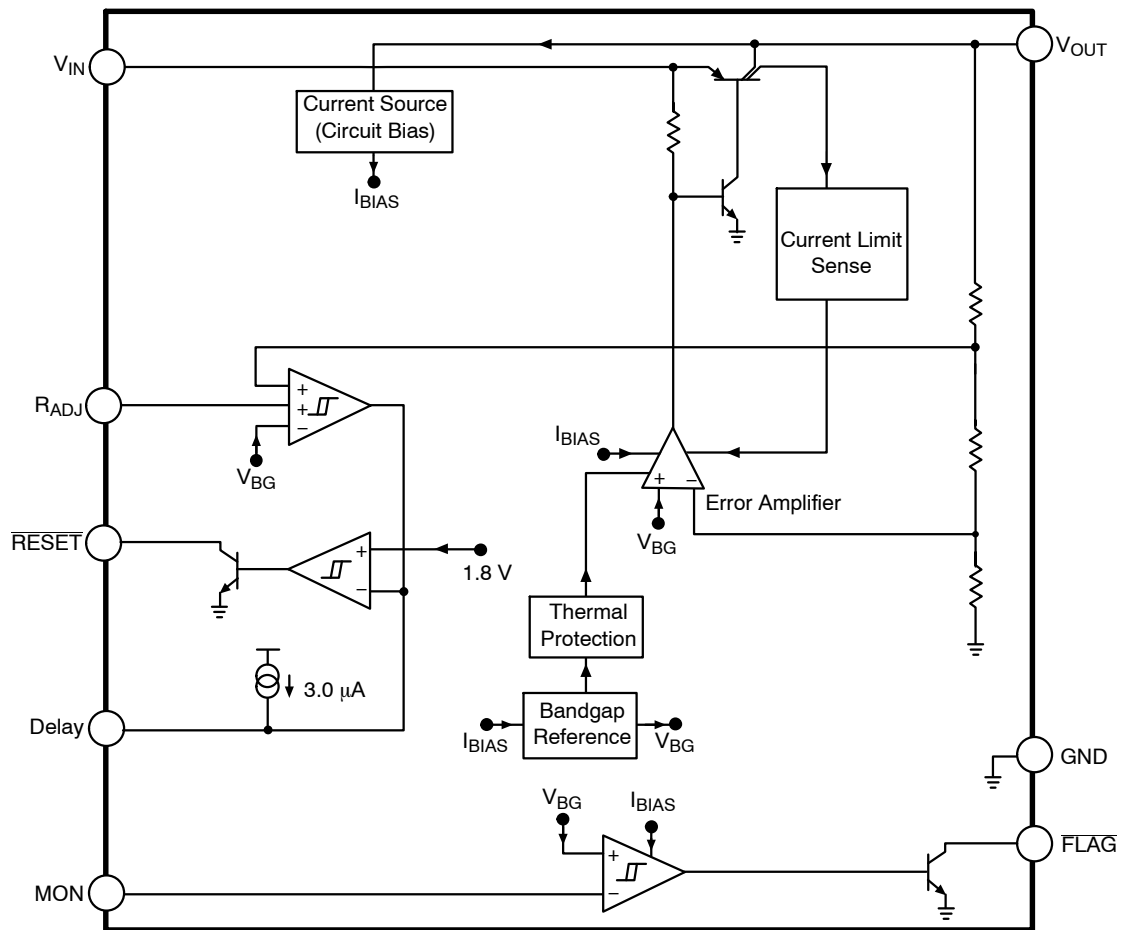


Figure 10. Block Diagram

## CIRCUIT DESCRIPTION

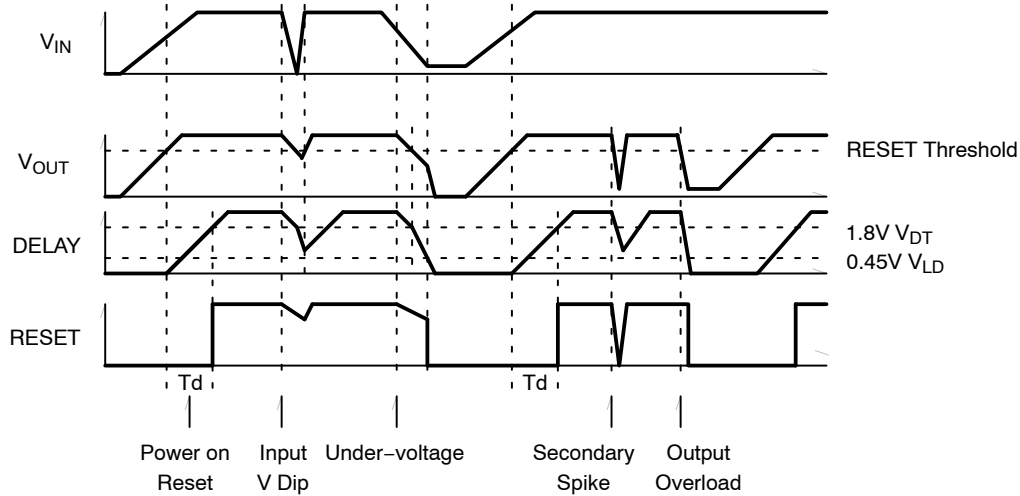


Figure 11. Reset and Delay Circuit Wave Forms

### REGULATOR CONTROL FUNCTIONS

The NCV8512 contains a microprocessor-compatible control function  $\overline{\text{RESET}}$  (Figure 11).

#### RESET Function

A  $\overline{\text{RESET}}$  signal (low voltage) is generated as the IC powers up. After  $V_{\text{OUT}}$  increases above the  $\overline{\text{RESET}}$  threshold, the DELAY timer is started. When the DELAY timer passes 1.8 V, the  $\overline{\text{RESET}}$  signal goes high. A discharge of the DELAY timer is started when  $V_{\text{OUT}}$  drops and stays below the  $\overline{\text{RESET}}$  threshold. When the DELAY timer level drops below 0.45 V, the  $\overline{\text{RESET}}$  signal is brought low.

The  $\overline{\text{RESET}}$  output is an open collector NPN transistor, controlled by a low voltage detection circuit. The circuit is functionally independent of the rest of the IC thereby guaranteeing that the  $\overline{\text{RESET}}$  signal is valid for  $V_{\text{OUT}}$  as low as 1.0 V.

#### Adjustable Reset Function

The reset threshold VRL can be decreased from a typical value of 4.65 V to as low as 3.5 V by using an external voltage divider connected from  $V_{\text{OUT}}$  to the pin  $R_{\text{ADJ}}$  as displayed in Figure 12. The resistor divider keeps the voltage above the  $V_{\text{RADJ.TH}}$  (typical 1.31 V) and overrides the internal threshold detector. Adjust the voltage divider according to the following relationship:

$$V_{\text{THRES}} = V_{\text{RADJ.TH}} \times \frac{R_{\text{ADJ1}} + R_{\text{ADJ2}}}{R_{\text{ADJ2}}} \quad (2)$$

Where;

$V_{\text{THRES}}$  is the desired output threshold voltage that starts the time delay for Power on Reset Delay.

$V_{\text{RADJ.TH}}$  is the default threshold voltage of 1.31 V typ.

$R_{\text{ADJ1}}$  is the resistor connected from the 5 V output to the  $R_{\text{ADJ}}$  pin.

$R_{\text{ADJ2}}$  is the resistor connected from the  $R_{\text{ADJ}}$  pin to ground.

If the reset adjust option is not needed, the  $R_{\text{ADJ}}$  pin should be connected to GND causing the reset threshold to go to its default value (4.65 V typical).

As an example, select resistors to give a threshold voltage of 4.0 V. This will allow the delay timer to start when the output crosses the 4.0 V level.

$$V_{\text{THRES}} = 4.0 \text{ V} = 1.31 \text{ V} \times (R_{\text{ADJ1}} + R_{\text{ADJ2}}) / R_{\text{ADJ2}}$$

Let  $R_{\text{ADJ2}}$  be 100 k $\Omega$  for low current consumption.

$$R_{\text{ADJ1}} = 2.05 \times 100 \text{ k} = 205 \text{ k}$$

With 5 V on the output, the voltage on the  $R_{\text{ADJ}}$  pin will be 1.64 V.

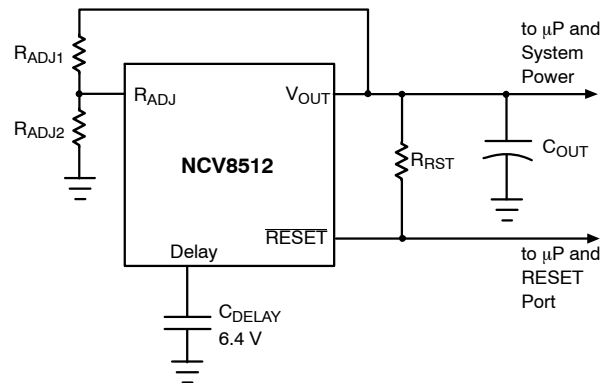


Figure 12. Adjustable  $\overline{\text{RESET}}$

#### DELAY Function

The reset delay circuit provides a delay (programmable by external capacitor) on the  $\overline{\text{RESET}}$  output lead.

The DELAY lead provides source current (typically 9  $\mu\text{A}$ ) to the external DELAY capacitor at the following times:

1. During Power Up (once the regulation threshold has been exceeded).

- After a reset event has occurred and the device is back in regulation. The DELAY capacitor is discharged when the regulation ( $\overline{\text{RESET}}$  threshold) has been violated. When the DELAY capacitor discharges to 0.45 V, the  $\overline{\text{RESET}}$  signal pulls low.

### FLAG/Monitor Function

An on-chip comparator is available to provide an early warning to the microprocessor of a possible reset signal. The reset signal typically turns the microprocessor off instantaneously. This can cause unpredictable results with the microprocessor. The signal received from the  $\overline{\text{FLAG}}$  pin will allow the microprocessor time to complete its present task before shutting down. This function is performed by a comparator referenced to the bandgap voltage. The actual

trip point can be programmed externally using a resistor divider to the input monitor (MON) (Figure 13). The typical threshold is 1.20 V on the MON Pin.

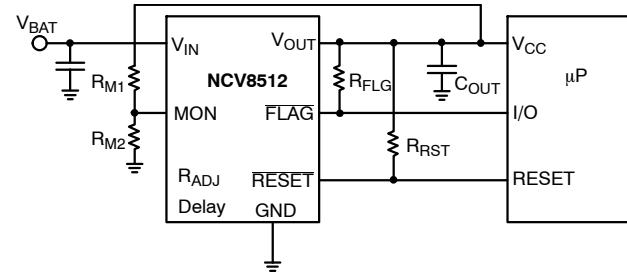


Figure 13. FLAG/Monitor Function

## APPLICATION NOTES

### FLAG MONITOR

Figure 14 shows the FLAG Monitor waveforms taken from the circuit depicted in Figure 13. As the output voltage falls ( $V_{\text{OUT}}$ ), the Monitor threshold is crossed. This causes the voltage on the  $\overline{\text{FLAG}}$  output to go low sending a warning signal to the microprocessor that a  $\overline{\text{RESET}}$  signal may occur in a short period of time.  $T_{\text{WARNING}}$  is the time the microprocessor has to complete the function it is currently working on and get ready for the  $\overline{\text{RESET}}$  shutdown signal.

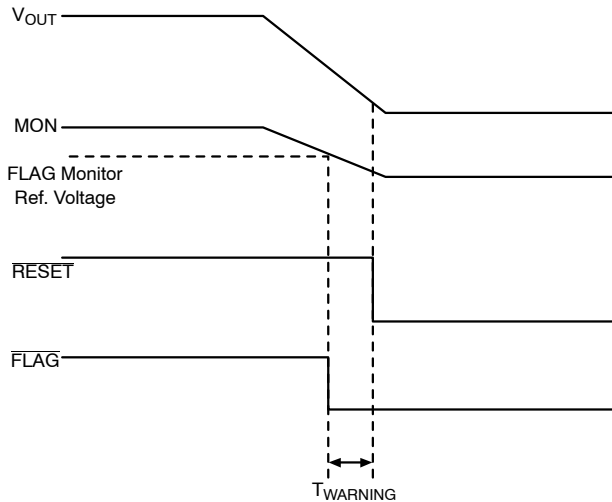


Figure 14. FLAG Monitor Circuit Waveform

### SETTING THE DELAY TIME

The delay time is controlled by the Reset Delay Low Voltage, Delay Switching Threshold, and the Delay Charge Current. The delay follows the equation:

$$t_{\text{DELAY}} = \frac{C_{\text{DELAY}}(V_{\text{DT}} - \text{Reset Delay Low Voltage})}{\text{Delay Charge Current}}$$

Example:

Using  $C_{\text{DELAY}} = 33 \text{ nF}$ .

Use the typical value for Delay Low Voltage = 0.04 V.

Use the typical value for  $V_{\text{DT}} = 1.8 \text{ V}$ .

Use the typical value for Delay Charge Current =  $9.0 \mu\text{A}$ .

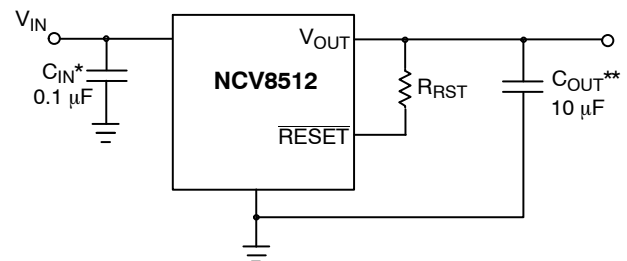
$$t_{\text{DELAY}} = \frac{[33 \text{ nF}(1.8 - 0.04 \text{ V})]}{9.0 \mu\text{A}} = 6.45 \text{ ms}$$

### STABILITY CONSIDERATIONS

The output or compensation capacitor helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures ( $-25^{\circ}\text{C}$  to  $-40^{\circ}\text{C}$ ), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information.

The value for the output capacitor  $C_{\text{OUT}}$  shown in Figure 15 should work for most applications, but is not necessarily the optimized solution.



\* $C_{\text{IN}}$  required if regulator is located far from the power supply filter.

\*\* $C_{\text{OUT}}$  required for stability. Capacitor must operate at minimum temperature expected.

Figure 15. Test and Application Circuit Showing Output Compensation



## CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 16) is:

$$P_{D(max)} = [V_{IN(max)} - V_{OUT(min)}]I_{OUT(max)} + V_{IN(max)}I_Q \quad (1)$$

where:

$V_{IN(max)}$  is the maximum input voltage,

$V_{OUT(min)}$  is the minimum output voltage,

$I_{OUT(max)}$  is the maximum output current for the application, and

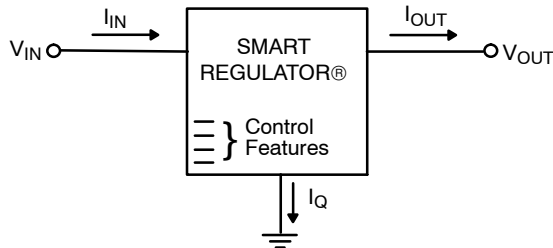
$I_Q$  is the quiescent current the regulator consumes at  $I_{OUT(max)}$ .

Once the value of  $P_{D(max)}$  is known, the maximum permissible value of  $R_{\theta JA}$  can be calculated:

$$R_{\theta JA} = \frac{150^\circ C - T_A}{P_D} \quad (2)$$

The value of  $R_{\theta JA}$  can then be compared with those in the package section of the data sheet. Those packages with  $R_{\theta JA}$ 's less than the calculated value in equation 2 will keep the die temperature below  $150^\circ C$ .

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.



**Figure 16. Single Output Regulator with Key Performance Parameters Labeled**

## HEATSINKS

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of  $R_{\theta JA}$ :

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (3)$$

where:

$R_{\theta JC}$  = the junction-to-case thermal resistance,

$R_{\theta CS}$  = the case-to-heatsink thermal resistance, and

$R_{\theta SA}$  = the heatsink-to-ambient thermal resistance.

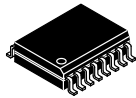
$R_{\theta JC}$  appears in the package section of the data sheet. Like  $R_{\theta JA}$ , it too is a function of package type.  $R_{\theta CS}$  and  $R_{\theta SA}$  are functions of the package type, heatsink and the interface between them. These values appear in heatsink data sheets of heat sink manufacturers.

Further mounting and cooling information is available in the application note, AN1040/D, "Mounting Considerations for Power Semiconductors" located in the ON Semiconductor web site.

## ORDERING INFORMATION

Device	Output Voltage	Package	Shipping <sup>†</sup>
NCV8512PW50G	5.0 V	SOW-16 E Pad (Pb-Free)	47 Units / Rail
NCV8512PW50R2G			1000 / Tape & Reel

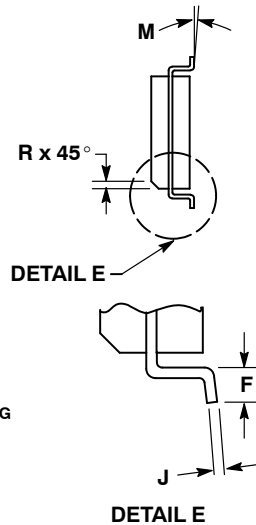
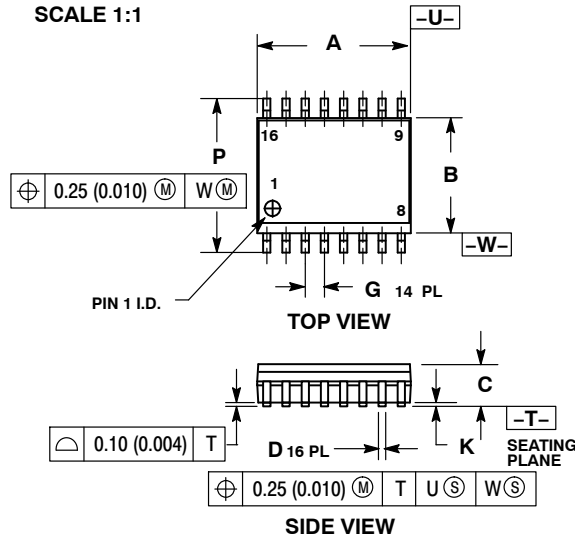
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 1:1

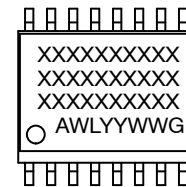
**SOIC 16 LEAD WIDE BODY, EXPOSED PAD**  
**CASE 751AG**  
**ISSUE B**

DATE 31 MAY 2016


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751R-01 OBSOLETE, NEW STANDARD 751R-02.

DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
H	3.45	3.66	0.136	0.144
J	0.25	0.32	0.010	0.012
K	0.00	0.10	0.000	0.004
L	4.72	4.93	0.186	0.194
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

**GENERIC MARKING DIAGRAM\***


XXXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

<b>DOCUMENT NUMBER:</b>	<b>98AON21237D</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SOIC-16, WB EXPOSED PAD</b>	<b>PAGE 1 OF 1</b>

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at  
[www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)