NCV8141

Linear Regulator - ENABLE, RESET, Watchdog

5.0 V, 500 mA

The NCV8141 is a linear regulator suited for microprocessor applications in automotive environments. This ON Semiconductor part provides the power for the microprocessors along with many of the control functions needed in today’s computer based systems. Incorporating all of these features saves both cost, and board space.

The NCV8141 provides a low sleep mode current as compared to the CS8141. Consult your local sales representative for a low sleep mode current version of the CS8140.

Features

- 5.0 V ± 3.0%, 500 mA Output Voltage
- Lower Quiescent Current
- Improved Filtering for /RESET Functionality
- µP Compatible Control Functions
  - Watchdog
  - RESET
  - ENABLE
- Low Dropout Voltage (1.25 V @ 500 mA)
- Low Quiescent Current (7.0 mA @ 500 mA)
- Low Noise, Low Drift
- Low Current SLEEP Mode 50 µA (max)
- Fault Protection
  - Thermal Shutdown
  - Short Circuit
  - 60 V Peak Transient Voltage
- These are Pb–Free Devices
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes

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ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package</th>
<th>Shipping†</th>
</tr>
</thead>
<tbody>
<tr>
<td>NCV8141D2TG</td>
<td>D²PAK (Pb–Free)</td>
<td>50 Units/Rail</td>
</tr>
<tr>
<td>NCV8141D2TR4G</td>
<td>D²PAK (Pb–Free)</td>
<td>750/Tape &amp; Reel</td>
</tr>
</tbody>
</table>

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
**PIN FUNCTION DESCRIPTION**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Symbol</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>V_{IN}</td>
<td>Supply voltage to IC, usually direct from the battery.</td>
</tr>
<tr>
<td>2</td>
<td>ENABLE</td>
<td>CMOS compatible logical input. V_{OUT} is disabled when ENABLE is LOW and WDI is invalid.</td>
</tr>
<tr>
<td>3</td>
<td>RESET</td>
<td>CMOS compatible output lead. RESET goes low whenever V_{OUT} drops 4.5% below its typical value for more than 2.0 ms or WDI signal falls below the watchdog threshold frequency.</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>Ground Connection.</td>
</tr>
<tr>
<td>5</td>
<td>Delay</td>
<td>Timing capacitor for Watchdog and RESET functions.</td>
</tr>
<tr>
<td>6</td>
<td>WDI</td>
<td>CMOS compatible input lead. The Watchdog function monitors the falling edge of the incoming digital pulse train. The signal is usually generated by the system microprocessor.</td>
</tr>
<tr>
<td>7</td>
<td>V_{OUT}</td>
<td>Regulated output voltage, 5.0 V (typ).</td>
</tr>
</tbody>
</table>
## MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Operating Range</td>
<td>−0.5 to 26</td>
<td>V</td>
</tr>
<tr>
<td>Peak Transient Voltage (46 V Load Dump @ 14 V VBAT)</td>
<td>60</td>
<td>V</td>
</tr>
<tr>
<td>Electrostatic Discharge (Human Body Model)</td>
<td>4.0</td>
<td>kV</td>
</tr>
<tr>
<td>WDI Input Signal Range</td>
<td>−0.3 to 7.0</td>
<td>V</td>
</tr>
<tr>
<td>Internal Power Dissipation</td>
<td>Internally Limited</td>
<td>–</td>
</tr>
<tr>
<td>Junction Temperature Range (TJ)</td>
<td>−40 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>−65 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>ENABLe</td>
<td>−0.3 to VIN</td>
<td>V</td>
</tr>
<tr>
<td>Package Thermal Resistance, D²PAK 7–Pin</td>
<td>1.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction–to–Case, RINJA</td>
<td>10–50†</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction–to–Ambient, RINA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lead Temperature Soldering: Reflow (SMD styles only) (Note 1)</td>
<td>225 peak (Note 2)</td>
<td>°C</td>
</tr>
</tbody>
</table>

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Depending on thermal properties of substrate RINJA = RINJC + RICA.
1. 60 seconds max above 183°C.
2. −5.0°C/+0°C allowable conditions.

## ELECTRICAL CHARACTERISTICS (7.0 ≤ VIN ≤ 26 V, 5.0 mA ≤ IOUT ≤ 500 mA, −40°C ≤ TJ ≤ 150°C, −40°C ≤ TA ≤ 125°C, unless otherwise noted.) (Note 3)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Stage (VOUT)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Voltage, VOUT</td>
<td>7.0 V ≤ VIN ≤ 26 V, 5.0 mA &lt; IOUT &lt; 500 mA</td>
<td>4.85</td>
<td>5.0</td>
<td>5.15</td>
<td>V</td>
</tr>
<tr>
<td>Dropout Voltage (VIN – VOUT)</td>
<td>IOUT = 500 mA</td>
<td>–</td>
<td>1.25</td>
<td>1.50</td>
<td>V</td>
</tr>
<tr>
<td>Line Regulation</td>
<td>IOUT = 50 mA, 7.0 V ≤ VIN ≤ 26 V,</td>
<td>–</td>
<td>5.0</td>
<td>25</td>
<td>mV</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>VIN = 14 V, 50 mA ≤ IOUT ≤ 500 mA</td>
<td>–</td>
<td>5.0</td>
<td>80</td>
<td>mV</td>
</tr>
<tr>
<td>Output Impedance, ROUT</td>
<td>500 mA DC and 10 mA AC, 100 Hz ≤ f ≤ 10 kHz</td>
<td>–</td>
<td>200</td>
<td>–</td>
<td>mΩ</td>
</tr>
<tr>
<td>Quiescent Current, (IQ)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Active Mode</td>
<td>0 ≤ IOUT ≤ 500 mA, 7.0 V ≤ VIN ≤ 26 V</td>
<td>–</td>
<td>7.0</td>
<td>15</td>
<td>µA</td>
</tr>
<tr>
<td>Sleep Mode</td>
<td>IOUT = 0 mA, VIN = 13 V, ENABLE = 0 V</td>
<td>–</td>
<td>25</td>
<td>50</td>
<td>µA</td>
</tr>
<tr>
<td>Ripple Rejection</td>
<td>7.0 V ≤ VIN ≤ 17 V, IOUT = 250 mA, f = 120 Hz</td>
<td>60</td>
<td>75</td>
<td>–</td>
<td>dB</td>
</tr>
<tr>
<td>Current Limit</td>
<td>VIN = 7.0 V, VOUT = 4.5 V</td>
<td>600</td>
<td>1200</td>
<td>2000</td>
<td>mA</td>
</tr>
<tr>
<td>Thermal Shutdown</td>
<td>Guaranteed by Design</td>
<td>150</td>
<td>180</td>
<td>–</td>
<td>°C</td>
</tr>
<tr>
<td>Overvoltage Shutdown</td>
<td>VOUT &lt; 1.0 V</td>
<td>30</td>
<td>34</td>
<td>38</td>
<td>V</td>
</tr>
</tbody>
</table>

## ENABLE

<table>
<thead>
<tr>
<th>Threshold</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>HIGH</td>
<td>VOUT ≥ 0.5 V, (VOUT(ON))</td>
<td>–</td>
</tr>
<tr>
<td>LOW</td>
<td>VOUT &lt; 0.5 V, (VOUT(OFF))</td>
<td>3.5</td>
</tr>
<tr>
<td>Input Current</td>
<td></td>
<td></td>
</tr>
<tr>
<td>HIGH</td>
<td>ENABLE = 5.0 V</td>
<td>–</td>
</tr>
<tr>
<td>LOW</td>
<td>ENABLE = 0 V</td>
<td>–1.0</td>
</tr>
<tr>
<td>Threshold Hysteresis</td>
<td>(HIGH – LOW)</td>
<td>–</td>
</tr>
</tbody>
</table>

3. To observe safe operating junction temperatures, low duty cycle pulse testing is used in tests where applicable.

http://onsemi.com
### Electrical Characteristics (continued)

(7.0 ≤ \( V_{IN} \) ≤ 26 V, 5.0 mA ≤ \( I_{OUT} \) ≤ 500 mA, −40°C ≤ \( T_J \) ≤ 150°C, −40°C ≤ \( T_A \) ≤ 125°C, unless otherwise noted.) (Note 4)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESET</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Threshold HIGH ( V_{R(HI)} )</td>
<td>( V_{OUT} ) Increasing</td>
<td>4.65</td>
<td>4.90</td>
<td>( V_{OUT} - 0.05 )</td>
<td>V</td>
</tr>
<tr>
<td>Threshold LOW ( V_{R(LOW)} )</td>
<td>( V_{OUT} ) Decreasing</td>
<td>4.50</td>
<td>4.70</td>
<td>4.90</td>
<td>V</td>
</tr>
<tr>
<td>Threshold Hysteresis ( (V_{RHI} - LOW) )</td>
<td></td>
<td>150</td>
<td>200</td>
<td>250</td>
<td>mV</td>
</tr>
<tr>
<td>RESET Output Leakage ( \text{RESET} = \text{HIGH} )</td>
<td>( V_{OUT} \geq V_{R(HI)} )</td>
<td>–</td>
<td>–</td>
<td>25</td>
<td>( \mu )A</td>
</tr>
<tr>
<td>Output Voltage Low ( (V_{L(LOW)}) )</td>
<td>( 1.0 ) V ≤ ( V_{OUT} ) ≤ ( V_{R(LOW)} ), ( R_P ) = 2.7 kΩ (Note 5)</td>
<td>–</td>
<td>0.1</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>Output Voltage Low ( (V_{\text{peak}}) )</td>
<td>( V_{OUT} ), Power up, Power down</td>
<td>–</td>
<td>0.6</td>
<td>1.0</td>
<td>V</td>
</tr>
<tr>
<td>Delay Time ( t_{POR} )</td>
<td>( C_{DELAY} = 0.1 ) μF</td>
<td>30</td>
<td>47.5</td>
<td>65</td>
<td>ms</td>
</tr>
<tr>
<td>Delay Time ( t_{WDI(RESET)} )</td>
<td>( C_{DELAY} = 0.1 ) μF</td>
<td>0.5</td>
<td>1.0</td>
<td>1.5</td>
<td>ms</td>
</tr>
</tbody>
</table>

**Watchdog**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage High</td>
<td></td>
<td>2.0</td>
<td>–</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>Input Voltage Low</td>
<td></td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>0.8</td>
</tr>
<tr>
<td>Input Current WDI ≤ ( V_{OUT} )</td>
<td></td>
<td>–</td>
<td>0</td>
<td>10</td>
<td>( \mu )A</td>
</tr>
<tr>
<td>Threshold Frequency ( f_{WDI} ) ( C_{DELAY} = 0.1 ) μF</td>
<td></td>
<td>64</td>
<td>77</td>
<td>105</td>
<td>Hz</td>
</tr>
</tbody>
</table>

4. To observe safe operating junction temperatures, low duty cycle pulse testing is used in tests where applicable.
5. \( R_P \) is connected to \( \text{RESET} \) and \( V_{OUT} \).
TYPICAL PERFORMANCE CHARACTERISTICS

Figure 2. Dropout Voltage vs. Output Current over Temperature

Figure 3. Dropout Voltage vs. Temperature

Figure 4. Output Stability

Figure 5. Output Stability with Capacitor Change

Figure 6. Delay Time

NOTE: At 125°C an additional area of instability occurs (0.1 μF only) for loads less than 5 mA and low ESR.

NOTE: At 25°C an additional area of instability occurs (0.1 μF only) for loads less than 5 mA and low ESR.
NCV8141

DEFINITION OF TERMS

Dropout Voltage: The input–output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14 V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Quiescent Current: The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak–to–peak input ripple voltage to the peak–to–peak output ripple voltage.

Current Limit: Peak current that can be delivered to the output.

CIRCUIT DESCRIPTION

The NCV8141 is a 5.0 V Watchdog Regulator with protection circuitry and three logic control functions that allow a microprocessor to control its own power supply. The NCV8141 is designed for use in automotive, switch mode power supply post regulator, and battery powered systems.

Basic regulator performance characteristics include a low noise, low drift, 5.0 V ±3.0% precision output voltage with low dropout voltage (1.25 V @ IOUT = 500 mA) and low quiescent current (7.0 mA @ IOUT = 500 mA). On board short circuit, thermal, and overvoltage protection make it possible to use this regulator in particularly harsh operating environments.

The Watchdog logic function monitors an input signal (WDI) from the microprocessor or other signal source. When the signal frequency goes below the externally programmable limit, a RESET signal is generated (RESET). Proper operation has been verified at a frequency up to 100 kHz. No abnormal RESET signals will occur with frequencies lower than 100 kHz and the maximum Threshold Frequency (96 Hz). An external capacitor (CDELAY) programs the watchdog frequency limit as well as the power on reset (POR) and RESET delay.

The RESET function is activated by any of three conditions: the watchdog signal moves outside of its preset limits; the output voltage drops out of regulation by more than 4.5%; or the IC is in its power up sequence. The RESET signal is independent of VIN and reliable down to VOUT = 1.0 V.

In conjunction with the Watchdog, the ENABLE function controls the regulator’s power consumption. The NCV8141’s output stage and its attendant circuitry are enabled by setting the ENABLE lead high. The regulator goes into sleep mode when the ENABLE lead goes low and the watchdog signal moves outside its preset limit. This unique combination of control functions in the NCV8141 gives the microprocessor control over its own power down sequence: i.e. it gives the microprocessor the flexibility to perform housekeeping functions before it powers down.

VOLTAGE REFERENCE AND OUTPUT CIRCUITRY

Precision Voltage Reference

The regulated output voltage depends on the precision band gap voltage reference in the IC. By adding an error amplifier into the feedback loop, the output voltage is maintained within ±3.0% over temperature and supply variation.

Output Stage

The composite PNP–NPN output structure (Figure 7) provides 500 mA (min) of output current while maintaining a low drop out voltage (1.25 V) and drawing little quiescent current (7.0 mA).

The NPN pass device prevents deep saturation of the output stage which in turn improves the IC’s efficiency by preventing excess current from being used and dissipated by the IC.

Output Stage Protection

The output stage is protected against overvoltage, short circuit and thermal runaway conditions (Figure 8).

If the input voltage rises above 30 V (e.g. load dump), the output shuts down. This response protects the internal circuitry and enables the IC to survive unexpected voltage transients.
Using an emitter sense scheme, the amount of current through the NPN pass transistor is monitored. Feedback circuitry insures that the output current never exceeds a preset limit.

**Figure 8. Typical Circuit Waveforms for Output Stage Protection**

Should the junction temperature of the power device exceed 180°C (typ), the power transistor is turned off. Thermal shutdown is an effective means to prevent die overheating since the power transistor is the principle heat source in the IC.

**REGULATOR CONTROL FUNCTIONS**

The NCV8141 differs from all other linear regulators in its unique combination of control features.

**Watchdog and ENABLE Function**

$V_{OUT}$ is controlled by the logic functions ENABLE and Watchdog (Table 1).

<table>
<thead>
<tr>
<th>ENABLE</th>
<th>WDI</th>
<th>$V_{OUT}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>Slow</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>Normal</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>High</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>Low</td>
<td>5</td>
</tr>
<tr>
<td>L</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

As long as ENABLE is high or ENABLE is low and the Watchdog signal is normal, $V_{OUT}$ will be at 5.0 V (typ). If ENABLE is low and the frequency of the Watchdog input goes below the threshold frequency, the output transistor turns off and the IC goes into SLEEP mode. Only the ENABLE circuitry in the IC remains powered up, drawing a quiescent current of less than 50 µA.

The Watchdog monitors the frequency of an incoming WDI signal. If the signal falls below the WDI limit, a frequency programmable pulse train is generated at the RESET lead (Figure 9) until the correct Watchdog input signal reappears at the lead (ENABLE = HIGH).

The threshold limit of the watchdog function is set by the value of $C_{DELAY}$. The limit is determined according to the following equation for the NCV8141:

$$t_{WDI} = (1.3 \times 10^5)C_{DELAY}$$

The capacitor $C_{DELAY}$ also determines the frequency of the RESET signal and the POWER–ON–RESET (POR) delay period.

**RESET Function**

The RESET function is activated when the Watchdog frequency signal is below the watchdog threshold (Figure 9), when the regulator is in its power up state (Figure 10) or when $V_{OUT}$ drops below $V_{OUT} - 4.5\%$ for more than 2.0 µs (Figure 11).

If the Watchdog signal falls outside of the preset voltage or below the frequency threshold, a frequency programmable pulse train is generated at the RESET lead (Figure 9) until the correct Watchdog input signal reappears at the lead. The duration of the RESET pulse is determined by $C_{DELAY}$ according to the following equation:

$$t_{WDI(RESET)} = (1.0 \times 10^4)C_{DELAY}$$

**RESET CIRCUIT WAVEFORMS WITH DELAYS INDICATED**

If an undervoltage condition exists, the voltage on the RESET lead goes low and the delay capacitor, $C_{DELAY}$, is discharged. RESET remains low until output is in regulation, the voltage on $C_{DELAY}$ exceeds the upper threshold and the Watchdog input signal is valid (Figures 10 and 11). The delay after the output is in regulation is:

$$t_{POR(typ)} = (4.75 \times 10^5)C_{DELAY}$$

The RESET delay circuit is also programmed with the external cap $C_{DELAY}$.

The output of the reset circuit is an open collector NPN. RESET is operational down to $V_{OUT} = 1.0$ V. Both RESET and its delay are governed by comparators with hysteresis to avoid undesirable oscillations.
**Figure 9. Timing Diagrams for Watchdog and ENABLE Functions**

**V_{OUT} When Watchdog is Held High and ENABLE = HIGH**
- \( V_{IN} \): 0 V
- ENABLE: 0 V
- WDI: 0 V
- RESET: 0 V
- V_{OUT}: 0 V

**V_{OUT} When Watchdog is Held Low and ENABLE = HIGH**
- \( V_{IN} \): 0 V
- ENABLE: 0 V
- WDI: 0 V
- RESET: 0 V
- V_{OUT}: 0 V

**V_{OUT} When Watchdog is too Slow and ENABLE = HIGH**
- \( V_{IN} \): 0 V
- ENABLE: 0 V
- WDI: 0 V
- RESET: 0 V
- V_{OUT}: 0 V

**WDI Held High After a Normal Period of Operation; ENABLE = LOW**
- \( V_{IN} \): 0 V
- ENABLE: 0 V
- WDI: 0 V
- RESET: 0 V
- V_{OUT}: 0 V

**WDI Held Low or is too Slow after a Normal Period of Operation; ENABLE = LOW**
- \( V_{IN} \): 0 V
- ENABLE: 0 V
- WDI: 0 V
- RESET: 0 V
- V_{OUT}: 0 V

---

**Figure 10. Power RESET and Power Down**

- \( V_{R(HI)} \)
- \( V_{R(LO)} \)
- \( V_{RI(LO)} \)
- \( V_{R(PEAK)} \)
- \( t_{POR} \)

**Figure 11. Undervoltage Triggered RESET**

- \( V_{OUT} \)
- \( V_{OUT} \) -4.5%
- \( t_{POR} \)
- \( V_{RESET} \) - 5.0 V
- \( t_{POR} \)
- \( \geq 6.0 \mu s \)
- \( \geq 6.0 \mu s \)
NCV8141 DESIGN EXAMPLE

The NCV8141 with its unique integration of linear regulator and control features: RESET, ENABLE and WATCHDOG, provides a single IC solution for a microprocessor power supply. The reset delay, reset duration and watchdog frequency limit are all determined by a single capacitor. For a particular microprocessor the overriding requirement is usually the reset delay (also known as power on reset). The capacitor is chosen to meet this requirement and the reset duration and watchdog frequency follow.

The reset delay is given by:

\[ t_{POR}(\text{typ}) = (4.75 \times 10^5) \times C_{\text{DELAY}} \]

Assume that the reset delay must be 200 ms minimum.

From the NCV8141 data sheet the reset delay has a ±37% tolerance due to the regulator.

Assume the capacitor tolerance is ±10%.

\[ t_{POR}(\text{min}) = (4.75 \times 10^5 \times 0.63) \times C_{\text{DELAY}} \times 0.9 \]

\[ C_{\text{DELAY}}(\text{min}) = \frac{t_{POR}(\text{min})}{2.69 \times 10^5} \]

Closest standard value is 0.82 \( \mu \)F.

Minimum and maximum delays using 0.82 \( \mu \)F are 220 ms and 586 ms.

The duration of the reset pulse is given by:

\[ T_{WDI}^{(\text{reset})}(\text{typ}) = (1.0 \times 10^4) \times C_{\text{DELAY}} \]

This has a tolerance of ±50% due to the IC, and ±10% due to the capacitor.

The duration of the reset pulse ranges from 3.69 ms to 13.5 ms.

The watchdog signal can be expressed as a frequency or time. From a programmers point of view, time is more useful since they must ensure that a watchdog signal is issued consistently several times per second.

The watchdog time is given by:

\[ t_{WDI} = (1.3 \times 10^5) \times C_{\text{DELAY}} \]

There is a tolerance of ±20% due to the NCV8141.

ENERGY CONSERVATION AND SMART FEATURES

Energy conservation is another benefit of using a regulator with integrated microprocessor control features. Using the NCV8141 as indicated in Figure 13, the microprocessor can control its own power down sequence. The momentary contact switch quickly charges C1 through R1.

When the voltage across C1 reaches 3.95 V (the enable threshold), the output switches on and VOUT rises to 5.0 V. After a delay period determined by \( C_{\text{DELAY}} \), a frequency programmable reset pulse train is generated at the reset output. The pulse train continues until the correct watchdog signal appears at the WDI lead. C1 is now left to discharge through the input impedance of the enable lead (approximately 150 k\( \Omega \)) and the enable signal disappears. The output voltage remains at 5.0 V as long as the NCV8141 continues to receive the correct watchdog signal.

The microprocessor can power itself down by terminating its watchdog signal. When the microprocessor finishes its housekeeping or power down software routine, it stops sending a watchdog signal. In response, the regulator generates a reset signal and goes into a sleep mode where VOUT drops to 0 V, shutting down the microprocessor.
Figure 13. Application Diagram for NCV8141. The NCV8141 Provides a 5.0 V Tightly Regulated Supply and Control Function to the Microprocessor. In this Application, the Microprocessor Controls its own Power Down Sequence (see text).
Figure 14. Application Diagram

STABILITY CONSIDERATIONS

The output or compensation capacitor \( C_2 \) in Figure 14 helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. An aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (\(-25^\circ C\) to \(-40^\circ C\)), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitor \( C_2 \) shown in Figure 14 should work for most applications, however it is not necessarily the optimized solution.

To determine an acceptable value for \( C_2 \) for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

**Step 1:** Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.

**Step 2:** With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

**Step 3:** Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

**Step 4:** Maintain the worst case load conditions set in Step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

**Step 5:** If the capacitor is adequate, repeat Steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat Steps 3 and 4 with the next larger standard capacitor value.

**Step 6:** Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.

**Step 7:** Increase the temperature to the highest specified operating temperature. Vary the load current as instructed in Step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of ±20% so the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than 50% of the maximum allowable ESR found in Step 3 above.

CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 15) is:

\[
P_D(\text{max}) = \left| V_{IN(\text{max})} - V_{OUT(\text{min})} \right| I_{OUT(\text{max})} + |V_{IN(\text{max})}| Q \quad (1)
\]

where:

- \( V_{IN(\text{max})} \) is the maximum input voltage,
- \( V_{OUT(\text{min})} \) is the minimum output voltage,
- \( I_{OUT(\text{max})} \) is the maximum output current for the application, and
IQ is the quiescent current the regulator consumes at IOUT(max).

Figure 15. Single Output Regulator With Key Performance Parameters Labeled

Once the value of PD(max) is known, the maximum permissible value of RJC and TA can be calculated:

\[
R_{\text{JA}} = \frac{150^\circ C - T_A}{P_D} \quad (2)
\]

The value of RJA can then be compared with those in the package section of the data sheet. Those packages with RJA's less than the calculated value in Equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

HEATSINKS

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of RJA.

\[
R_{\text{JA}} = R_{\text{JC}} + R_{\text{CS}} + R_{\text{SA}} \quad (3)
\]

where:
\( R_{\text{JC}} \) = the junction-to-case thermal resistance,
\( R_{\text{CS}} \) = the case-to-heatsink thermal resistance, and
\( R_{\text{SA}} \) = the heatsink-to-ambient thermal resistance.

\( R_{\text{JC}} \) appears in the package section of the data sheet. Like \( R_{\text{JA}} \), it too is a function of package type. \( R_{\text{CS}} \) and \( R_{\text{SA}} \) are functions of the package type, heatsink and the interface between them. These values appear in heatsink data sheets of heatsink manufacturers.
D²PAK–7 (SHORT LEAD)
CASE 936AB–01
ISSUE B

DATE 08 SEP 2009

NOTES:
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH AND GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.005 MAXIMUM PER SIDE. THESE DIMENSIONS TO BE MEASURED AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1. DIMENSIONS D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THE THERMAL PAD.

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*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "∥", may or may not be present.