Current Sense Amplifier, 80 V Common-Mode Voltage, Bidirectional

NCS7041, NCV7041

The NCS7041 and NCV7041 are high voltage, high resolution, current sense amplifiers. They feature gain options of 14, 20, 50, and 100 V/V, with a maximum ±0.3% gain error over the entire temperature range. Each part consists of a preamplifier and buffer with access to output and input via A1 and A2 pins for an intermediate filter network or modified gain. These parts offer excellent input common−mode rejection from −6 V to 80 V. The NCS7041 can perform unidirectional or bidirectional current measurements across a sense resistor in a variety of applications. Automotive qualified options are available under NCV prefix. All versions are specified over the extended operating temperature range from −40°C to 150°C.

Features

- Gain Bandwidth: 100 kHz
- Input Offset Voltage: ±300 μV Max
- Input Offset Drift over Temperature: ±3 μV/°C Max
- Gain Error: ±0.3% Max
- Quiescent Current: 1.5 mA Typ
- Supply Voltage: 3 V to 5.5 V
- Common−Mode Input Voltage Range: −6 V to 80 V
- CMRR: 85 dB Min
- PSRR: 75 dB Min
- Low−pass Filter (1−pole or 2−pole)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These are Pb−Free Devices

Typical Applications

- Telecom Equipment
- Power Supply Designs
- Diesel Injection Control
- Automotive
- Motor Control

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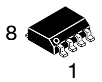
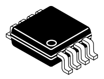
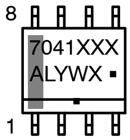


SOIC−8 NB
CASE 751−07



Micro8 / MSOP−8
CASE 846A−02

MARKING DIAGRAMS



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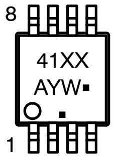
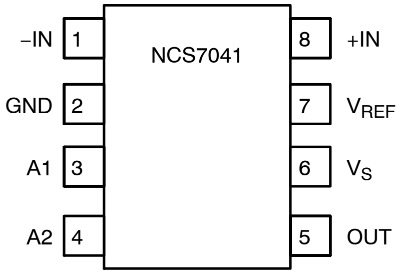


Micro8 / MSOP−8

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 15 of this data sheet.

June, 2021 − Rev. 0

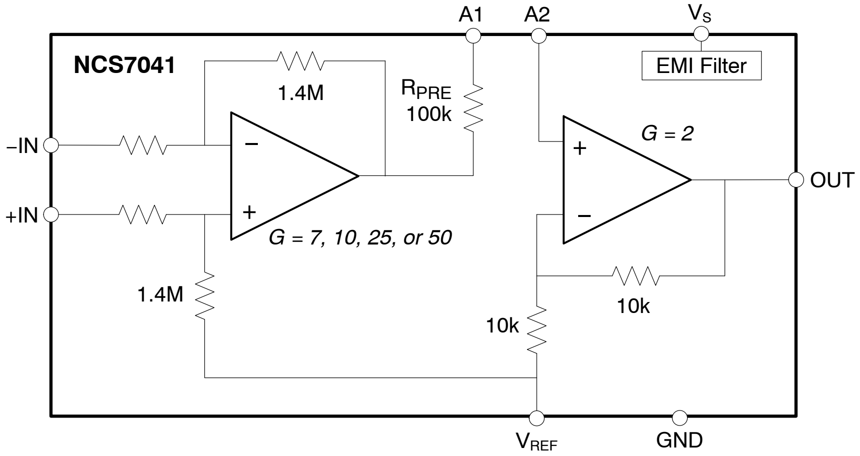
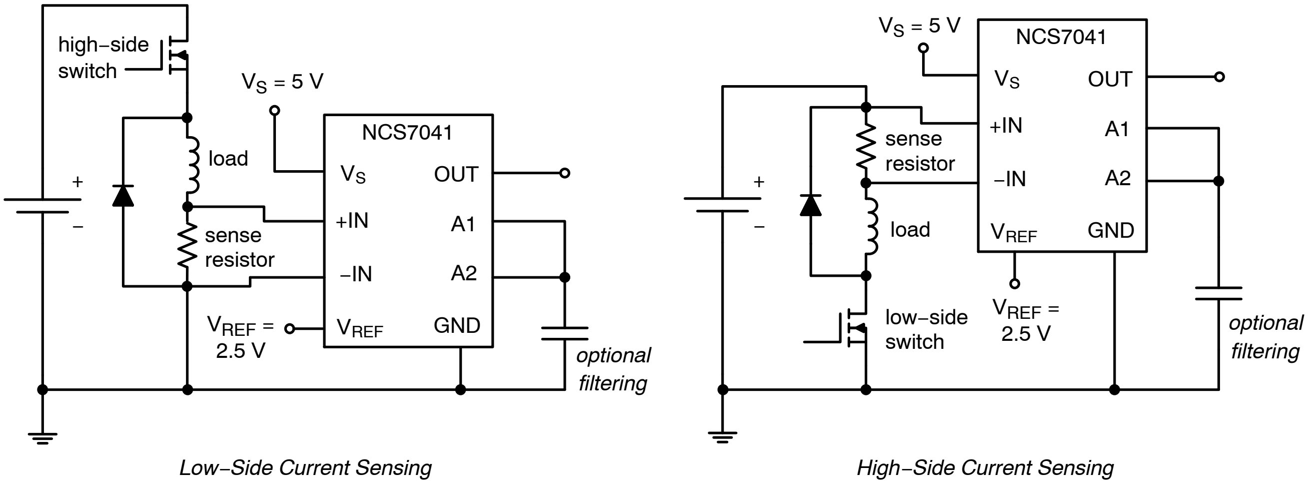


Figure 1. Simplified Representative Block Diagram



Low−Side Current Sensing

High−Side Current Sensing

Figure 2. Application Schematics

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	−IN	Inverting input. Connect to sense resistor
2	GND	Device ground
3	A1	Pre−amp output connection
4	A2	Buffer amp input connection
5	OUT	Device output
6	V_S	Power supply connection. Connect a bypass capacitor of 0.1 μF as close as possible to this pin
7	V_{REF}	Voltage reference connection to offset output
8	+IN	Non−inverting input. Connect to sense resistor

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_S	Input Voltage Range (Note 1)	−0.3 to 7	V
V_{REF}	Reference Pin Voltage	−0.3 to (V_S + 0.3)	V
V_{CM}	Input Common−Mode Voltage Range	−14 to 85	V
V_{ID}	Differential Input Voltage	±V_S	V
I_I	Maximum Input Current	±10	mA
I_O	Maximum Output Current	±50	mA
P_D	Continuous Total Power Dissipation	200	mW
$T_{J(max)}$	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	−65 to 150	°C
ESD_{HBM}	ESD Capability (Note 2) Human Body Model, Input pins Human Body Model, All other pins Charged Device Model	 ±7000 ±4000 ±1000	V
	Latch−Up Current (Note 3)	±100	mA
MSL	Moisture Sensitivity Level	1	−
T_{SLD}	Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 3)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per JS−001−2017 (AEC−Q100−002)
   ESD Charged Device Model tested per JS−002−2014 (AEC−Q100−004)
3. Latch−up current maximum rating: ±100 mA per JEDEC standard JESD78E
4. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

THERMAL CHARACTERISTICS (Note 5)

Symbol	Parameter	Package	**Value** (Note 6)	Unit
θ_{JA}	Thermal Resistance, Junction−to−Air	Micro8	163	°C/W
		SOIC−8	128	°C/W
Ψ_{JT}	Thermal Characteristic, Junction−to−Case Top	Micro8	24.4	°C/W
		SOIC−8	28.5	°C/W
Ψ_{JB}	Thermal Characteristic, Junction−to− Board	Micro8	137.3	°C/W
		SOIC−8	103.5	°C/W

5. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.
6. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

OPERATING RANGES (Note 7)

Symbol	Parameter	Min	Max	Unit
V_S	Supply Voltage	3	5.5	V
V_{REF}	Reference Voltage	0	V_S	V
V_{CM}	Input Common−Mode Range	−6	80	V
T_A	Ambient Temperature	−40	150 (Note 8)	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

7. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
8. Operation up to T_A = 150°C is permitted, provided the total power dissipation is limited to prevent the junction temperature from exceeding the 150°C absolute maximum limit.

ELECTRICAL CHARACTERISTICS (At V_S = 5 V, T_A = +25°C, V_{CM} = 12 V, V_{REF} = 2.5 V, R_L ≥ 10 kΩ, unless otherwise noted. *Italicface* limits apply over the specified temperature range, guaranteed by characterization and/or design.)

Symbol	Parameter	Conditions	Temp (°C)	Min	Typ	Max	Unit
GAIN							
G	Total Gain, Preamplifier and Buffer	G = 14 V//V G = 20 V/V G = 50 V/V G = 100 V/V	25	– – – –	14 20 50 100	– – – –	V/V
G_e	Gain Error		–40 to 125	–	–	*±0.3*	%
			–40 to 150	–	–	*±0.5*	
ΔG/ΔT	Gain Drift	G = 14 G = 20 G = 50	–40 to 125	–	–	*±20*	ppm / °C
		G = 100		–	–	*±35*	
VOLTAGE OFFSET							
V_{OS}	Input Offset Voltage		25	–	±100	±300	μV
			–40 to 125	–	–	*±300*	
			–40 to 150			*±400*	
$ΔV_{OS}/ΔT$	Input Offset Voltage Drift		–40 to 125	–	–	3	μV / °C
INPUT							
V_{CM}	Common−Mode Input Voltage Range		–40 to 150	*–6*	–	*80*	V
CMRR	Common−Mode Rejection Ratio	V_{CM} = –6 to 80 V	–40 to 150	*85*	105	–	dB
		f = 10 kHz V_{CM} = 12 V, 1 V_{PP} G = 14 G = 20 G = 50 G = 100	–40 to 150	*65* *70* *70* *75*	75 80 83 90	– – – –	
PREAMPLIFIER							
G_{PRE}	Gain	G = 14 V//V G = 20 V/V G = 50 V/V G = 100 V/V	25	– – – –	7 10 25 50	– – – –	V/V
G_e	Gain Error		–40 to 125	–	–	*±0.3*	%
V_{OH}	Output Voltage Swing to V_S		–40 to 150	*V_S – 0.05*	*V_S – 0.002*	–	V
V_{OL}	Output Voltage Swing to GND		–40 to 150	–	1.5	*25*	mV
R_{PRE}	Output Resistance		25	98	100	102	kΩ
			–40 to 150	*94*	–	*106*	
I_{IB}	Input Bias Current		–40 to 125	–	200	*500*	μA
OUTPUT BUFFER							
G_{OUT}	Gain		25	–	2	–	V/V
G_e	Gain Error		–40 to 125	–	–	*±0.3*	%
V_{OH}	Output Voltage Swing to V_S		–40 to 150	*V_S – 0.05*	*V_S – 0.003*	–	V
V_{OL}	Output Voltage Swing to GND		–40 to 150	–	0.5	*25*	mV
I_{IB}	Input Bias Current		–40 to 125	–	*±5*	*±20*	nA
DYNAMIC PERFORMANCE							
BW	Bandwidth		25	–	100	–	kHz
SR	Slew Rate		25	–	1	–	V / μs
NOISE							
V_n	0.1 Hz to 10 Hz		25	–	10	–	$μV_{p−p}$
e_N	Spectral Density, 1 kHz (RTI)		25	–	275	–	nV / √Hz
POWER SUPPLY							
V_S	Operating Voltage Range		–40 to 150	*3*	–	*5.5*	V
I_{DD}	Quiescent Current		25	–	1.5	2.4	mA
			–40 to 125	–	–	*2.7*	
			–40 to 150	–	–	*2.8*	
PSRR	Power Supply Rejection Ratio		–40 to 150	*75*	90	–	dB

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

At T_A = 25°C, V_S = 5 V, V_{CM} = 12 V, V_{REF} = 2.5 V, R_L = 10 kΩ, unless otherwise noted

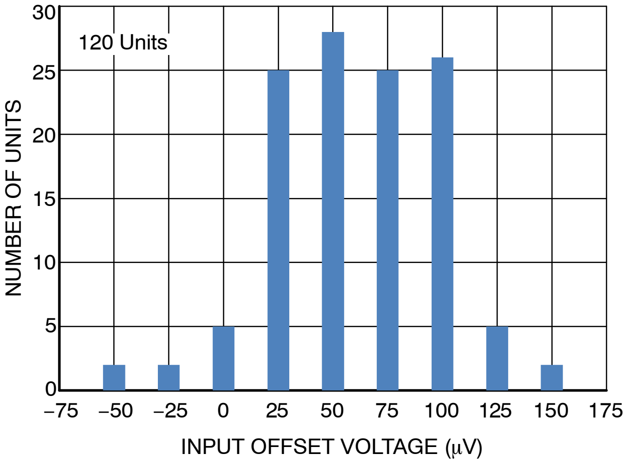


Figure 3. Input Offset Voltage Distribution

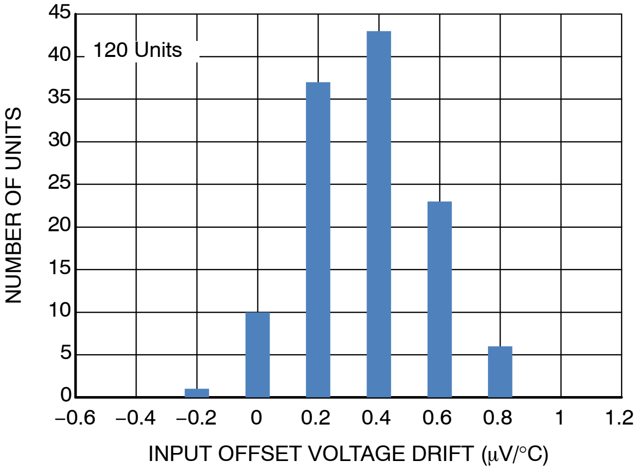


Figure 4. Input Offset Voltage Drift Distribution

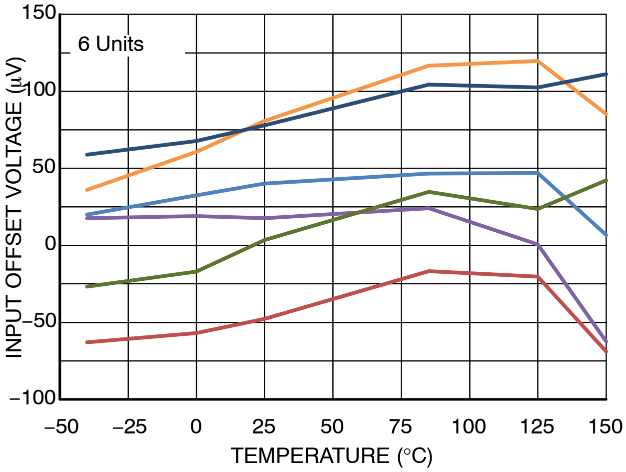


Figure 5. Input Offset Voltage vs. Temperature

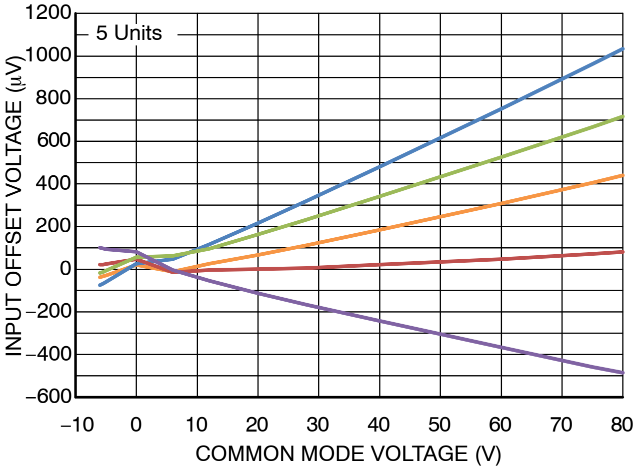


Figure 6. Input Offset Voltage vs. Common Mode Input Voltage

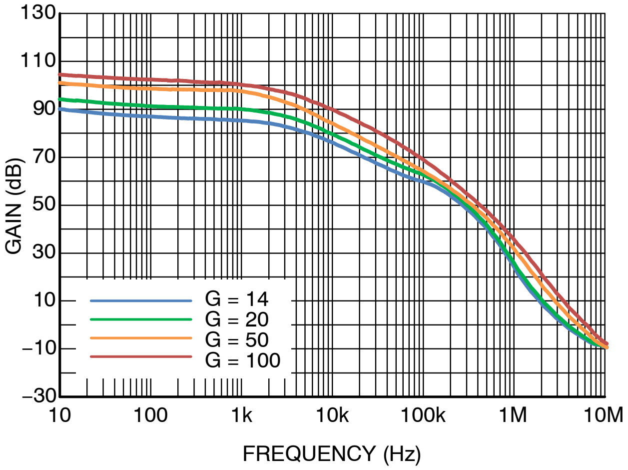


Figure 7. CMMR vs. Frequency

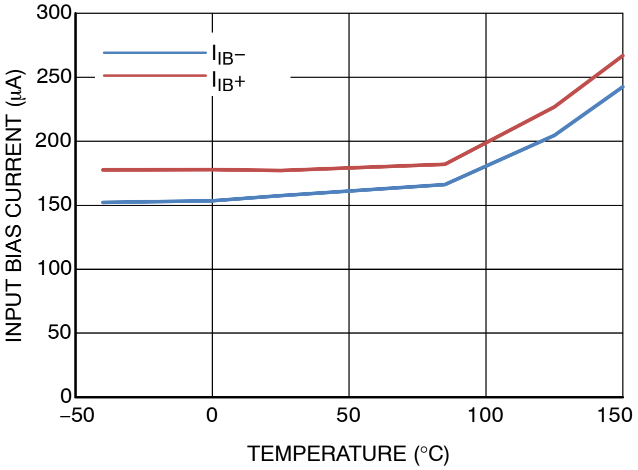


Figure 8. Preamplifer Input Bias Current vs. Temperature

TYPICAL CHARACTERISTICS

At T_A = 25°C, V_S = 5 V, V_{CM} = 12 V, V_{REF} = 2.5 V, R_L = 10 kΩ, unless otherwise noted

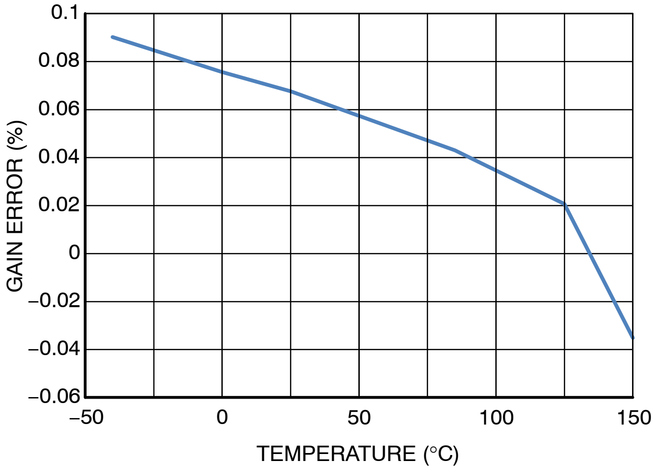


Figure 9. Preamplifier Gain Error vs. Temperature

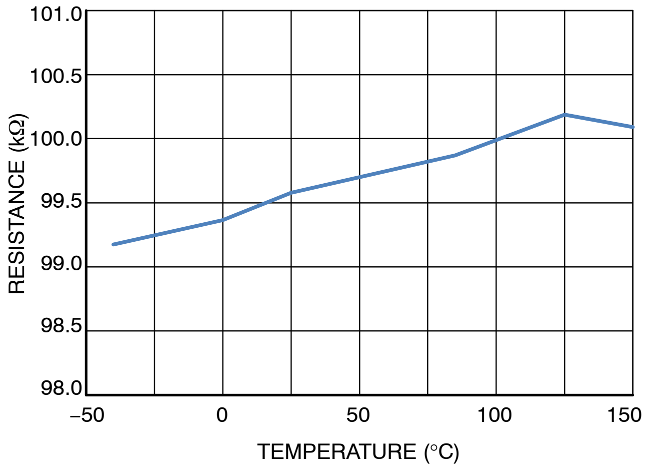


Figure 10. Preamplifier Output Resistance vs. Temperature

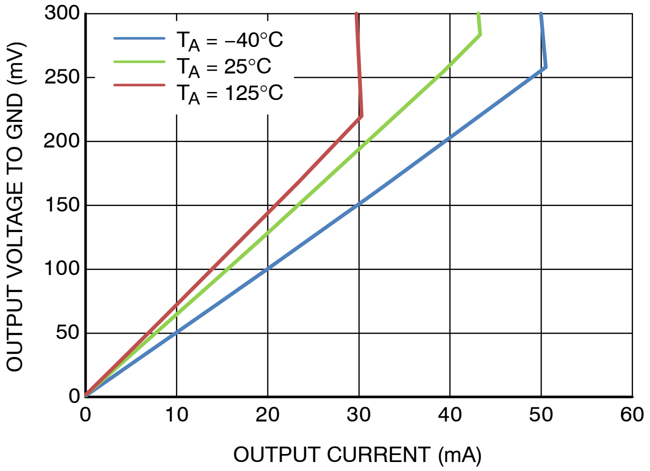


Figure 11. Buffer Output Voltage Swing to GND vs. Output Current

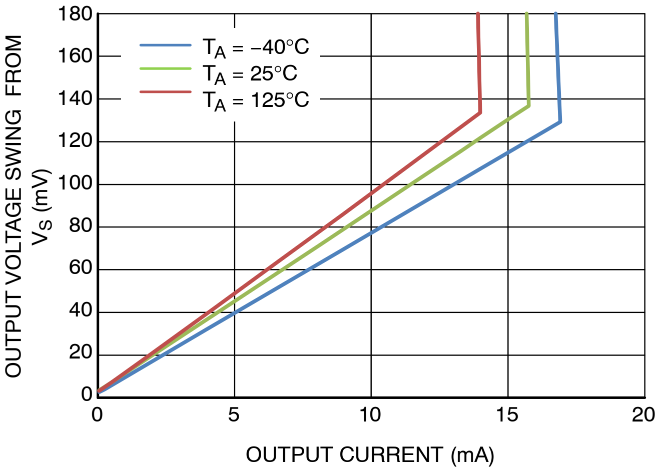


Figure 12. Buffer Output Voltage Swing from Supply Rail vs. Output Current

TYPICAL CHARACTERISTICS

At T_A = 25°C, V_S = 5 V, V_{CM} = 12 V, V_{REF} = 2.5 V, R_L = 10 kΩ, unless otherwise noted

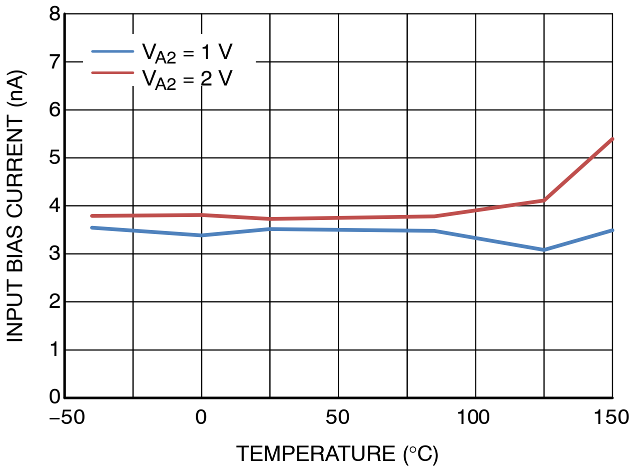


Figure 13. Buffer, Input Bias Current vs. Temperature

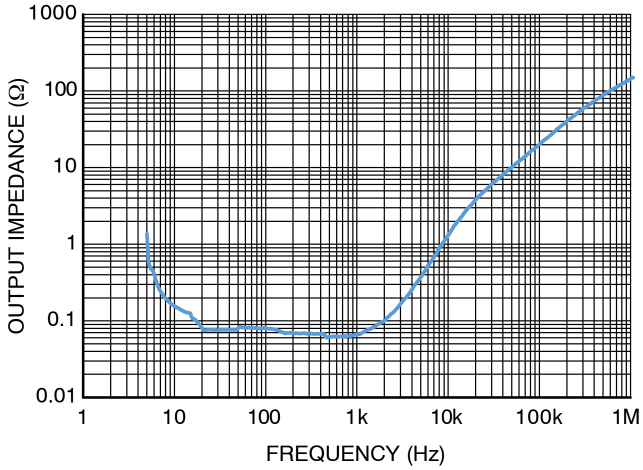


Figure 14. Buffer Output Impedance vs. Frequency

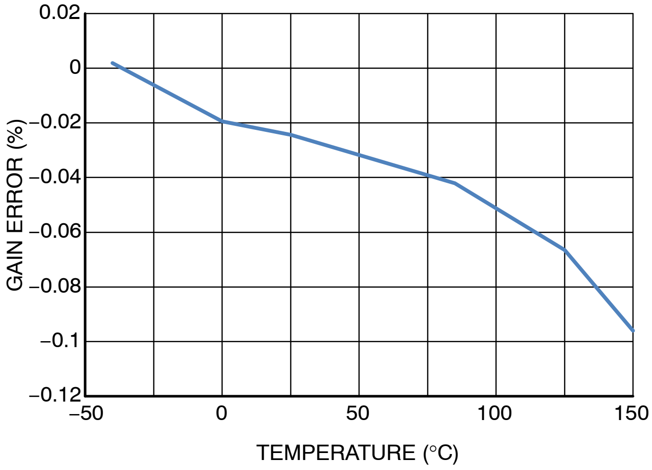


Figure 15. Total Gain Error vs. Temperature

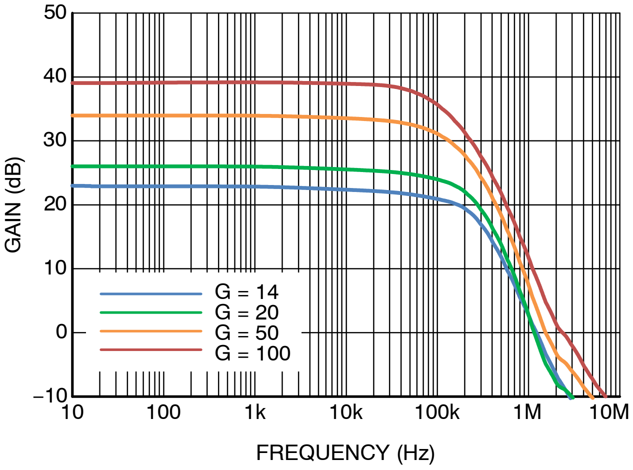


Figure 16. Gain vs. Frequency

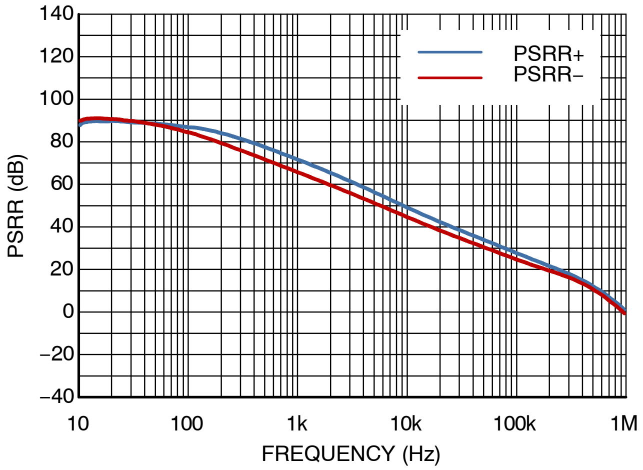


Figure 17. PSRR vs. Frequency

TYPICAL CHARACTERISTICS

At T_A = 25°C, V_S = 5 V, V_{CM} = 12 V, V_{REF} = 2.5 V, R_L = 10 kΩ, unless otherwise noted

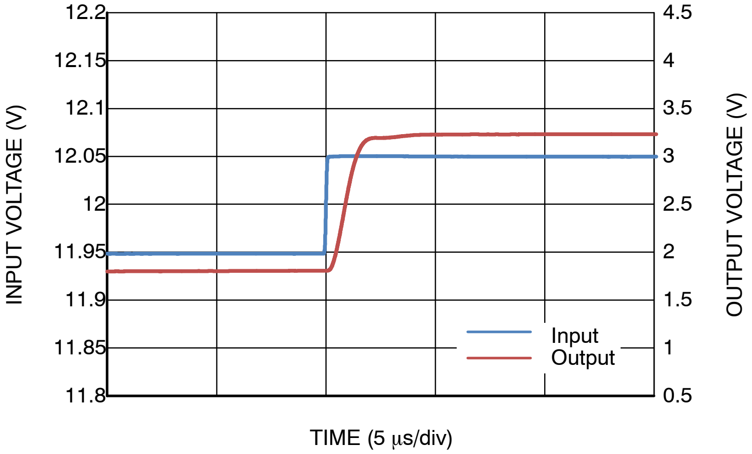


Figure 18. Transient Response

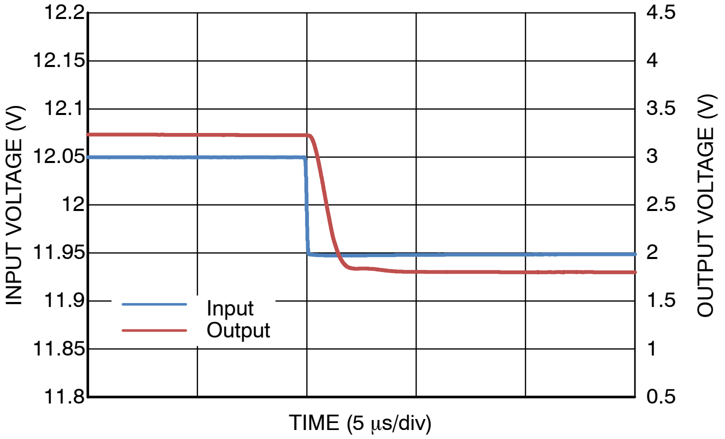


Figure 19. Transient Response

TYPICAL CHARACTERISTICS

At T_A = 25°C, V_S = 5 V, V_{CM} = 12 V, V_{REF} = 2.5 V, R_L = 10 kΩ, unless otherwise noted

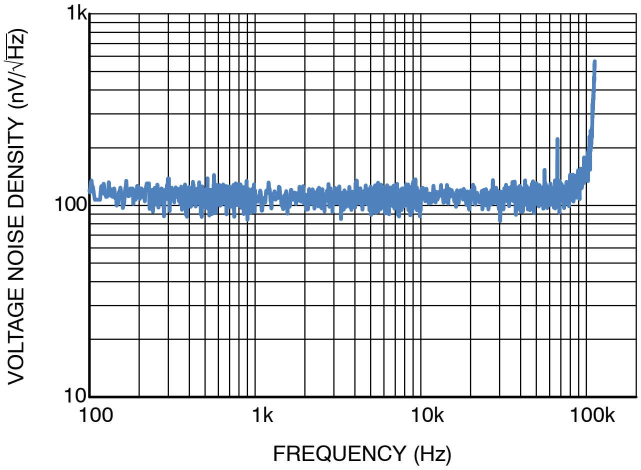


Figure 20. Voltage Noise Density

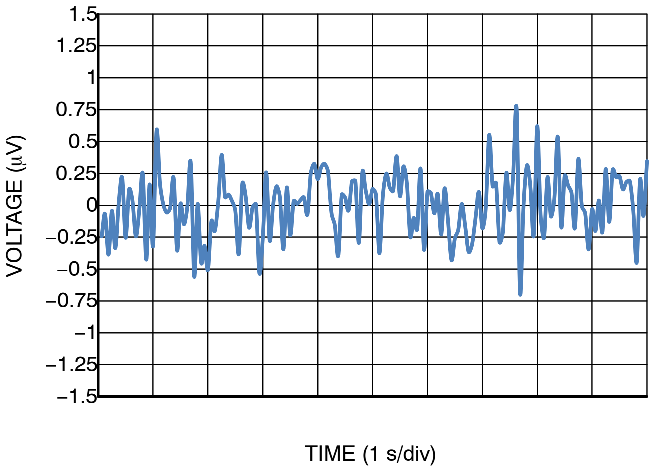


Figure 21. Noise, 0.1 Hz to 10 Hz, Referred to Input

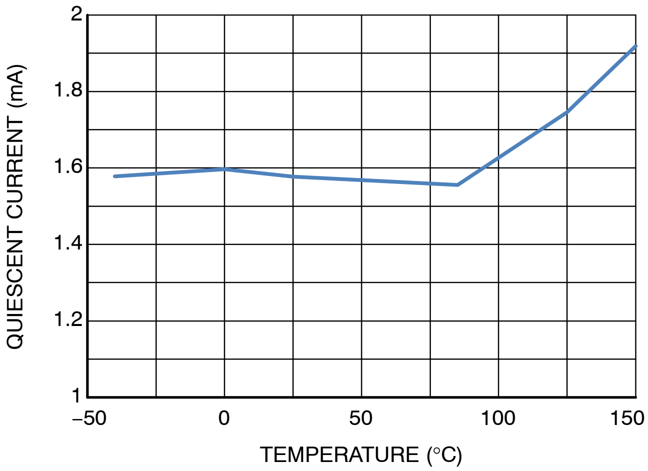


Figure 22. Quiescent Current

APPLICATION INFORMATION

The NCS7041 and NCV7041 are current sense amplifiers featuring a wide common mode voltage up to 80 V independent of the supply voltage. The NCS7041 series current−sense amplifiers can be configured for both low−side and high−side current sensing.

Current Sensing Techniques

Low−side sensing gives the impression of having the advantage of being straightforward, inexpensive, and easily implemented with a simple op amp circuit. However, a current sense amplifier such as NCS7041 provides the full differential input necessary to get accurate shunt connections, while also providing a built−in gain network with precision difficult to obtain with external resistors. The NCS7041 is shown in a low−side configuration in Figure 23 below.

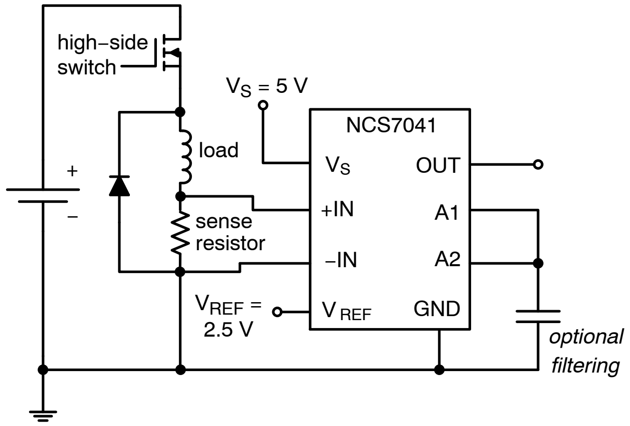


Figure 23. Low−side Current Sensing

Although certain applications require low−side sensing, only high−side sensing can detect a short from the positive supply line to ground. Furthermore, high−side sensing avoids adding resistance to the ground path of the load being measured. The sections below focus primarily on high−side current sensing. Figure 24 shows the NCS7041 configured for high−side current sensing.

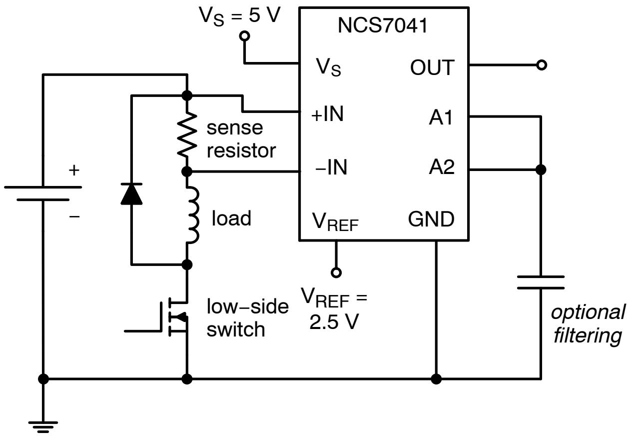


Figure 24. High−side Current Sensing

Unidirectional and Bidirectional Operation

The NCS7041 is capable of both unidirectional and bidirectional current sensing. In unidirectional current sensing, the measured load current always flows in the same direction. Common applications for unidirectional operation include power supplies and load current monitoring. In bidirectional current sensing, the measured load current can flow in either the positive or negative direction. Common applications for bidirectional operation include battery charging and discharging.

The internal circuitry of the NCS7041 is referenced to the V_{REF} pin, allowing the user to set the reference voltage by setting this voltage with a DC voltage source or other low impedance voltage source as described in the “Connecting the V_{REF} Pin” section.

For unidirectional sensing, the IN+ pin of the NCS7041 should be connected to the high side of the sense resistor, while the IN− pin should be connected to the low side of the sense resistor. When no current is flowing though the R_{SHUNT}, the NCS7041 output is expected to be close to ground. When current is flowing through R_{SHUNT}, the output will swing positive, up to within the specified voltage drop from the applied supply voltage, V_S.

For bidirectional current sensing, typically V_{REF} is set to mid−supply. The shunt resistor can be connected to the IN+ and IN− pins in direction depending on the preferred polarity of the output. When there no current being measured, the output voltage will be at the V_{REF} voltage.

$$V_{OUT} = (V_{+IN} - V_{-IN}) \times G + V_{REF} \qquad \text{(eq. 1)}$$

In bidirectional current sensing with V_{REF} set to mid−supply, the output will be at the V_{REF} voltage when no current is flowing through R_{SHUNT}. When current flows from the IN+ to IN− terminal, the output will swing towards the V_S supply. When current flows in the other direction from IN− to IN+, the output will swing towards GND.

Power Supplies

The NCS7041 can be connected to the same power supply that it is monitoring current from, or it can be connected to a separate power supply. If it is necessary to detect short circuit current on the load power supply, which may cause the load power supply to sag to near zero volts, a separate power supply must be used on the NCS7041. When using multiple supplies, there are no restrictions on power supply sequencing.

Connecting the V_{REF} Pin

In bidirectional current sensing, the current measurements are taken when current is flowing in both directions. For example, in fuel gauging, the current is measured when the battery is being charged or discharged. Bidirectional operation requires the output to swing both positive and negative around a bias voltage applied to the V_{REF} pin. The voltage applied to the V_{REF} pin depends on the application. However, most often it is biased to either half of the supply voltage or to half the value of the measurement system reference.

Figure 25 shows bidirectional operation with two different circuit choices that can be connected to the V_{REF} pin to provide a voltage reference to the NCS7041. The V_{REF} pin must always be connected to a low impedance circuit. If a resistor divider network is used to provide the reference voltage, a unity gain buffer circuit must be used, as shown in Figure 25 (a). The V_{REF} pin can be connected directly to any voltage supply or voltage reference (shunt or series).

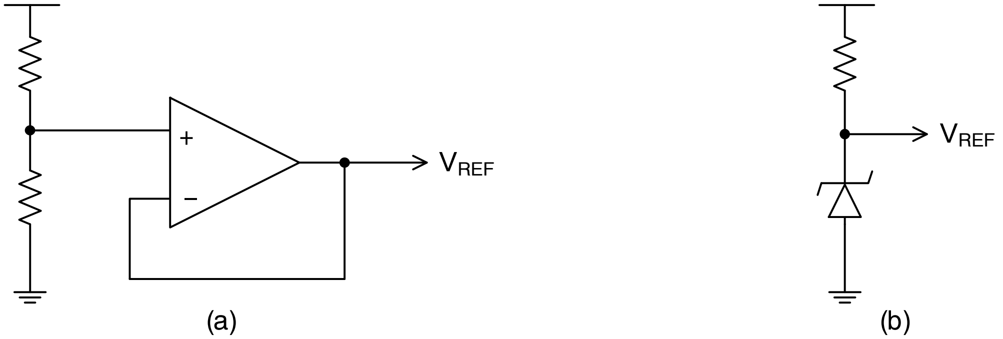


Figure 25. Voltage sources for V_{REF} must be low impedance. If using a resistor divider, the output must be buffered as shown in (a). Alternatively, a Zener diode or voltage reference may be used to set the V_{REF} voltage as shown in (b).

In bidirectional applications, any voltage that exceeds $V_S + 0.3$ V applied to the V_{REF} pin will forward bias an ESD diode between the V_{REF} pin and the V_S pin. Note that this exceeds the Absolute Maximum Ratings for the device.

A1 and A2 Pins

A1 is the preamplifier output and the A2 is the buffer input. These pins can be used to make adjustments to the gain or to create a low−pass filter. The output of the preamplifier integrates a precision resistor of 100 kΩ ±2%, which can be utilized for either of these purposes.

The high impedances at the A1 and A2 pins make this connection particularly sensitive, and a careful layout is necessary if the high frequency response is required. Trace lengths should be kept at a minimum and test points should be avoided when possible at these pins. Even a small capacitance of 20 pF from the PCB can lower the −3dB signal bandwidth to 80 kHz. This filtering effect is useful for decreasing noise, and is further discussed in the upcoming ”Filtering with A1 and A2” section.

Lowering the Gain with A1 and A2

The gain can be lowered by using the A1 and A2 pins. Connecting A1 to A2 and adding a resistor from this net to REF creates a resistor divider network in combination with the internal 100 kΩ resistor, as shown by Figure 26. For example, adding an external 100 kΩ resistor, reduces the voltage going into A2 by half, reducing the overall gain by half.

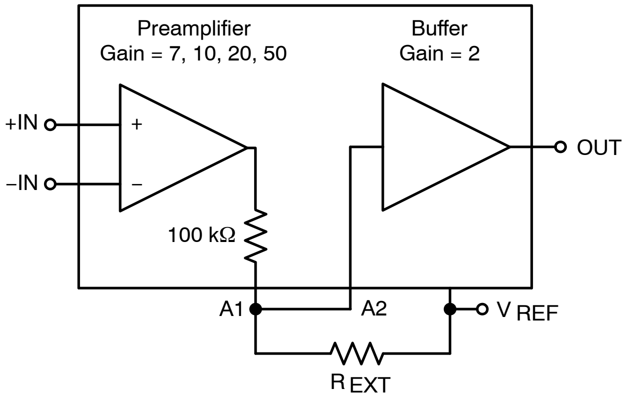


Figure 26. Lowering the Gain Using an External Resistor

The adjusted overall decreased gain, G_{ADJ-}, becomes a factor of the total gain, G, and the external resistor, R_{EXT}.

$$G_{ADJ} = \frac{G \times R_{EXT}}{R_{EXT} + 100\ k\Omega} \qquad \text{(eq. 2)}$$

This equation can be rearranged to calculate the external resistor value for the desired gain value.

$$R_{EXT} = \frac{100\ k\Omega \times G_{ADJ-}}{G - G_{ADJ-}} \qquad \text{(eq. 3)}$$

Increasing the Gain with A1 and A2

The gain can be increased by adding an external resistor in positive feedback as shown in Figure 27.

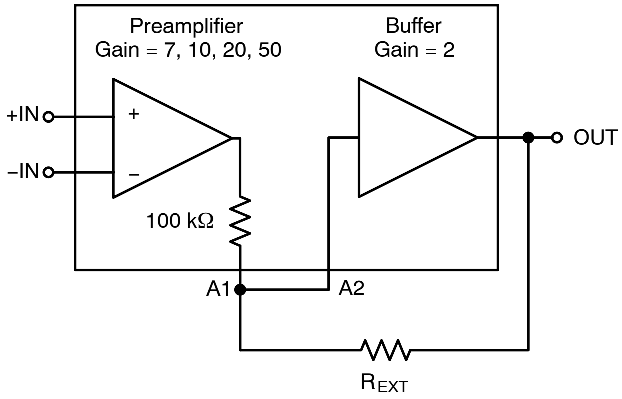


Figure 27. Increasing the Gain Using an External Resistor in Positive Feedback

$$G_{ADJ} = \frac{G \times R_{EXT}}{R_{EXT} - 100\ k\Omega} \qquad \text{(eq. 4)}$$

Filtering with A1 and A2

In some applications, the current being measured may be inherently noisy. A low−pass filter can be created by connecting A1 and A2 together and adding a capacitor from the net to GND as shown in Figure 28. This creates a simple RC filter with the internal 100 kΩ resistor. This single pole filter has a 20 dB/decade attenuation.

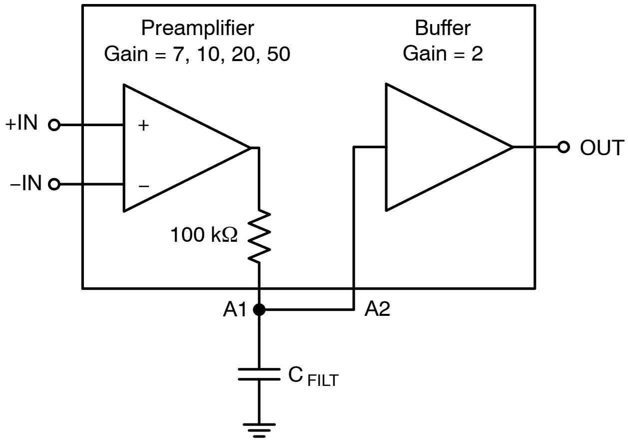


Figure 28. Implementing a Single−pole, Low−pass RC Filter

$$f_{FILT} = \frac{1}{2\pi\,(100\ k\Omega)\ C_{FILT}} \qquad \text{(eq. 5)}$$

A two−pole filter with 40 dB/decade attenuation can be created with a Sallen−Key topology as shown in Figure 29.

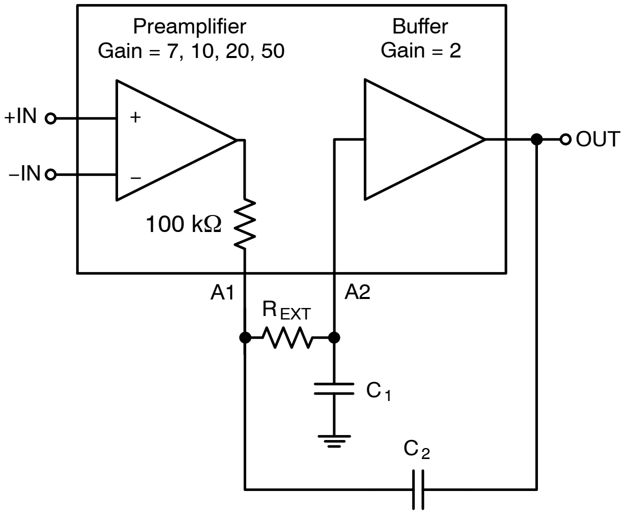


Figure 29. Implementing a Two−pole, Low−pass Filter Using the Sallen−Key Topology

Input Filtering

Some applications may require filtering at the input of the current sense amplifier. Figure 30 shows the recommended schematic for input filtering. Possible reasons for adding input filtering include the elimination of noise before it enters the current sense signal path or counteracting shunt inductance effects.

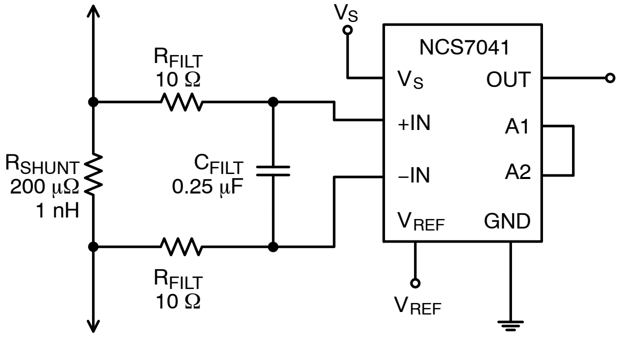


Figure 30. Input Filtering Compensates for Shunt Inductance on Shunts Less than 1 mΩ, as Well as High Frequency Noise in Any Application

Input filtering is complicated by the fact that the added resistance of the filter resistors and the associated resistance mismatch between them can adversely affect gain, CMRR, and V_{OS}. The effect on V_{OS} is partly due to input bias currents as well. As a result, the value of the input resistors should be limited to 10 Ω or less.

As the shunt resistors decrease in value, shunt inductance can significantly affect frequency response. At values below 1 mΩ, the shunt inductance causes a zero in the transfer function that often results in corner frequencies in the low 100's of kHz. This inductance increases the amplitude of high frequency spike transient events on the current sensing line that can overload the front end of any shunt current sensing IC. This problem must be solved by filtering at the input of the amplifier. Note that all current sensing IC's are vulnerable to this problem, regardless of manufacturer claims. Filtering is required at the input of the device to resolve this problem, even if the spike frequencies are above the rated bandwidth of the device.

Ideally, select the capacitor to exactly match the time constant of the shunt resistor and its inductance; alternatively, select the capacitor to provide a pole below that point. Make the input filter time constant equal to or larger than the shunt and its inductance time constant:

$$\frac{L_{SHUNT}}{R_{SHUNT}} \le 2\,R_{FILT}\,C_{FILT} \qquad \text{(eq. 6)}$$

To determine the value of C_{FILT} based on using 10 Ω resistors for each R_{FILT}, the equation simplifies to:

$$C_{FILT} \ge \frac{L_{SHUNT}}{20\,R_{SHUNT}} \qquad \text{(eq. 7)}$$

If the main purpose is to filter high frequency noise, the capacitor should be increased to a value that provides the desired filtering. The capacitor can have a low voltage rating, but should have good high frequency characteristics. As an example, a filtering frequency of 10 kHz would require a 0.8 μF capacitor.

$$f_{FILT} = \frac{1}{2\,\pi\,(2\,R_{FILT})\,C_{FILT}} \qquad \text{(eq. 8)}$$

Common Mode Voltage Step Response

Large common mode voltage steps with fast slew rates can invoke transient voltage spikes on the output. Certain applications that operate with large common mode input voltage steps, including solenoid applications, require a thorough evaluation of the output response during such events.

There are a few methods to address this. One way to decrease the transient voltage spike is by decreasing the slew rate of the common mode voltage step. The measurement can also be filtered or averaged; this can be done by adding a low−pass filter using the A1 and A2 pins as described in the previous ”Filtering with A1 and A2” section. Finally, there is the option of adding a time delay in the measurement after a common mode voltage step occurs.

The ac response to disturbances in the CMRR voltage is quantified to a certain degree in the CMRR vs. Frequency graph in Figure 7.

Advantages When Used For Low−Side Current Sensing

The NCS7041 series offers many advantages for low−side current sensing. The true differential input is ideal for connection to either Kelvin Sensing shunts or conventional shunts. Additionally, the true differential input rejects the common−mode noise often present even in low−side current sensing. Providing all of this in a tiny package makes it very competitive when compared to discrete op amp solutions.

Selecting the Shunt Resistor

The desired accuracy of the current measurement determines the precision, shunt size, and the resistor value. The larger the resistor value, the more accurate the measurement possible, but a large resistor value also results in greater current loss.

For the most accurate measurements, use four terminal current sense resistors. It provides two terminals for the current path in the application circuit, and a second pair for the voltage detection path of the sense amplifier. This technique is also known as *Kelvin Sensing*. This insures that the voltage measured by the sense amplifier is the actual voltage across the resistor and does not include the small resistance of a combined connection. When using non−Kelvin shunts, follow manufacturer recommendations on how to lay out the sensing traces closely.

Shutting Down the NCS7041

While the NCS7041 does not provide a shutdown pin, a simple MOSFET, power switch, or logic gate can be used to switch off the power to the NCS7041 and eliminate the quiescent current. Note that the shunt input pins will always have a current flow via the input and feedback resistors. The input pins support the rated common mode voltage even when the NCS7041 does not have power applied. If the V_{REF} pin is powered by a separate voltage source, the power should be disconnected from V_{REF} as well.

Layout

PCB layout is an important part of getting accurate measurements in current sensing applications. Figure 31 shows an example recommended layout for the NCS7041. External resistors are shown in dark blue, while external capacitors are shown in yellow. Bypass capacitors are shown on the V_S and V_{REF} pins.

The large component shown at the top is the sense resistor. Note how the traces are routed from the center of each resistor pad, and symmetry is maintained between the +IN and −IN paths. This is the typical connection recommended for a sense resistor, but refer to the sense resistor manufacturer's guidelines. Maintaining symmetric input traces reduces PCB−induced offsets. The optional common mode input filter is shown here, and these components are placed symmetrically also.

At the A1 and A2 pins, an optional filter capacitor and gain decreasing resistor are shown. Due to the sensitivity of the high impedance A1 and A2 pins, a keep−out area around these pins and surrounding components will reduce parasitic capacitance. For more details, refer to the previous sections for filtering and adjusting the gain at the A1 and A2 pins.

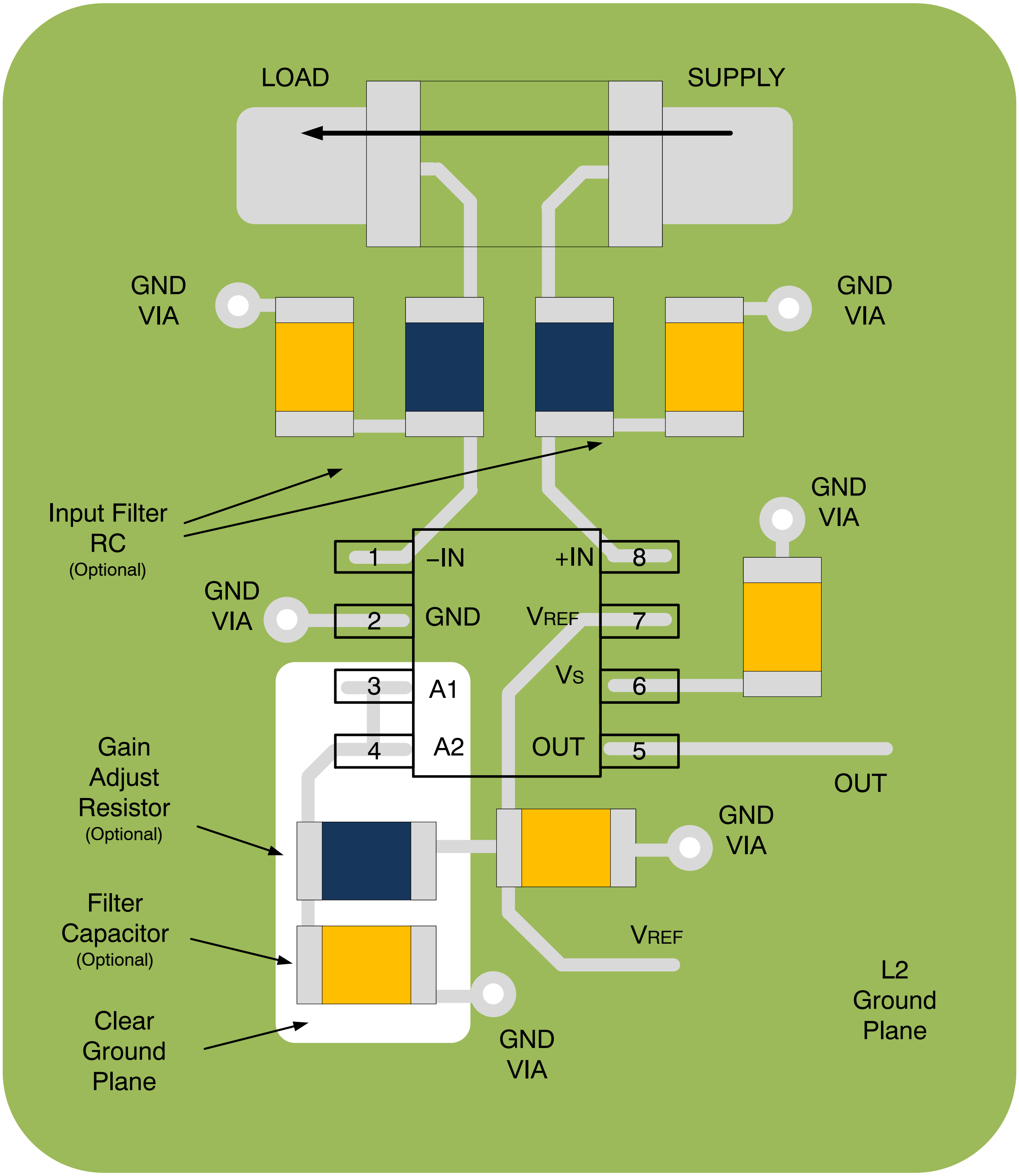


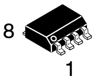
Figure 31. Example Layout for Filtering and Gain Adjustment

ORDERING INFORMATION

Device	Marking	Package	Gain	Shipping†
INDUSTRIAL AND COMMERCIAL				
NCS7041D3G014R2G*	7041014	SOIC−8 (Pb−Free)	14	2500 / Tape & Reel
NCS7041DM3G014R2G*	4114	Micro8 (Pb−Free)		4000 / Tape & Reel
NCS7041D3G020R2G*	7041020	SOIC−8 (Pb−Free)	20	2500 / Tape & Reel
NCS7041DM3G020R2G*	4120	Micro8 (Pb−Free)		4000 / Tape & Reel
NCS7041D3G050R2G	7041050	SOIC−8 (Pb−Free)	50	2500 / Tape & Reel
NCS7041DM3G050R2G*	4150	Micro8 (Pb−Free)		4000 / Tape & Reel
NCS7041D3G100R2G*	7041100	SOIC−8 (Pb−Free)	100	2500 / Tape & Reel
NCS7041DM3G100R2G*	4100	Micro8 (Pb−Free)		4000 / Tape & Reel
AUTOMOTIVE				
NCV7041D3G014R2G*	704014	SOIC−8 (Pb−Free)	14	2500 / Tape & Reel
NCV7041DM3G014R2G*	4114	Micro8 (Pb−Free)		4000 / Tape & Reel
NCV7041D3G020R2G*	7041020	SOIC−8 (Pb−Free)	20	2500 / Tape & Reel
NCV7041DM3G020R2G*	4120	Micro8 (Pb−Free)		4000 / Tape & Reel
NCV7041D3G050R2G*	7041050	SOIC−8 (Pb−Free)	50	2500 / Tape & Reel
NCV7041DM3G050R2G*	4150	Micro8 (Pb−Free)		4000 / Tape & Reel
NCV7041D3G100R2G*	7041100	SOIC−8 (Pb−Free)	100	2500 / Tape & Reel
NCV7041DM3G100R2G*	4100	Micro8 (Pb−Free)		4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

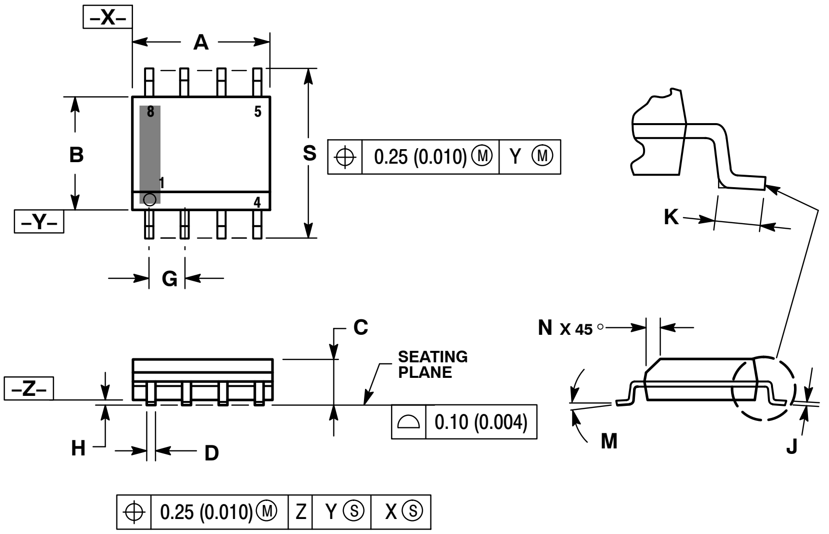
*In development. Contact local sales office for more information.



SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

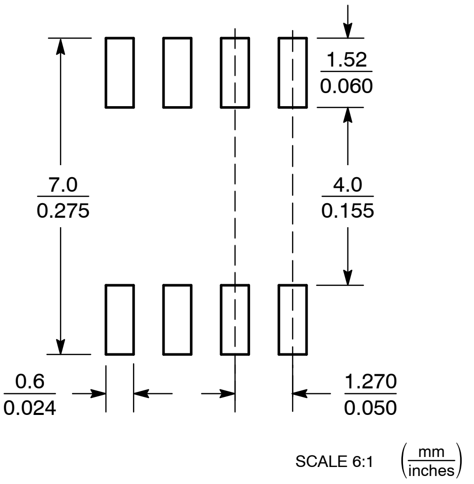
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

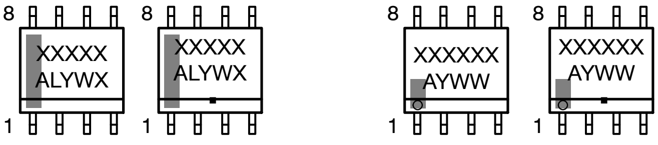
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC **IC (Pb−Free)** **Discrete** **Discrete (Pb−Free)**

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SOIC−8 NB**	**PAGE 2 OF 2**

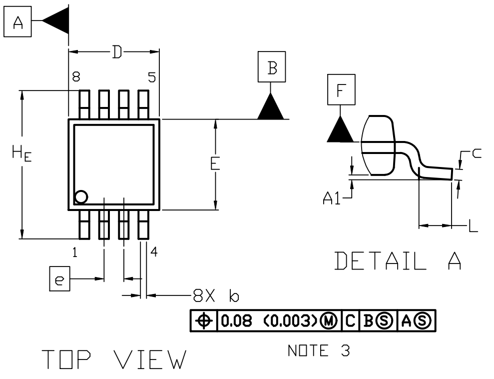
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 2:1

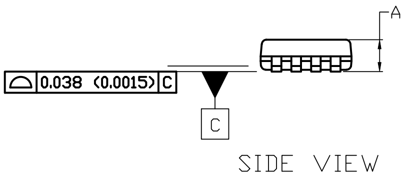
Micro8
CASE 846A−02
ISSUE K

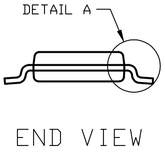
DATE 16 JUL 2020

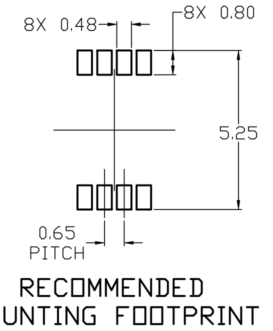


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIO OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



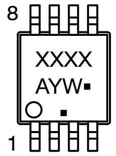




* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
b	0.25	0.33	0.40
c	0.13	0.18	0.23
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.65 BSC		
H_E	4.75	4.90	5.05
L	0.40	0.55	0.70

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:
PIN 1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

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DESCRIPTION:	**MICRO8**	**PAGE 1 OF 1**

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