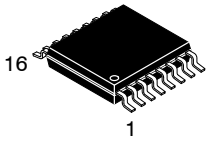
5S Battery Protector with State of Charge Indication

NCS35011



TSSOP−16
CASE 948F

The NCS35011 is an ultra−low power protection integrated circuit managing lithium−ion batteries from 3 to 5 cells in series.

Each cell in the battery pack is monitored for an over−voltage and under−voltage condition. Upon detecting an over−voltage, the ODI pin will assert indicating a fault condition and stay asserted until the fault is cleared. During an under voltage condition, the UDI pin will also assert indicating the fault but will have a pulse width that is pre−set in the protector. Both over and under voltage detections have a hard coded pre−set delay time before fault indication.

The NCS35011 can also indicate the state−of−charge on up to 5 LEDs. When the ENB pin is pulled high, the battery voltage is measured. The result is compared to a preprogrammed lookup table to determine which of the LED outputs are driven.

Hardware protection and battery monitoring run autonomously and allows operation without a microcontroller.

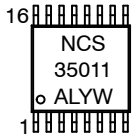
Features

- Over−Voltage (OV) and Under−Voltage (UV) Detection
- Protection for 3, 4 and 5 Series Cells
- State of Charge (SoC) Indication with High Voltage Tolerant LED Drivers
- Configurable Fault Outputs (Active High or Low for Push−Pull or Open Drain)
- High−Accuracy Cell−Voltage Measurement: ±5 mV
- Low Power Consumption I_{cc} = 4 μA
- Input BAT Voltage Range 5 V to 28 V, tolerant to 70 V for Increased Immunity to Surge
- Extended Junction Temperature Range to 125°C

Typical Applications

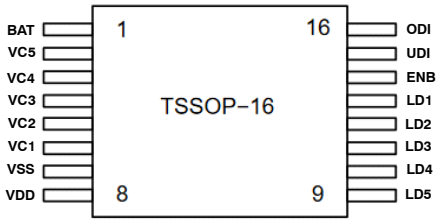
- Primary Protection for Power and Gardening Tools
- Secondary Protection for E−mobility, Medical Equipment, Mowers, and Backup Power Systems

MARKING DIAGRAM



NCS35011 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCS35011DTBR2G	TSSOP−16 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Block Diagram

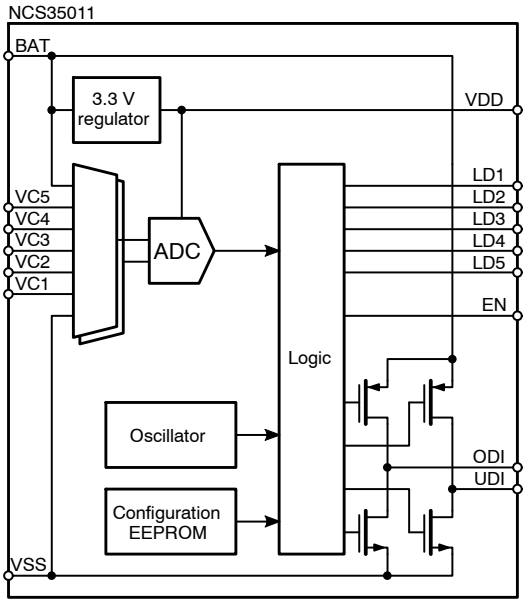


Figure 1. Simplified Block Diagram

Pin Connections

TSSOP−16

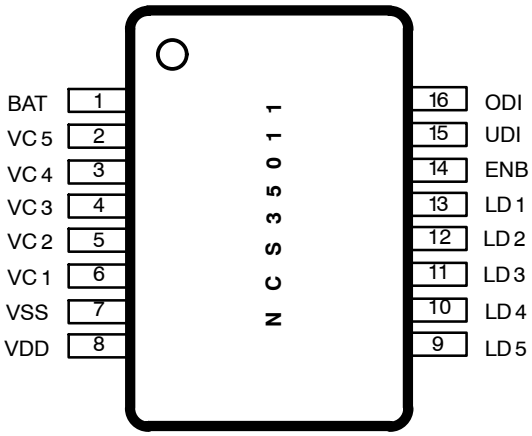


Figure 2. NCS35011 Pinout (TSSOP−16)

PIN DESCRIPTION

Signal Name	Pin No.	Type	Description
BAT	1	Power	Positive Battery input voltage
VC5	2	Analog	Battery cell 5 anode voltage
VC4	3	Analog	Battery cell 4 anode voltage
VC3	4	Analog	Battery cell 3 anode voltage
VC2	5	Analog	Battery cell 2 anode voltage
VC1	6	Analog	Battery cell 1 anode voltage
VSS	7	Ground	Negative Battery input voltage
VDD	8	Power	3.3 V regulator output voltage; for internal use only, do not use for any other purpose
LD5	9	Output Open Drain	LED output 5, open drain; active low

PIN DESCRIPTION (continued)

Signal Name	Pin No.	Type	Description
LD4	10	Output Open Drain	LED output 4, open drain; active low
LD3	11	Output Open Drain	LED output 3, open drain; active low
LD2	12	Output Open Drain	LED output 2, open drain; active low
LD1	13	Output Open Drain	LED output 1, open drain; active low
ENB	14	Input	LED output indication enable input; pull down, active high
UDI	15	Output	Cell Under voltage detection output indication; configurable (CMOS active low or high; nFET open drain active on or off)
ODI	16	Output	Cell over voltage detection output indication; configurable (CMOS active low or high; nFET open drain active on or off)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input voltage (Note 1)	V_{BAT}	−0.5 to 70	V
Supply Current	I_{BAT}	10	mA
VC1, VC2, VC3, VC4, VC5, ODI, UDI, LD1, LD2, LD3, LD4, LD5 voltage	V_{IHV}	−0.5 to min { 70, V_{BAT} + 0.5 }	V
ENB voltage	V_{ILV}	−0.5 to min { 70, V_{BAT} + 0.5 }	V
VCn − VCn−1 differential cell input voltages	V_{CELLD}	−0.5 to 30	V
Maximum Junction Temperature	$T_{J(max)}$	125	°C
Storage Temperature Range	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2	kV
ESD Capability, Charge Device Model (Note 2)	ESD_{CDM}	500	V
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 3)	T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating: ≤100 mA per JEDEC standard: JESD78
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, TSSOP−16 (Note 1) Thermal Resistance, Junction−to−Air (Note 5) Thermal Reference, Junction−to−Case (Note 5)	 $R_{\theta JA}$ $R_{\psi JC}$	115	°C/W

4. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Typ	Max	Unit
BAT Input voltage	V_{BAT}	5	18	28	V
Cell voltage (VCn − VCn−1)	V_{CELLD}	2		5	V
ODI, UDI voltage	V_{PRES}	0		V_{BAT}	V
LED voltage (LD1, LD2, LD3, LD4, LD5)	V_{LED}	0		V_{BAT}	V
ENB voltage	V_{EN}	0		V_{BAT}	V
Ambient Temperature	T_A	−40		85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL SPECIFICATIONS

Rating	Symbol	Min	Typ	Max	Unit
VOLTAGE MONITORING (VC1, VC2, VC3, VC4, VC5 and BAT)					
BAT Voltage Detection Accuracy (T_A = 25°C)	V_{BAT_QA}		±75		mV
Cell Voltage Detection Accuracy (T_A = 25°C, V_{CELLD} = 3V to 4.7V)	V_{OA}	−5		5	mV
Cell Voltage Detection Accuracy Across Temperature (T_A = −40 to 85°C)	V_{OAD}	−30		30	mV
Overvoltage Detection (OVD) Configuration Range (Note 5)	V_{OVD}	3.6		4.7	V
Overvoltage Detection Hysteresis (OVH) Configuration Range (Note 5)	V_{OVH}	50		500	mV
Undervoltage Detection (UVD) Configuration Range (Note 5)	V_{UVD}	1.5		2.8	V
Undervoltage Detection Hysteresis (UVH) Configuration Range (Note 5)	V_{UVH}	50		500	mV
BAT Threshold Voltage for SoC indication, LD1	V_{DET1}		Tables 2 and 4		V
BAT Threshold Voltage for SoC indication, LD2	V_{DET2}		Tables 2 and 4		V
BAT Threshold Voltage for SoC indication, LD3	V_{DET3}		Tables 2 and 4		V
BAT Threshold Voltage for SoC indication, LD4	V_{DET4}		Tables 2 and 4		V
BAT Threshold Voltage for SoC indication, LD5	V_{DET5}		Tables 2 and 4		V
SUPPLY AND LEAKAGE CURRENT					
Supply Current – Standby mode with no fault and ENB low	I_{CC}		4		μA
Input Current at VCx pins	I_{IN}	−0.1		0.1	μA
Supply Current – State of Charge Mode (ENB = 3.6 V, Ldx = 0, V_{CELLD} = 4 V, T_A = 25°C)	I_{SOC}		26		μA
ODI/UDI OUTPUT PIN, CMOS ACTIVE HIGH OR LOW VERSION					
ODI/UDI Active High Across Temperature ($I_{ODI-H} \leq$ 5 mA, *Tested with V_{BAT}=5V)	V_{ODI-H}		*V_{BAT}−1.7		V
ODI/UDI Active Low Across Temperature ($I_{ODI-L} \leq$ 5 mA)	V_{ODI-L}		0.1		V
OUTPUT DRIVE ODI/UDI, OPEN DRAIN NMOS FET ACTIVE ON OR OFF VERSION					
Static Drain−Source On−Resistance (nFET On−Resist), I_{ODI} = 5mA, T_A = 110°C	R_{DS-ON}			15	Ω
ODI/UDI Off Current	$I_{ODI-OFF}$			0.1	μA
ENB INPUT					
ENB Input Voltage “High”	V_{EN-H}		1.5		V
ENB Input Voltage “Low”	V_{EN-L}		1.3		V
ENB Pull Down Current	I_{PD}		50		kΩ
LED OUTPUT CURRENT DRIVE					
Output Sink Current	I_{LED-ON}			10	mA
Output Leakage Current	$I_{LED-OFF}$			0.1	μA

TIMING REQUIREMENTS

Rating	Symbol	Min	Typ	Max	Unit
DELAY TIMER					
Overvoltage Delay Time (ODEL) Configuration Range (Note 5)	t_{ODEL}	0.94	Table 3	5	s
Undervoltage Delay Time (UDEL) Configuration Range (Note 5)	t_{UDEL}	0.125	Table 3	1	s
Undervoltage Pulse Time (UPUL) Configuration Range (Note 5)	t_{UPUL}	1	Table 3	5	s
Delay/pulse Response Timing Accuracy (T_A = 25°C)	t_{error}	−6%		6%	
Delay/pulse Response Timing Accuracy Across Temperature (T_A = −40 to 85°C)	t_{error}		±6%		

TIMING REQUIREMENTS

Rating	Symbol	Min	Typ	Max	Unit
DEBOUNCE/DUTY CYCLE					
ENB Debounce for SoC Indication	t_{ENB}	30		55	ms
LDx Pulse Duration (LEDD) Time Configuration Range (Note 5)	t_{LEDD}		Table 3	5	s

5. These configurations are programmed at the factory, they are not customer programmable. However, for high volumes, **onsemi** can define further IC variants with any combination of the configurations shown in the last line of Table 3. Contact your sales representative.

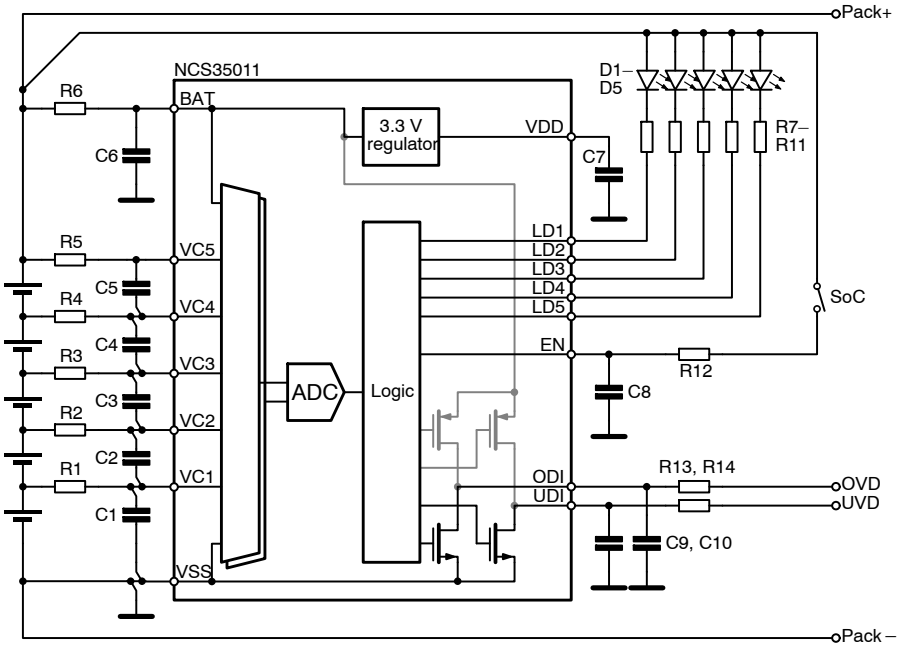


Figure 3. Application Example Diagram for 5 Cells, 5 LEDs, Open−drain Outputs (NCS35011DTBR2G)

Table 1. RECOMMENDED EXTERNAL COMPONENTS

Component Type	Instance	Value	Note
LED	D1,D2,D3,D4,D5	–	LEDs for state of charge indication
Capacitor	C6	1 μF	Battery pack voltage capacitor
Capacitor	C1−C5	100 nF	Input cell voltage filter capacitor
Capacitor	C7	1 μF	3.3V regulator output filter capacitor
Resistor	R7−R11	4.7 kΩ	LED current limiting resistor, set according to desired brightness; To guarantee the chip spec, it is recommended to limit each LED current to less than 10 mA.
Resistor	R12	100 kΩ	Limiting resistor for switch input refer to ENB pull−down current spec to set the resistance
Resistor	R1−R5	2 kΩ	Input cell voltage filter resistor
Resistor	R6	1 kΩ	Battery input filter resistor; Limit R12 resistance when IC ODI/UDI pin is configured as CMOS push/pull
Capacitor	C8−C10	100 nF	ESD protection
Resistor	R13, R14	10 kΩ	ESD protection

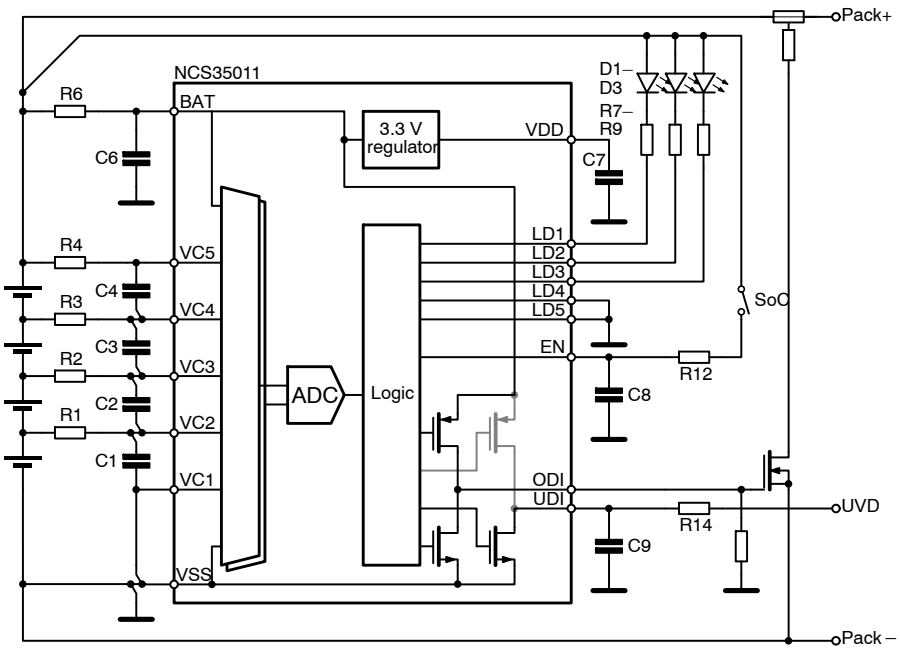


Figure 4. Application Example Diagram for 4 Cells, 3 LEDs, Mixed Push−Pull and Open−Drain Outputs (configuration variant not yet released), shown with Self−Control Protector (SCP)

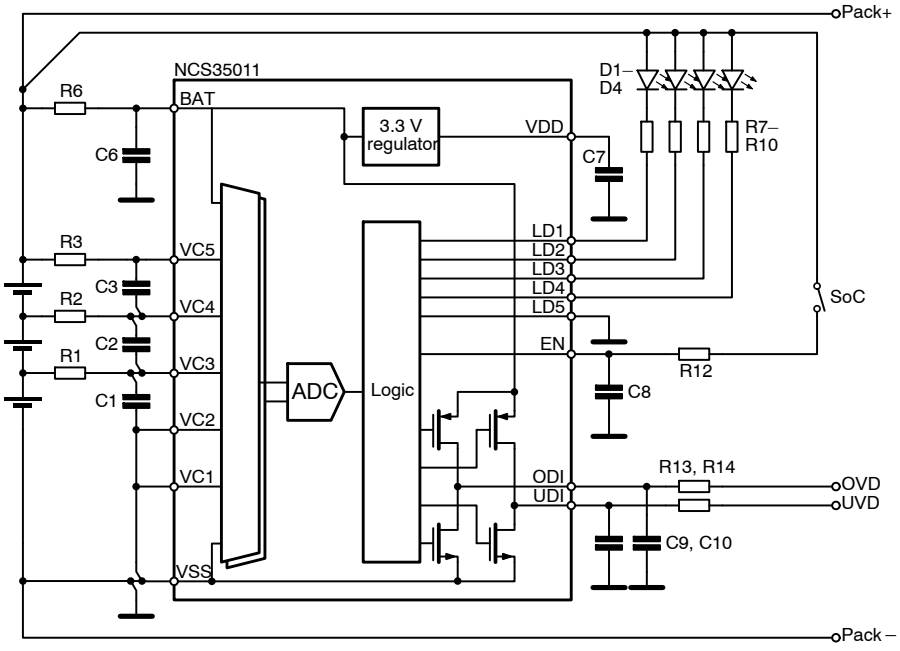


Figure 5. Application Example Diagram for 3 Cells, 4 LEDs, Push−Pull Outputs (configuration variant not yet released)

Overview

The NCS35011 is a low−power integrated−circuit (IC) for battery monitoring. It observes the voltage of the individual cells of the battery to detect over−and under−voltage conditions. The IC can also estimate the state−of−charge from the total pack voltage and drive LEDs to communicate this estimate to a user.

The NCS35011 is programmed at the factory to configure its behaviour. This configuration cannot be modified by the user. Each configuration is associated with an orderable part number (OPN).

A configuration consists of 10 settings, shown in Table 3. The bottom row of this table shows the possible values for each parameter. For instance, the cell−count (second column) can be set to either 3, 4, or 5.

The rows above show the released part numbers. For instance, the part number NCS35011DTBR2G is programmed at the factory for 5−cell batteries. For high volumes, onsemi can define further IC variants with any combination of the possible configuration values. Contact your sales representative for more information.

Cell Connections

Battery packs with 3, 4, or 5 series−connected cells are supported. Figures 3−5 show application diagrams for battery packs with 5, 4, and 3 cells, respectively. VC1 must be grounded when 4 cells are used; both VC1 and VC2 must be grounded for 3−cell packs.

The lowest cell is monitored relative to the VSS pin; for the other cells, the difference between two VC*n* pins is used. For instance, for 5 cells, $V_{CELLD1} = V_{C1} - V_{SS}$ and $V_{CELLDn} = V_{Cn} - V_{Cn-1}$.

An RC filter is required to protect the IC against electrostatic discharges (ESD) and other transients. Figures 3−5 show the recommended topologies.

Over− and Under−voltage Detection

The NCS35011 monitors each cell voltage for over−and under−voltage conditions with an on−chip analogue−to−digital converter (ADC).

In normal operation, the ADC samples each cell every 125 ms.

The results are compared to the over−voltage detection threshold (V_{OVD}). If any cell exceeds the over−voltage detection threshold for more than the over−voltage detection−delay time (t_{ODEL}), an over−voltage condition is assumed. From that point onwards, the over−voltage condition remains active as long as any cell remains above the recovery threshold. This recovery threshold is given by $V_{OVD} - V_{OVH}$, where V_{OVH} is the hysteresis. The detection threshold, detection−delay time, and hysteresis are all programmed at the factory (Table 3).

As the normal sampling period is 125 ms, the time required to detect an over−voltage lies between t_{ODEL} and t_{ODEL} + 125 ms.

Under−voltages are detected in the same way. If any cell voltage falls below the under−voltage threshold V_{UVD} for more than the detection−delay time t_{UDEL}, an under−voltage condition is assumed. Once an under−voltage condition is active, the ADC sampling period is reduced to 15.625 ms to be able to recover faster. Recovery requires two subsequent measurements where all cell voltages exceed the recovery threshold $V_{UVD} + V_{UVH}$. The minimum recovery time is therefore 31.25 ms.

As with an over−voltage, the delay from an under−voltage to detection has a sampling uncertainty of 125 ms. The detection time is therefore t_{UDEL} to t_{UDEL} + 125 ms.

Over−and under−voltage conditions are independent, and both may co−exist. This will for instance happen when V_{CELLD1} = 5 V and V_{CELLD2} = 1 V.

Over− and Under−voltage Signalling

An over−voltage condition is signalled through the ODI pin. ODI is active as long as the over−voltage condition is present, i.e., this is a static indication. ODI is configured at the factory in one of four modes: it can be an active−low or active−high pin, as well as an open−drain or push−pull pin (Table 3).

For instance, the NCS35011DTBR2G has an open−drain active−high configuration: ODI is pulled to VSS when no over−voltage has been detected, and left highly−impedant otherwise.

An under−voltage condition is signalled through the UDI pin. UDI is not static; instead, it is driven active from the moment an under−voltage is detected for the pulse time t_{UPUL} configured at the factory.

As with ODI, UDI can be configured as an active−low or−high pin and, separately, as an open−drain or push−pull pin.

For instance, in the NCS35011DTBR2G, UDI is configured as an open−drain active−low pin with a pulse time of t_{UPUL} = 1.5 s. In this variant, UDI is normally highly−impedant. When an under−voltage condition is detected, the pin pulses low for 1.5 s, then reverts to the highly−impedant state. It will only pulse low again when the under−voltage condition disappears and then re−appears.

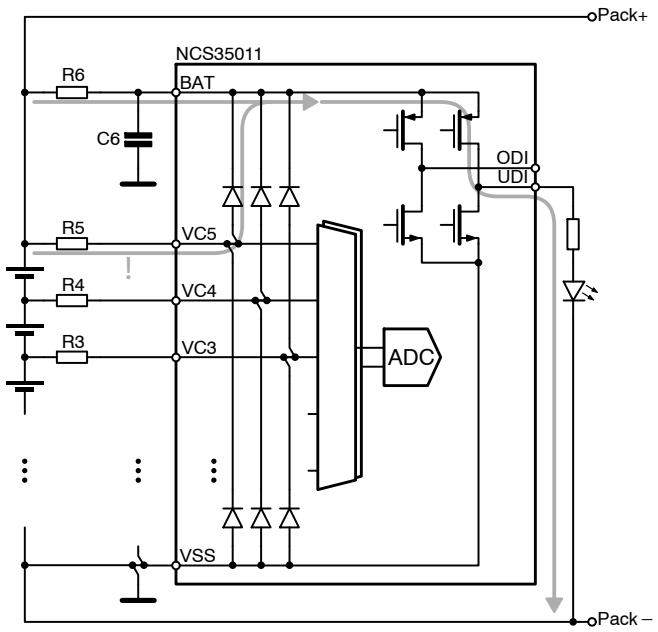


Figure 6. ODI and UDI May be Configured as Push−Pull Pins, but Care Must be Taken to Avoid Excessive Current Draw

As noted, ODI and UDI can be configured as push−pull pins. In this pin configuration, the pin is either driven to BAT or VSS. When driven to BAT, care must be taken to limit the current drawn from the pin. This current will mostly flow through the series−protection resistor R6 (figure A, upper current path), causing a voltage drop at the BAT pin. As a result, the measured voltage for the state−of−charge (SoC, see below) function will be slightly lower.

More seriously, when the current becomes so high that the voltage drop over R6 approaches the forward voltage of the ESD diode from VC5 to BAT, this diode will start to conduct. The current flowing into VC5 (Figure 6, lower current path) will cause a voltage drop over the associated filter resistor (here, R5). This drop will cause the perceived voltage of the highest cell to drop. In turn, this may cause a false under−voltage detection, or (worse) it may mask an over−voltage on the highest cell.

The current should therefore be limited to

$$I_{ODI} \leq \frac{V_{F,VC5-VBAT}}{R_6}$$

where is the forward voltage of the ESD diode. At high junction temperatures, may be as low as 0.4 V. With R6 = 1 kΩ, the current should therefore not exceed 400 μA.

It is also recommended to keep the sinking current (i.e., to VSS) below 5 mA to avoid excessive dissipation inside the IC.

Battery Pack State−of−Charge Indication

The NCS35011 can indicate the state−of−charge (SoC) of the battery pack through LEDs. The SoC is deduced from the total battery−pack voltage as measured on the BAT pin; the individual cell voltages (VCn pins) are not taken into account.

To save power, the pack voltage is measured only on request, that is, when the ENB pin is driven high. Most commonly, ENB is connected to a push−button switch. The ENB pin is tolerant to voltage up to V_{BAT}, so it may be connected to the positive battery terminal.

The ENB pin is debounced for 30–55 ms (t_{ENB} specification). If the ENB remains high for this entire time, the NCS35011 will measure the voltage at the BAT pin. The result is divided by the configured number of cells to obtain the average cell voltage.

This voltage is divided again by the configured over−voltage threshold (V_{OVD}). The result Q_{CELL} is a fraction of the voltage of a fully charged cell. If the battery pack is fully charged, Q_{CELL} = 1. Note that Q_{CELL} = 0 corresponds to a cell voltage of 0 V, *not* to the voltage of a discharged cell. For typical Li−ion chemistries, the latter is about 2–2.5 V, and $Q_{CELL} \approx 0.5$.

As an example, consider the factory−programmed configuration NCS35011DTBR2G. This IC is configured for 5 cells and for V_{OVD} = 4.275 V. Q_{CELL} is therefore derived as

$$Q_{CELL} = \frac{V_{BAT}}{5 \cdot 4.275\ V}$$

If V_{BAT} is for example measured as 13 V (close to fully discharged), Q_{CELL} = 61%.

Q_{CELL} is then compared to 5 SoC thresholds, V_{DET1} to V_{DET5}. Four threshold sets are available, called “A”–“D”, to allow for different chemistries (see Table 2). Each V_{DETx} threshold corresponds to an LD*n* pin. If Q_{CELL} exceeds a threshold, the corresponding LD*n* pin is driven low.

The active LD*n* pins are then driven low. The NCS35011 can be factory−configured to drive these pins as long as the ENB pin is high. Alternatively, a pulse time t_{LEDD} of either

3 s or 5 s may be configured. The pulse starts at the rising edge on ENB. Inactive pins remain highly−impedant. For pulsed operation, after the pulse time has elapsed, ENB may be driven high again to start a new SoC indication. The timing is shown in Figure 13.

Consider again the NCS35011DTBR2G. This IC is factory−configured to use threshold set “A”. If Q_{CELL} = 61% (as above), Table 2 shows that Q_{CELL} > VDET1 = 59%, and that Q_{CELL} is smaller than all other thresholds V_{DET2}–V_{DET5}. As a result, LD1 is driven low while LD2–LD5 remain highly−impedant.

As noted, the NCS35011 has 4 multiplier sets to choose from, shown in Table 2. The resulting cell and battery−pack threshold voltages are shown in Table 4.

The pins are usually connected to LEDs. Not all pins need to be connected: the designer can choose to skip pins. However, either LD2 or LD4 should always be used.

If the SoC function is not required at all, ENB should be connected to VSS (preferred) or left floating, and LD1–LD5 should be connected to VSS.

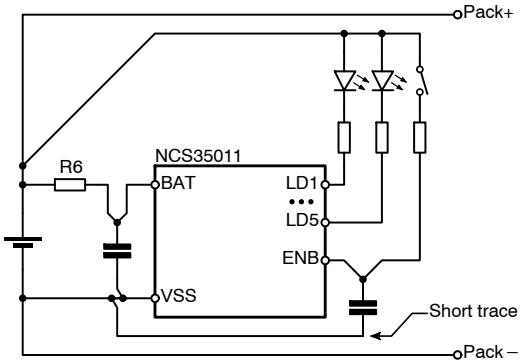


Figure 7. Series Resistors Decrease the Susceptibility of the ENB and LD1–5 Pins to ESD. The Resistor must be Connected at the Pin Side (left). Only a Single Connection should be made to Pack+ and Pack−.

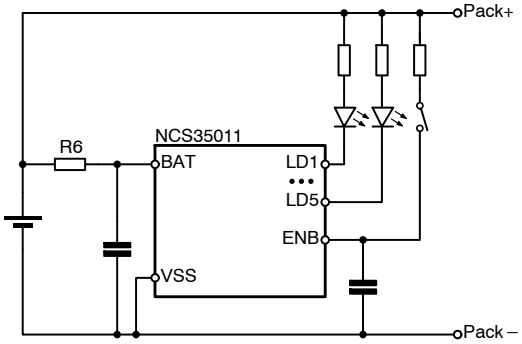


Figure 8. Poor Layout Practices: Stubs on Capacitors; Direct Path from Switches and LEDs to the IC; Multiple Connections to Pack+ and Pack−

Protection and Layout Guidelines

Battery packs are exposed to electrostatic discharge (ESD) from end users and switching transients from loads and chargers. Care needs to be taken during schematic and layout design to protect the NCS35011 from such interference.

The ENB pin is commonly connected to a mechanical switch. Depending on the design of the switch and the enclosure, this often provides a path for ESDs to the NCS35011. Adding a series resistor and a decoupling capacitor is strongly recommended (Figures 3–5).

If the ODI and UDI pins are routed to pack−connector pins, these too will be vulnerable to ESD. Again, a resistor and capacitor are recommended (Figure 3).

In some designs, the LEDs provide a path for electrostatic discharge to reach the NCS35011. If so, series resistors between the LEDs and the IC pins LD1–LD5 help; see Figure 7. This also reduces the internal dissipation.

In all cases, the resistor must be placed between the outside world and the NCS35011 (Figure 7); do not put the LED or switch between the NCS35011 and the resistor (as in Figure 8).

Any signal traces with protection capacitors should be routed first to the capacitor pad, and only then to the pin (compare Figures 7 and 8). Stub traces to the capacitor degrade the decoupling effectiveness.

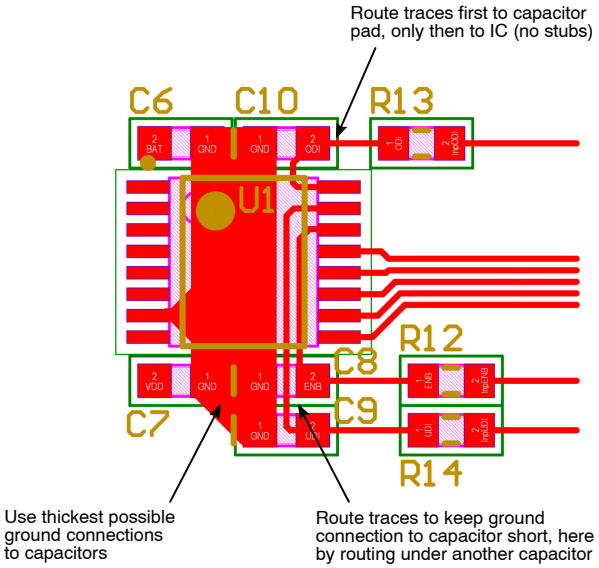


Figure 9. Possible Single−Layer Layout for ODI, UDI, and ENB Decoupling

The capacitor should have a low−impedance path to the VSS pin. This is achieved by keeping the trace between the grounded capacitor pad and the VSS pin as short and wide as possible. Place the capacitor as close as possible to the IC as possible. This is not always easy in single−layer layouts. Routing traces under capacitors helps; refer to Figure 9 for an example for protecting the ENB, ODI, and UDI pins. If necessary, a bigger capacitor package can be used.

The same principle can be used for two−layer layouts; while vias should be added to the ground plane on the second layer, the copper plane on the top layer shown in Figure 9 can

be kept to lower the impedance between the capacitors and the VSS pin.

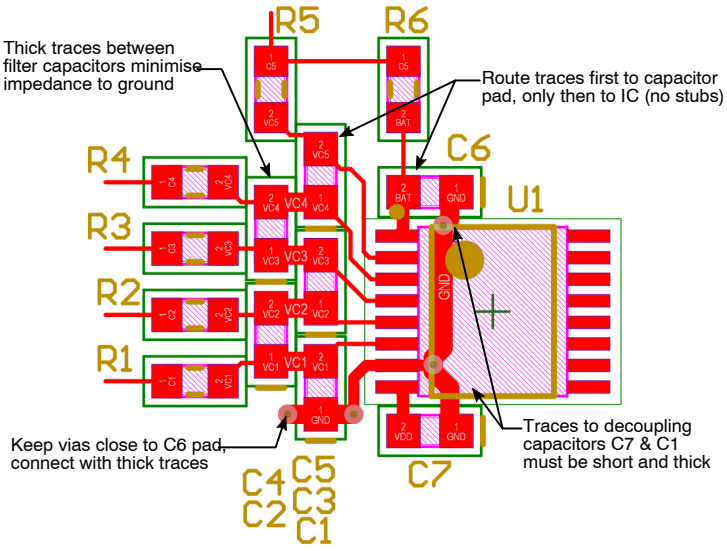


Figure 10. Suggested Layout for the Cell−Sensing Filter and the VDD Capacitor

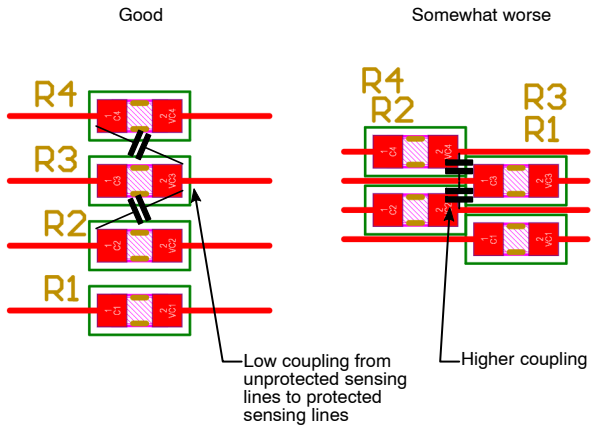


Figure 11. Care Must be Taken to Minimise the Coupling between Nets Before and Nets After the Cell−Sensing Filter Resistor. Left: Low Coupling; Right: Higher Coupling.

The layout of the cell−sensing filter should follow the same principle (see also “Cell connection”). Due to the larger component density, it is often not easy to achieve a low decoupling impedance to VSS. Place all decoupling capacitors as close as possible to the IC, and focus on keeping the loop of the decoupling on VC5 as small as possible. In Figure 3, this loop flows through C1–C5 and is closed by the IC (pins VC5 to VSS).

Figure 10 shows a possible layout (the ground plane is not shown).

The resistors, too, should be placed reasonably close to the capacitors (Figure 10). They should be placed to minimise the parasitic capacitance between the nets before and after the resistors (Figure 11).

In a two−layer design, keep crossing traces in the ground plane as short as possible. Prefer multiple short crossing bridges to a single longer trace. Design the ground place to cover all components to be protected, but do not extend it further.

The NCS35011 and its associated components should be connected to the Pack+ and Pack− nets through a single connection only. Multiple connections may decrease the ESD robustness. Compare Figure 7 (good) with Figure 8 (worse).

Consider ESD robustness when selecting components. Physically−bigger capacitors and resistors are less susceptible to damage. In addition, during a discharge, a

spark may form over a physically−small resistor. This can be avoided by selecting a bigger package or coating the board.

The voltage rating of decoupling capacitors should also be sufficiently high to tolerate the voltage rise induced by the ESD charge. The capacitance of modern ceramic capacitors drops rapidly with increasing DC bias. Choose either a higher voltage rating or a bigger nominal capacitance to compensate.

Table 2.

SoC Multiplier Sets	LED pin (LDx)	Symbol (V_{DETX})	Multiplier
A	LD5	V_{DET5}	0.954
	LD4	V_{DET4}	0.936
	LD3	V_{DET3}	0.898
	LD2	V_{DET2}	0.837
	LD1	V_{DET1}	0.585
B	LD5	V_{DET5}	0.918
	LD4	V_{DET4}	0.875
	LD3	V_{DET3}	0.847
	LD2	V_{DET2}	0.819
	LD1	V_{DET1}	0.781
C	LD5	V_{DET5}	0.877
	LD4	V_{DET4}	0.847
	LD3	V_{DET3}	0.788
	LD2	V_{DET2}	0.765
	LD1	V_{DET1}	0.729
D	LD5	V_{DET5}	0.931
	LD4	V_{DET4}	0.883
	LD3	V_{DET3}	0.841
	LD2	V_{DET2}	0.756
	LD1	V_{DET1}	0.659

NOTE: Depends on the application, user may combine or skip certain LED pins to create a desired SoC combination. Unused LED pin can be floated.

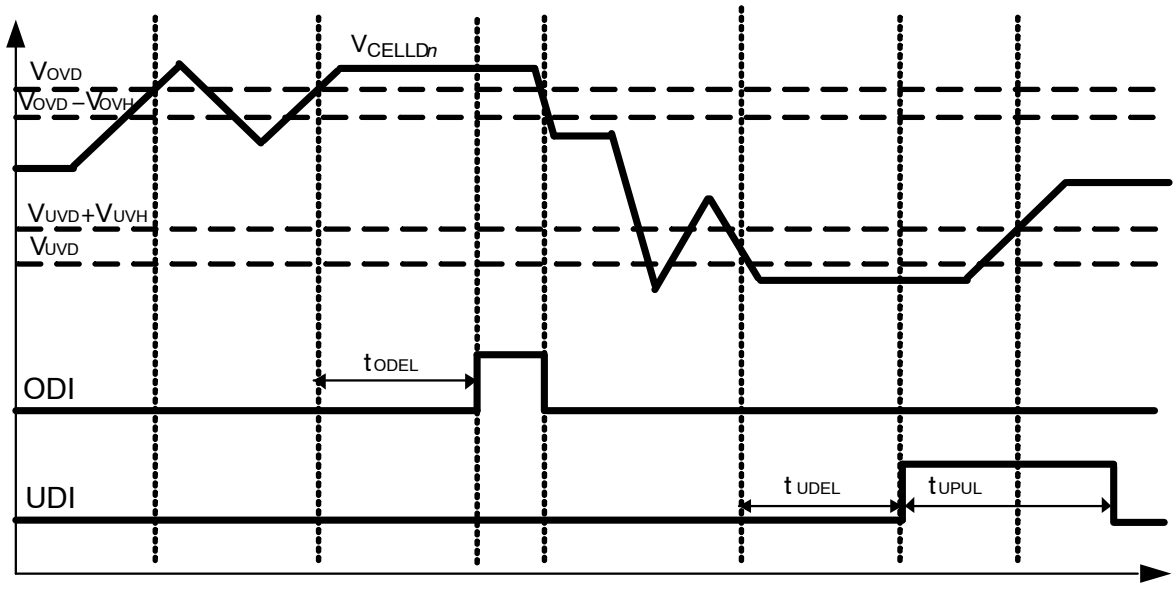


Figure 12. Timing for OV and UV Detection (ODI Configured Active−High, UDI Active−Low, as NCS35011DTBR2G)

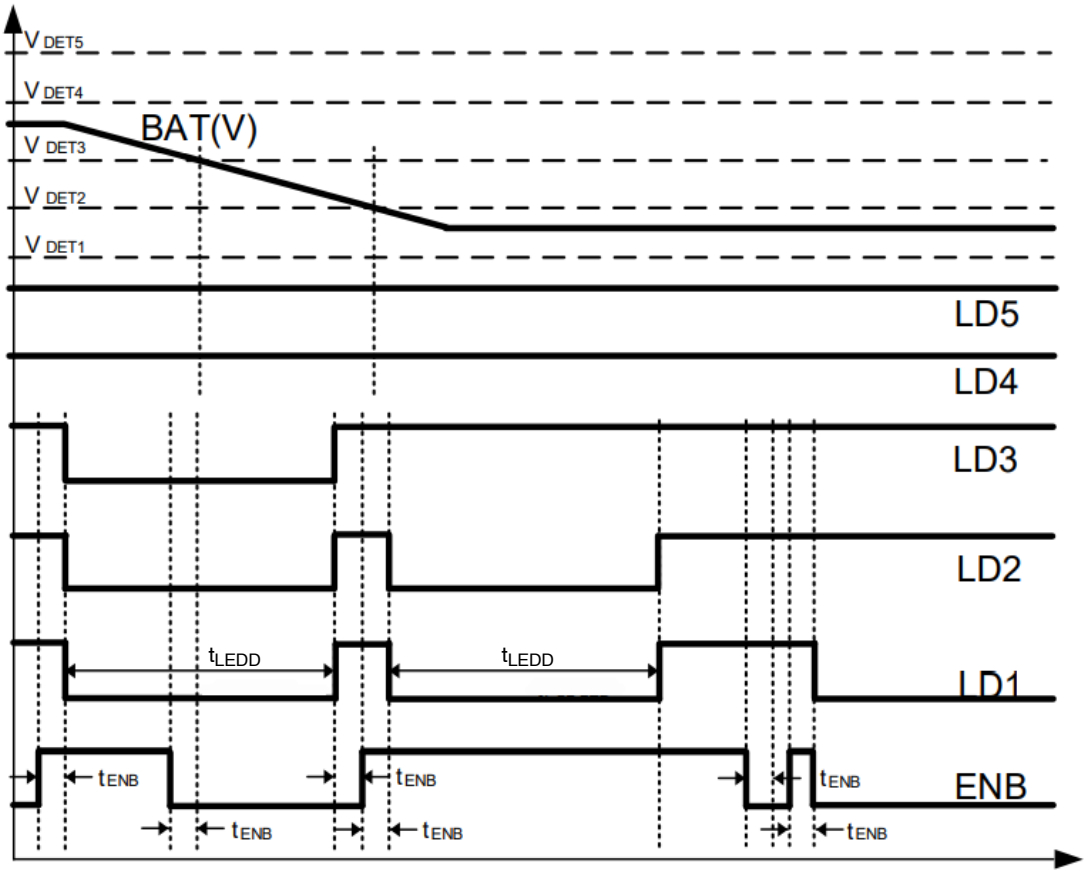


Figure 13. ENB Input Timing for State of Charge Indication

Table 3. ORDERABLE PART DIFFERENTIATION

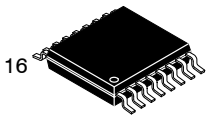
Part Number	3/4/5 cells	V_{OVD} (V)	V_{OVH} (V)	V_{UVD} (V)	V_{UVH} (V)	t_{ODEL} (s)	t_{UDEL} (s)	t_{UPUL} (s)	ODI Pin Type	ODI Pin Polarity	UDI Pin Type	UDI Pin Polarity	t_{LEDD} (s)	SoC sets
NCS35011D-TBR2G	5	4.275	0.05	2	0.25	0.875	1	1.5	OD	1	OD	0	3	A
NCS35011D-TBxyR2G	3–5	3.6–4.7	0.05–0.5	1.5–2.8	0.05–0.5	0.875–4.875	0.125–1	1–5	OD/PP	0/1	OD/PP	0/1	ENB/3/5	A/B/C/D

NOTE: **OD** = nFET open drain; **PP** = CMOS push or pull;
nFET open drain (OV/UV polarity 0): active low (nFET ON);
nFET open drain (OV/UV polarity 1): active high impedance (nFET OFF);
CMOS push−pull (OV/UV polarity 0): active low;
CMOS push−pull (OV/UV polarity 1): active high;

For high volumes, **onsemi** can define further IC variants with any combination of the shown configurations NCS35011DTBxyR2G. Contact your sales representative.

Table 4. STATE−OF−CHARGE THRESHOLDS BY CONFIGURATION

OPN:	NCS35011DTBR2G	
	Threshold	
LED Pin	Cell [V]	Pack [V]
LD5	4.08	20.4
LD4	4.00	20.0
LD3	3.84	19.2
LD2	3.58	17.9
LD1	2.50	12.5



SCALE 2:1

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CASE 948F
ISSUE B

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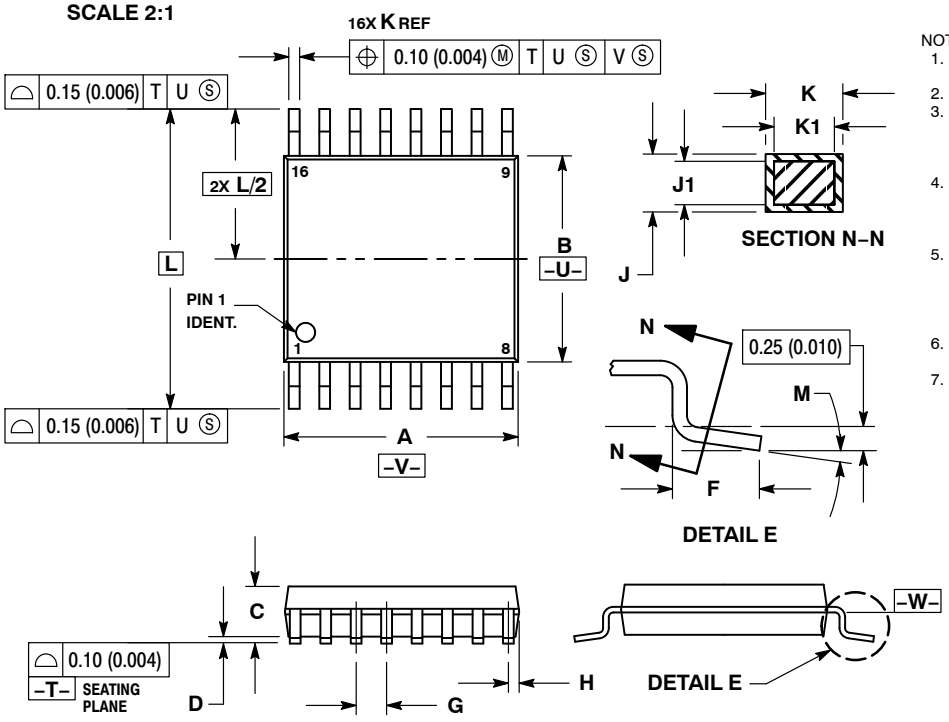
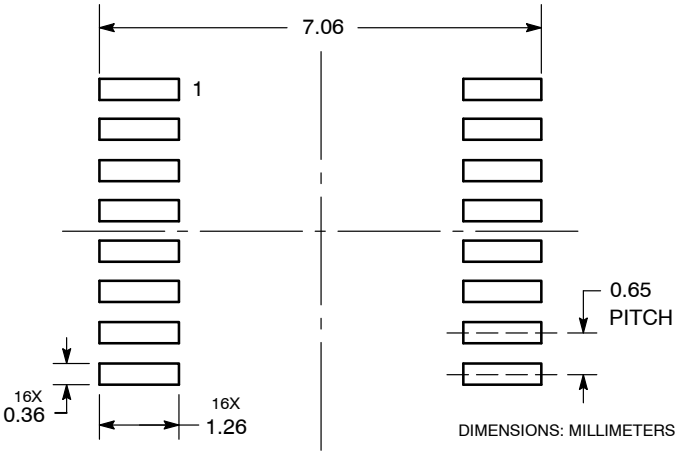


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

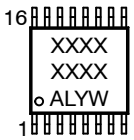
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
G or ▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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