NCS29001

LED Backlight Driver

The NCS29001 is an integrated LED driver used in LCD display backlighting applications. A configurable bill of materials allows the designer to create a highly efficient solution for a variety of LCD screen sizes. The NCS29001 uses a boost type converter to deliver constant current in a string of LEDs. High accuracy PWM dimming is supported for a frequency up to 500 Hz . The integrated soft start function provides excellent control during the power up sequence to avoid current overshoot. The device protects against output overvoltage, open / short LED, and thermal overload. The NCS29001 is offered in the cost effective SOIC−14 package.

Features

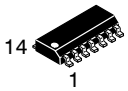
- 8.5 V to 18 V Input Voltage Range
- ±1% Vref Voltage Accuracy to set LED Current
- PWM Controlled Dimming
- Soft Start Limits In−Rush Current
- Open Feedback Protection
- Open LED Protection
- Short LED Protection
- LED String Cathode Short to ground Protection
- Max Duty Cycle Above 90%
- SOIC−14 Package
- This is a Pb−Free Device

Typical Application

- TFT−LCD TV Panels
- LCD Monitor Panels

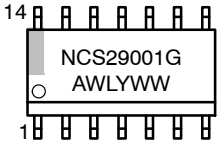
ON Semiconductor®

http://onsemi.com



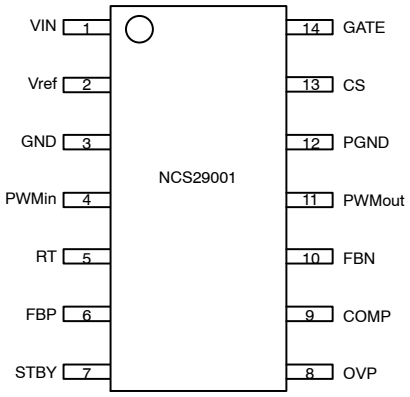
SOIC−14 NB
CASE 751A

MARKING DIAGRAM



NCS29001 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 15 of this data sheet.

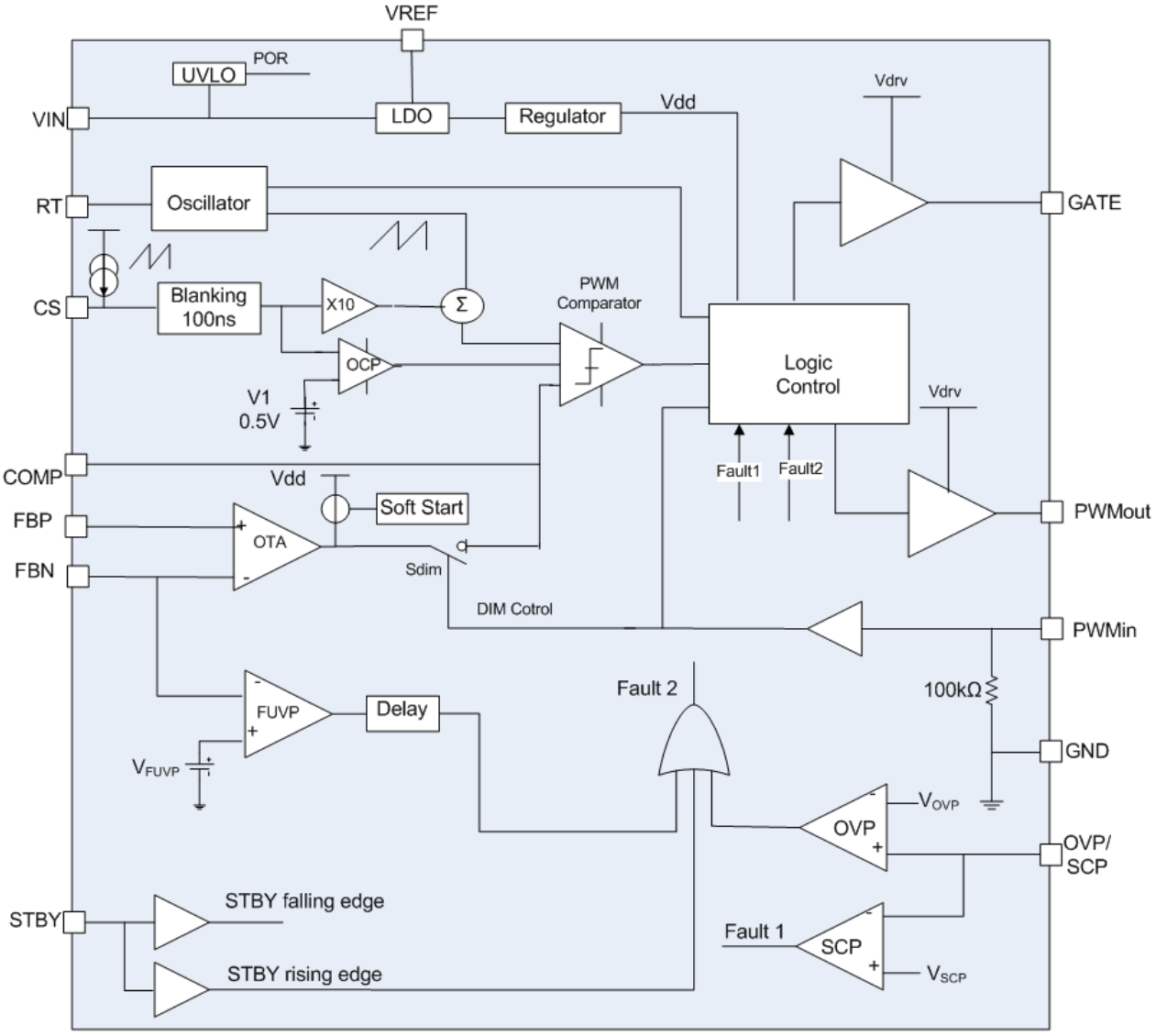


Figure 1. Block Diagram

PINOUT ASSIGNMENT

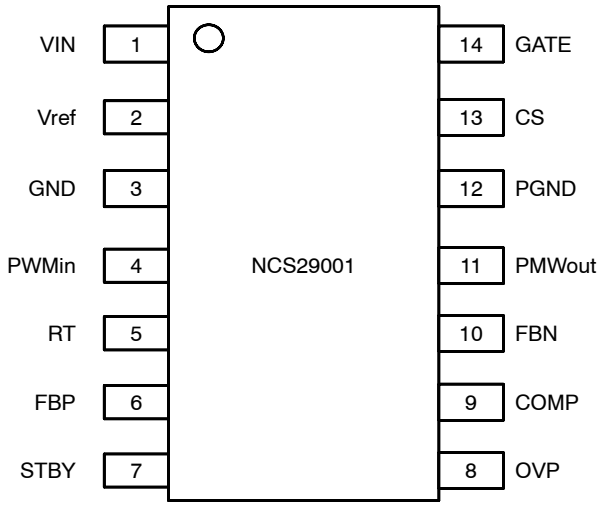


Figure 2. NSC29001 Pinout

PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	VIN	Input	VIN supply input. Small 1.0 μF low ESR bypass capacitor required from VIN to GND.
2	VREF	Output	5 V / 10 mA reference voltage. Small 1.0 μF low ESR bypass capacitor required from VREF to GND.
3	GND	Ground	Analog ground.
4	PWMin	Output	PWM dimming control input.
5	RT	Output	The resistor connected between RT and GND sets the switching frequency
6	FBP	Input	The reference voltage for the feedback (FBN). Reference level can be adjusted from 0.5 V up to 3.0 V using an external voltage divider.
7	STBY	Input	The converter enters in standby mode when STBY is floating or pulled high. When STBY goes from low to high the circuit will discharge the capacitors on the COMP pin and keep PWMout high to discharge the output capacitor. STBY must remain high for 50 ms before the part enters standby mode.
8	OVP	Output	This pin provides the overvoltage protection for the converter. When the voltage at this pin exceeds 1.2 V, the boost converter stops immediately and the device enters standby mode.
9	COMP	Power	Loop compensation pin
10	FBN	Input	Feedback pin and LED cathode connection. External resistor from FBN to GND sets the LED current.
11	PWMout	Output	PWM dimming output driver.
12	PGND	Ground	Power ground.
13	CS	Power	This pin is used to sense the drain current of the external power MOSFET. It includes a built−in blanking time.
14	GATE	Output	This pin is the output GATE driver for an external N−channel power MOSFET

ATTRIBUTES

Characteristics	Values
ESD protection (all pins) Human Body Model (HBM) (Note 1) Machine Model (MM)	 2 kV 150 V
Moisture sensitivity (Note 2)	Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latch−up Test	

1. Human Body Model (HBM), R = 1500 Ω, C = 100 pF.
2. For additional information, see Application Note AND8003/D.

ABSOLUTE MAXIMUM RATINGS

Rating	V_{MIN}	V_{MAX}	Unit
V_{IN}	−0.3	30	V
PWMin	−0.3	5.5	V
STBY	−0.3	5.5	V
FBP	−0.3	5.5	V
FBN	−0.3	5.5	V
OVP	−0.3	5.5	V
CS	−0.3	5.5	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

OPERATING CONDITIONS (T_A = +25°C)

Rating	Min	Typ	Max	Unit
V_{IN}	8.5	12	18	V
VIL_PWMin: PWMin input low voltage			1	V
VIH_PWMin: PWMin input high voltage	2			V
FBP	0.5		3.0	V
VIL_STBY: STBY input low voltage			1	V
VIH_STBY: STBY input high voltage	2			V
RT clock frequency resistor (Note 3)	20		140	kΩ
Fdim dimming frequency (5 V amplitude)	100		300	Hz
Ddim dimming duty−cycle	3		95	%

NOTE: With respect to the GND pin.

3. Choose RT to keep clock frequency between 100 kHz and 500 kHz.

THERMAL RATINGS

Parameter	Symbol	Rating	Unit
Junction to ambient thermal impedance (Note 4)	$R_{\theta JA}$	150	°C/W
Maximum Junction Temperature (Note 5)	T_J	+150	°C
Operating Ambient Temperature	T_A	−40 to +85	°C
Storage temperature	T_{stg}	−65 to +150	°C

4. Power dissipation must be considered to ensure maximum junction temperature (θ**JA**) is not exceeded.
5. Thermal Pad attached to PCB, 0 lfm airflow, and 76 mm x 76 mm copper area.

ELECTRICAL SPECIFICATIONS V_{IN} = 12 V, T_{AMB} = −40°C to 85°C; typical values are at 25°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIN (VIN Pin)						
I_{VIN}	Operating Supply Current	V_{IN} = 12 V; PWMin = 5 V; no load, STBY = 5 V			5	mA
$I_{SHUTDOWN}$	Shutdown Mode Supply Current	PWMin = GND Ambient temperature 25°C STBY = 5 V			12	uA
UVLO	Under Voltage Lockout Threshold	VIN Rising	7.5	8	8.5	V
ΔUVLO	UVLO Hysteresis			475		mV
$T_{startup}$	Startup time	Time from standby falling edge to steady−state V_{boost} operation with 30% dimming pattern − (Note 6)			100	ms
VREF (VREF Pin)						
VREF	Vref voltage	REF bypassed with a 1 μF capacitor to GND	4.95	5	5.05	V
Line_Reg	Line Regulation	V_{IN} = 8.5 V to 24 V at I_REF = 10 mA		0.08	0.20	%
Load_Reg	Load Regulation	0 mA < I_REF < 10 mA at VIN = 12 V			0.6	mV/mA
I_{CC} (Vref)	Iref output current	VREF bypassed with a 1 μF capacitor to GND			10	mA
GATE (GATE, RT Pins)						
V_{OH_GATE}	GATE output high voltage	V_{IN} = 12 V	7.5	10	15	V
I_{SOURCE}	GATE short circuit current			0.33	0.45	A
I_{SINK}	GATE sinking current			0.33	0.45	A
T_{RISE}	GATE output rise time	Output voltage rise−time @ C_L = 1 nF, 10−90% of output signal (Note 6)	−	40		ns
T_{FALL}	GATE output fall time	Output voltage fall−time @ C_L = 1 nF, 90−10% of output signal (Note 6)	−	20		ns
R_{OH}	Source resistance			13		Ω
R_{OL}	Sink resistance			6.0		Ω
D_{LSS_MAX}	Maximum Duty Cycle	(Note 6)	93	95		%
F_{OSC}	Boost Switching Frequency range		100		500	kHz
$\pm\Delta F_{OSC}$	Frequency Accuracy		−10		+10	%
V_{RT}	RT pin output voltage		0.85	1	1.15	V
PWM DIMMING (PWMin, PWMout Pins)						
V_{OH_PWMout}	PWMout output high voltage	V_{IN} = 12 V	7.5	10	15	V
ΔD_DIM	PWMout/PWMin Duty cycle Tolerance		0.98	1	1.02	%
T_{RISE}	PWMout output rise time	Output voltage rise−time @ C_L = 1 nF, 10−90% of output signal	−	−	2	us
T_{FALL}	PWMout output fall time	Output voltage fall−time @ C_L = 1 nF, 90−10% of output signal	−	−	2	us
I_{SOURCE}	PWMout short circuit current			15	20	mA
I_{SINK}	PWMout sinking current			15	20	mA
R_{OH}	Source resistance			270		Ω
R_{OL}	Sink resistance			230		Ω

6. Guaranteed by characterization and design

ELECTRICAL SPECIFICATIONS V_{IN} = 12 V, T_{AMB} = −40°C to 85°C; typical values are at 25°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
CURRENT SENSE (CS Pin)						
V_{CS}	Reference voltage threshold for current clamp monitoring OCP comparator			0.5	0.6	V
I_{RAMP}	Slope compensation ramp			130		A/s
PROTECTION (OVP, FBP, FBN Pins)						
V_{OVP}	Output Overvoltage Protection on OVP pin			1.2	1.3	V
V_{SCP}	Short Circuit Protection on OVP pin		60	75		mV
V_{UVPfb}	Output Undervoltage Protection on FBN		60	75		mV
T_{SD}	Thermal Shutdown	(Note 6)	140	150	160	°C
ΔT_{SD}	TSD hytheresis	(Note 6)		15		°C
STANDBY (STBY Pin)						
$T_{STANDBY}$	Standby mode delay	(Note 6)		50		ms

6. Guaranteed by characterization and design

APPLICATION DIAGRAM

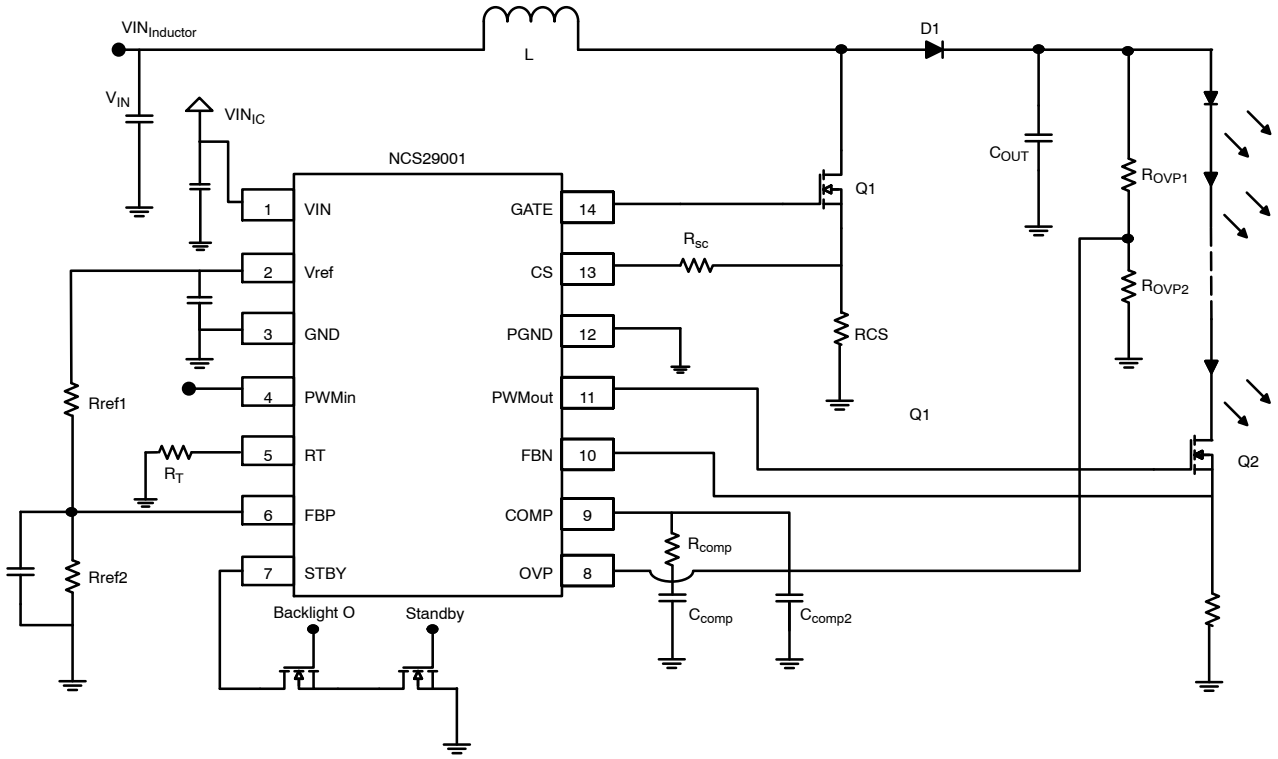


Figure 3. Application Schematic

APPLICATION CONDITIONS

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIN_{IC}	VIN pin voltage		8.5	12	18	V
$VIN_{Inductor}$	Inductor input voltage		8.5		80	
V_{OUT}	Output voltage range	$V_{OUT}/VIN_{Inductor}$ Max = 5 $VIN_{Inductor}$ = 8.5 to 24 V | V_{OUT} = 50 to 80 V $VIN_{Inductor}$ = 24 to 50 V | V_{OUT} = 80 to 130 V $VIN_{Inductor}$ = 50 to 80 V | V_{OUT} = 130 to 240 V	50		240	V
η	Peak efficiency	VIN_{IC} = 12 V, V_{OUT} = 130 V, I_{OUT} = 200 mA VIN_{IC} = 12 V, V_{OUT} = 240 V, I_{OUT} = 200 mA		95 95		%
$\Delta\varsigma_{OYT}$	Output Voltage Accuracy	including voltage ripple, from −40°C to 85°C, VIN_{IC} = 8.5 V to 18 V	−2		2	%

POWER UP SEQUENCE

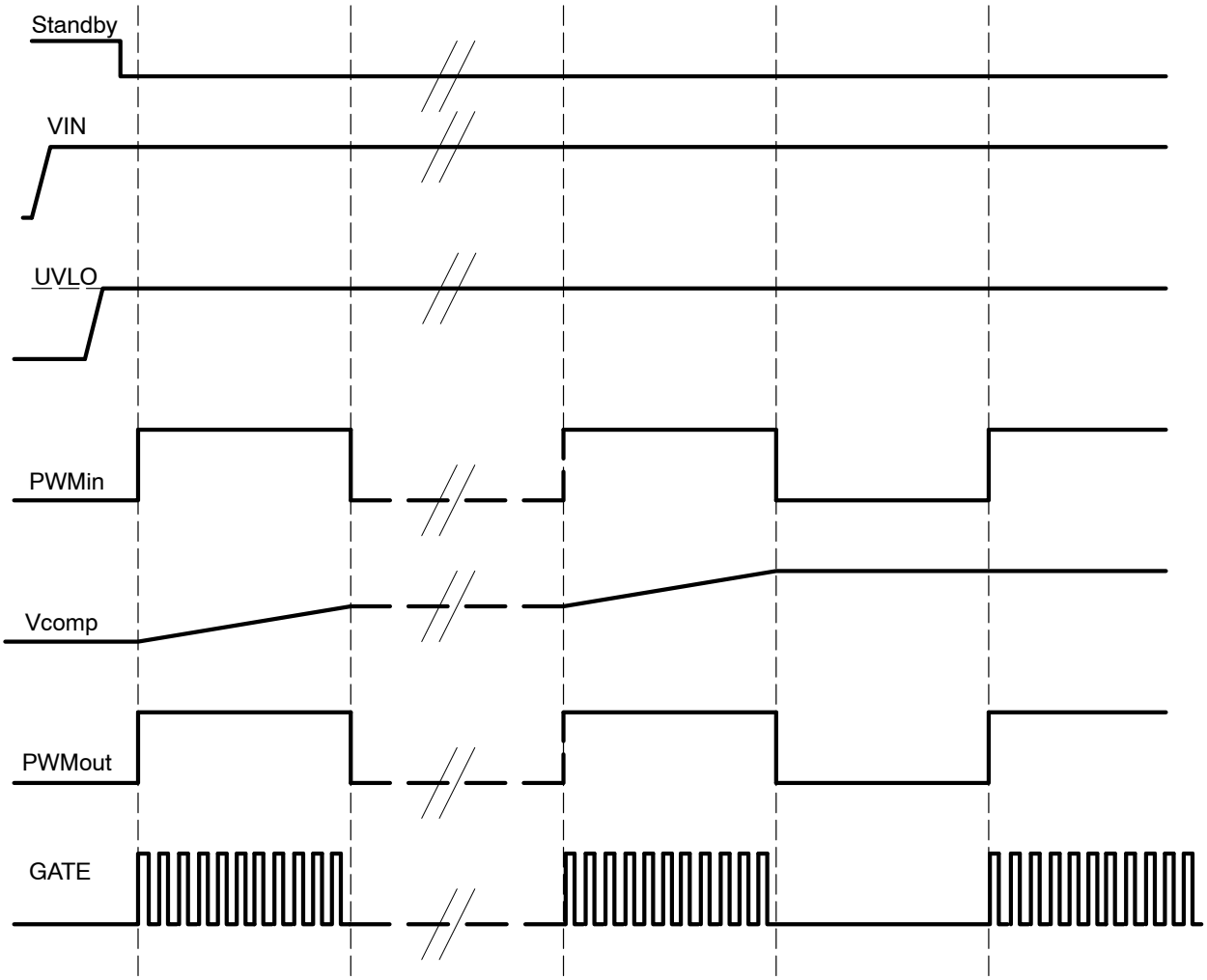


Figure 4. Soft Start Power Up from Standby

For the device to begin the soft start sequence the VIN pin voltage needs to be above the UVLO threshold and the OVP pin voltage needs to be above the V_{SCP} threshold. From standby mode soft start will begin when STBY pin goes low and PWMin pin goes high and lasts for a fixed number of clock cycles. This ensures that smooth start up if the device is powered on from standby with a PWM input.

STANDBY ON AND OFF SEQUENCE

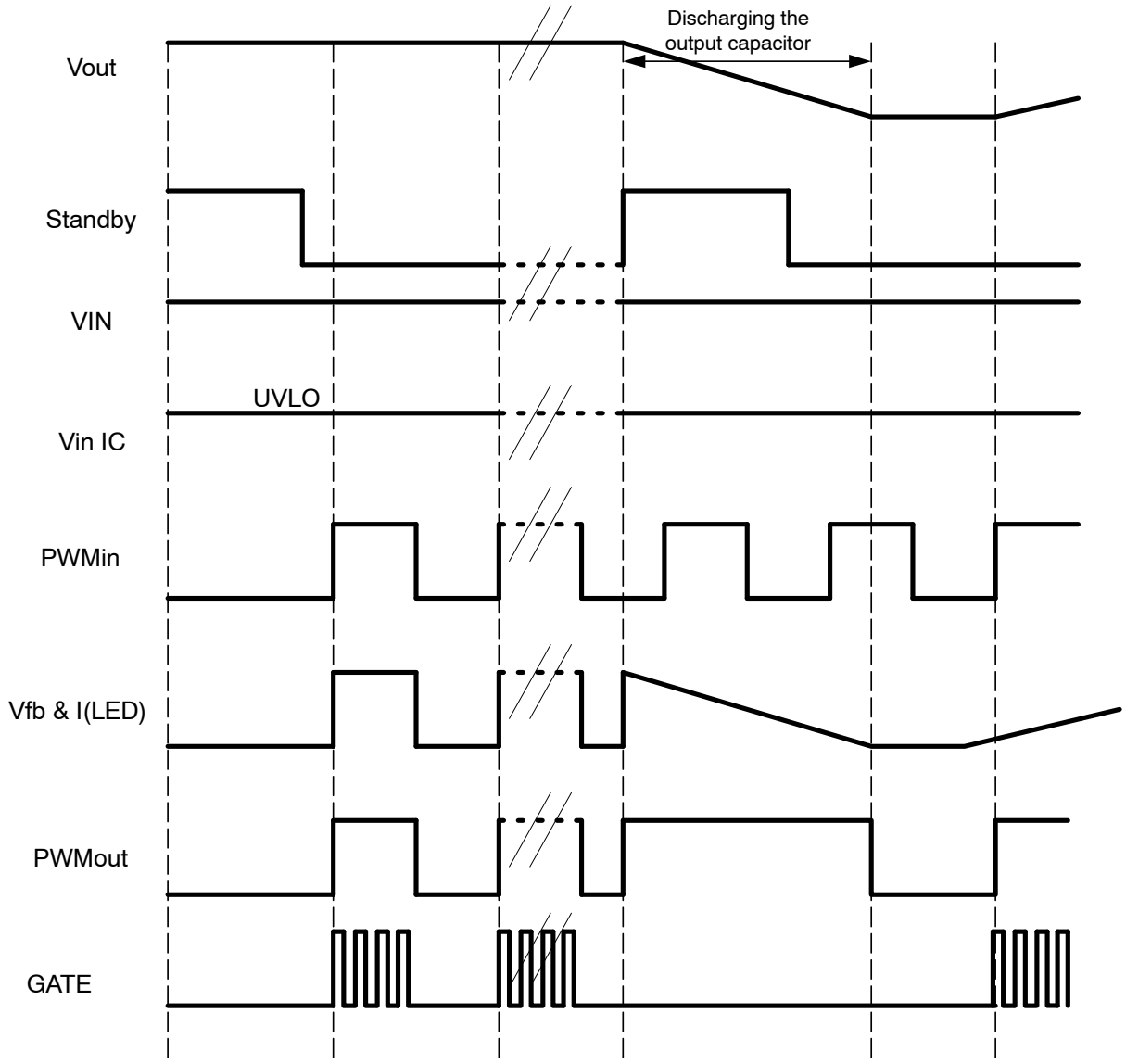


Figure 5. Entering Standby Mode

The STBY pin contains an internal 5 MΩ pull−up resistor to VREF. This resistor limits current consumption when the device is in standby mode and also ensures the device will remain in standby if the STBY pin is left floating.

When the STBY goes high the boost converter will stop switching and the PWMout pin will switch, or remain high for 50 ms. This allows the output capacitor to discharge and the LED current to fall to zero. The device will be in a low power standby mode and can begin soft start from the next enable sequence.

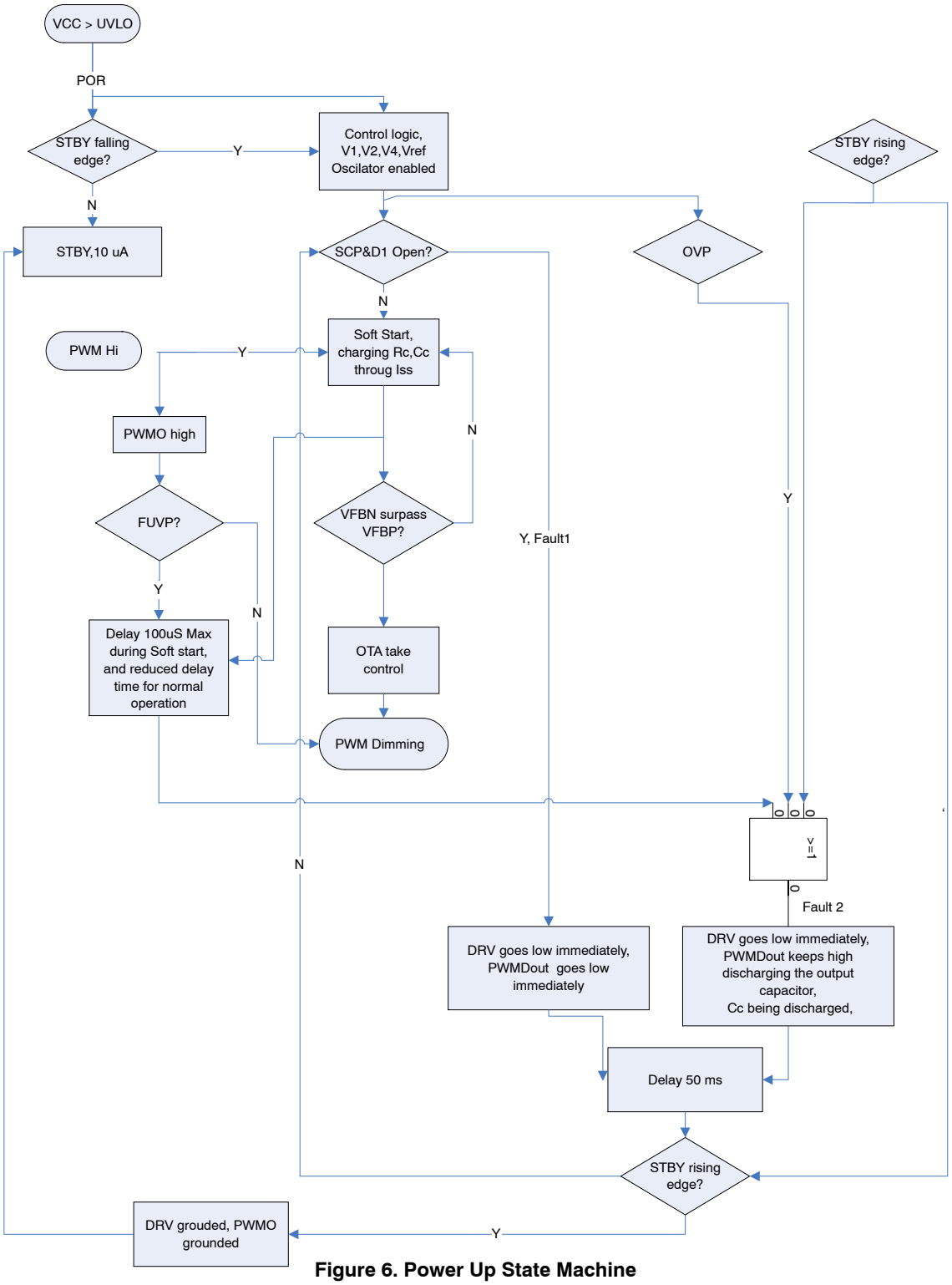


Figure 6. Power Up State Machine

SOFT START WITH PWM INPUT

Figure 7 below shows an example of a soft start when the device is powered up from standby with a PWM input. The PWM signal here is at 100 Hz with a duty cycle of 30%. In this case the LED reaches 100% of its programmed value in 100 ms. This time can be decreased if the PWM signal runs at a higher duty cycle.

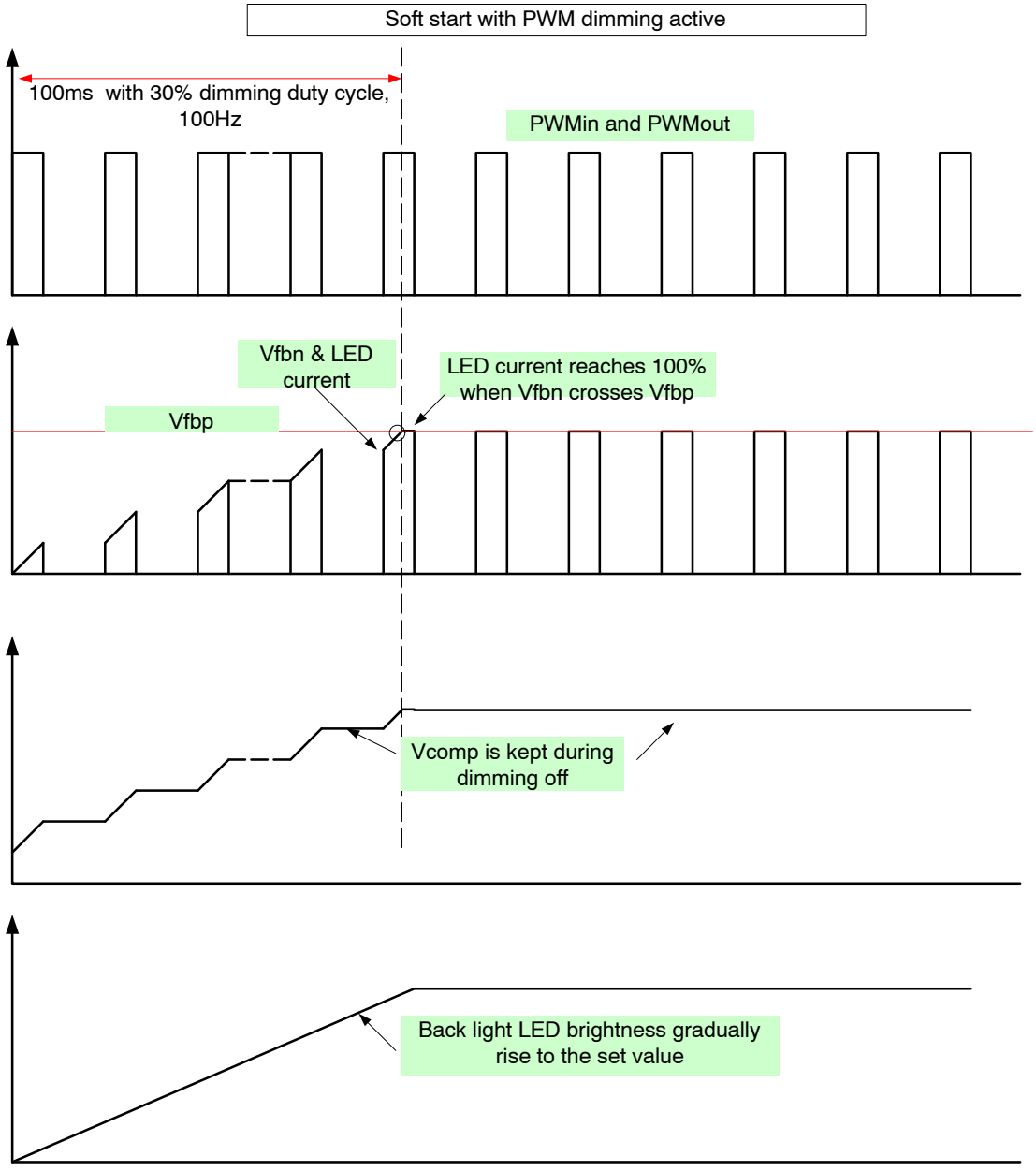


Figure 7. Soft Start with PWM Input

GATE AND PWMOUT PIN DRIVER CIRCUIT

Since external transistors are required for the boost converter and PWM dimming functions, the device contains an internal 10 V regulator to drive the gate of these transistors. In the case of the PWM transistor this also functions as a level translator for the PWMin input pin. When selecting external components it is important that the transistor has enough gate drive to ensure low $R_{DS(on)}$ for the expected current.

It should be noted that the internal 10 V regulator will start to drop when the VIN voltage is sufficiently low. When the V_{IN} voltage is 8.5 V the gate drivers will be limited to around 7.7 V.

VREF REFERENCE VOLTAGE

The device contains an accurate 5 V reference that can supply up to 10 mA and can be accessed through the VREF pin. It can be used to program the LED feedback voltage by using a resistor divider on the FBP pin. This reference is only active when STBY = low. When the device is in standby mode the VREF pin voltage will drop to 4.2 V typical with a minimum of 3.5 V. The VREF will return to 5 V immediately when STBY is driven high.

MINIMUM ON & OFF TIME

If the steady state duty cycle and switching frequency combine to generate short Ton times (low VOUT/VIN converter ratio), the converter will skip some cycles to regulate V_{OUT} which will increase output voltage ripple. The timing limit is set by the intrinsic loop propagation delay and the switching frequency will be limited by the minimum ON time and OFF time.

THE INDUCTOR SELECTION

For a given application, it is necessary to know the input voltage at the inductor ($VIN_{INDUCTOR}$), the output current (I_{OUT}) set by RFBN and the voltage on the FBP pin, and the switching frequency (F_{sw}). The inductor can be chosen using the formula below:

$$L_{max} < \frac{1}{2 \times F_{sw} \times I_{OUT}} \times \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \times \left(V_{OUT} - V_{IN}\right) \quad \text{(eq. 1)}$$

The minimal inductor value is determined with the desired peak current flowing through the inductor. Using the chosen inductor value the steady state duty cycle and peak inductor current can be calculated:

$$D = \frac{\sqrt{2 \times L \times F_{sw} \times I_{OUT} \times \left(V_{OUT} - V_{IN}\right)}}{V_{IN}} \quad \text{(eq. 2)}$$

And the inductor peak current is now:

$$I_{peak} = \frac{V_{IN} \times D}{L \times F_{sw}} = \sqrt{\frac{2 \times I_{OUT} \times (V_{OUT} - V_{IN})}{L \times F_{sw}}} \quad \text{(eq. 3)}$$

THE CURRENT SENSE RESISTOR

Set a current limit between 2 and 2.5 times the peak inductor current to account for inductor tolerance:

$$I_{limit} = 2.5 \times I_{peak} \quad \text{(eq. 4)}$$

The current limit reference fixed on the over-current protection comparator is V_{CS} = 0.5 V and the resistance can be calculated using following the equation:

$$R_{CS} = \frac{V_{CS}}{2.5 \times I_{peak}} \quad \text{(eq. 5)}$$

SLOPE COMPENSATION

After the current sense resistor is calculated additional calculations are needed for the external slope compensation ramp. Using the R_{SENSE} value the typical slope of the compensation ramp can be calculated:

$$Mramp = \frac{1}{2} R_{SENSE} \frac{V_{OUT} - V_{IN}}{L} \quad \text{(eq. 6)}$$

Using the typical value for , the external compensation resistor can be calculated as follows:

$$R_{SC} = \frac{M_{RAMP}}{I_{RAMP}} \quad \text{(eq. 7)}$$

The slope compensation ramp has an offset current, , which is used to calculate the peak ramp current and finally the adjusted current sense resistor.

$$I_{RAMP,peak} = I_{OFF} + D \frac{I_{RAMP}}{R_{SW}} \quad \text{(eq. 8)}$$

$$R_{CS} = \frac{V_{CS} - R_{CS} \times I_{RAMP,peak}}{I_{limit} + I_{RAMP,peak}} \quad \text{(eq. 9)}$$

OUTPUT CAPACITOR and OUTPUT VOLTAGE RIPPLE

Calculating the output voltage ripple will size the output capacitor value. The output voltage ripple equation below takes into account the parasitic impedance (ESR) of this output capacitor:

$$\Delta V_{COUT} = \frac{I_{OUT} \times (1 - D_2)}{C_{OUT} \times F_{sw}} + ESR \times I_{OUT} \quad \text{(eq. 10)}$$

$$\Delta V_{COUT} = \frac{I_{OUT}}{C_{OUT} \times F_{sw}} \times \left(1 - \frac{I_{peak} \times L \times F_{sw}}{V_{OUT} - V_{IN}}\right) + ESR \times I_{OUT} \quad \text{(eq. 11)}$$

Without taking into account the ESR, the output capacitor becomes:

$$C_{OUT} > \frac{I_{OUT}}{\Delta V_{OUT} \times F_{sw}} \times \left(1 - \frac{I_{peak} \times L \times F_{sw}}{V_{OUT} - V_{IN}}\right) \quad \text{(eq. 12)}$$

If the ESR value of the selected output capacitor is high, the voltage ripple will increase. The error due to the ESR can be estimated follow the equation below:

$$\Delta V_{OUTESR} = ESR \times I_{peak} \quad \text{(eq. 13)}$$

SIZING THE COMP PIN CAPACITOR

The transistor Q1 is turned ON (reset of the duty cycle) when the Vf of the output current amplifier reaches the control output voltage V_c. The control voltage V_c is simply a reduced voltage out of the follower servicing the voltage on the COMP pin. In steady state, at DT_{sw}, the voltage at the current amplifier output is represented by the equation below:

$$V_C = I_{peak} \times R_{CS} \times G_i \quad \text{(eq. 14)}$$

$$V_{comp} = V_C + V_{OS} \quad \text{(eq. 15)}$$

V_{comp} = COMP pin output voltage
V_c = Voltage Control of the transconductance amplifier
V_{os} = voltage offset of the transconductance amplifier

$$V_f = \frac{V_{IN} \times D \times R_{CS} \times G_i}{L \times F_{sw}} \quad \text{(eq. 16)}$$

$$i = C \times \frac{dv}{dt} \Rightarrow C_{comp} = \frac{i_{EA} \times t_{rise}}{V_{comp}} = \frac{i_{EA} \times t_{rise}}{V_c + V_{os}} \quad \text{(eq. 17)}$$

i_{EA} = 4 μA error amplifier output current capability
t_{rise} = soft start time
V_{os} = 0.9 V voltage offset due to the follower

So

$$C_{comp} < \frac{i_{EA} \times t_{rise}}{V_C + V_{OS}} \quad \text{(eq. 18)}$$

$$C_{comp} = 0.7 \times \frac{i_{EA} \times 30\ ms}{\frac{V_{IN} \times D \times R_{CS} \times G_L}{L \times F_{sw}} + V_{OS}} \quad \text{(eq. 19)}$$

During the soft start and with the dimming function activated, the COMP pin voltage is rising during 30 ms within the 100 ms soft start time so V_{comp} holds for another during 70 ms afterwards. Attention needs to be brought to the DC voltage rating. As the capacitor value decreases and the DC voltage increases, the value chosen needs to be

SIZING THE R_{comp} RESISTOR for the LOOP STABILITY

Combining Equations 2 and 16 gives the following expression for I_{OUT}:

$$I_{OUT} = \frac{V_f{}^2 \times L \times F_{sw}}{2 \times \left(V_{OUT} - V_{IN}\right) \times \left(R_{CS} \times G_i\right)^2} \quad \text{(eq. 20)}$$

To obtain the small signal equation, partial derivates of the output current are calculated with respect to the control voltage Vc and the output voltage V_{OUT}.

$$\frac{\partial I_{OUT}}{\partial V_{OUT}} = \frac{V_C \times L \times F_{sw}}{\left(V_{OUT} - V_{IN}\right) \times \left(R_{CS} \times G_i\right)^2} \quad \text{(eq. 21)}$$

$$\frac{\partial I_{OUT}}{\partial V_{OUT}} = \frac{V_C{}^2 \times L \times F_{sw}}{2 \times \left(V_{OUT} - V_{IN}\right)^2 \times \left(R_{CS} \times G_i\right)^2} = \frac{I_{OUT}}{V_{OUT} - V_{IN}} \quad \text{(eq. 22)}$$

From the AC model below the control to output transfer function can be calculated:

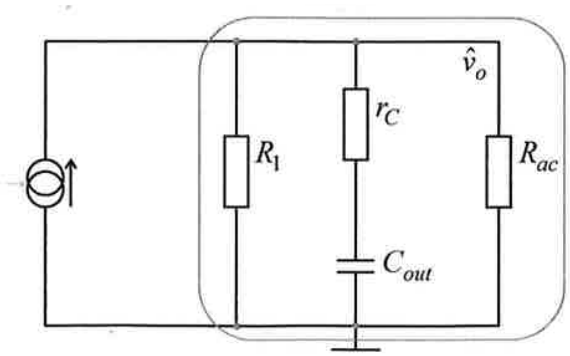


Figure 8. Control to Output Transfer Function

$$H(s) = \frac{V_{OUT}(s)}{V_C(s)} = \frac{V_{OUT}(s)}{I_{(s)}} \times \frac{I_{OUT}(s)}{V_C(s)} \quad \text{(eq. 23)}$$

$$H(s) = Z_{OUT}(s) \times \frac{I_{OUT}(s)}{V_C(s)} \quad \text{(eq. 24)}$$

$$Z_{OUT}(s) = \frac{\left(ESR + \frac{1}{sC_{OUT}}\right) \times R_{eq}}{\left(ESR + \frac{1}{sC_{OUT}}\right) + R_{eq}} = R_{eq} \times \frac{1 + s \times ESR \times C_{OUT}}{1 + s \times C_{OUT}\left(ESR + R_{eq}\right)} \quad \text{(eq. 25)}$$

Where

$$R_{eq} = \frac{R_{ac} \times R_1}{R_{ac} \times R_1}$$

$$R_1 = \frac{1}{\frac{I_{OUT}(s)}{V_{OUT}(s)}} = \frac{2 \times \left(V_{OUT} - V_{IN}\right)^2 \times \left(R_{cs} \times G_i\right)^2}{V_c{}^2 \times F_{sw} \times L} = \frac{V_{OUT} - V_{IN}}{I_{OUT}} \quad \text{(eq. 26)}$$

The dynamic resistance $r_{AC(LED)}$ is evaluated using the LED specification.

$$R_{AC} = R_{sense} + r_{AC(LED)} \times nb_{LED} \quad \text{(eq. 27)}$$

Theory

The control to output transfer function is expressed following the formula below:

$$H(s) = H_0 \times \frac{1 + \frac{s}{w_Z}}{1 + \frac{s}{s_p}} \quad \text{(eq. 28)}$$

Where

$$H_o = \frac{\partial I_{OUT}}{\partial V_C} \times R_{eq} = \frac{V_C \times L \times F_{sw}}{\left(V_{OUT} - V_{IN}\right) \times \left(R_{CS} \times G_I\right)^2} \times \frac{R_{AC} \times R_1}{R_{AC} + R_1} \quad \text{(eq. 29)}$$

$$H_o = \sqrt{\frac{2 \times I_{OUT} \times L \times F_{sw}}{\left(V_{OUT} - V_{IN}\right)}} \times \frac{1}{R_{CS} \times G_i} \times \frac{R_{AC} \times R_1}{R_{AC} + R_1} \quad \text{(eq. 30)}$$

$$f_p = \frac{1}{2\pi \times \left(ESR + R_{eq}\right) \times C_{OUT}} \quad \text{(eq. 31)}$$

There is also a right half plane zero:

$$f_z = \frac{1}{2\pi \times ESR \times C_{OUT}} \quad \text{(eq. 32)}$$

As the boost converter also operates in DCM, there is also a right half plane zero regulated to high frequency:

$$f_{rhpz} = \frac{2 \times f_{sw}}{2\pi \times D} \quad \text{(eq. 33)}$$

Type II compensation is used to compensate the two dominant poles f_p of the control to output transfer function. The compensator zero has to be placer at the f_p frequency of the transfer function.

$$f_p = \frac{1}{2\pi \times (ESR + R_{eq}) \times C_{OUT}} = f_z = \frac{1}{2\pi \times R_{comp} \times C_{comp}} \quad \text{(eq. 34)}$$

$$R_{comp} = \frac{(ESR + R_{eq}) \times C_{OUT}}{C_{comp}} \quad \text{(eq. 35)}$$

The dominant pole is expressed following the equation:

$$f_{p1} = \frac{1}{2\pi \times R_{EA} \times C_{comp}} \quad \text{(eq. 36)}$$

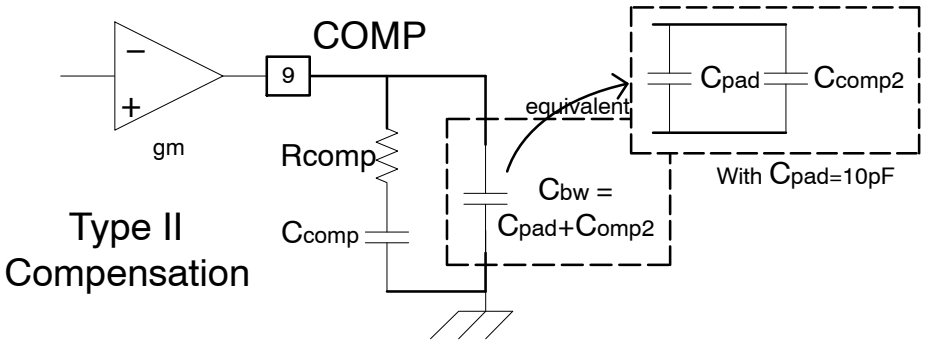


Figure 9. Slope Compensation Network

The natural second pole is expressed following the equation:

$$f_{p2} = \frac{1}{2\pi \times R_{comp} \times C_{bw}} \quad \text{(eq. 37)}$$

The zero is expressed following the equation:

$$f_z = \frac{1}{2\pi \times R_{comp} \times C_{comp}} \quad \text{(eq. 38)}$$

OSCILLATOR FREQUENCY SETTING

The simplified equation to set the switching frequency using resistor R_T:

$$f_{sw} = \frac{13750}{R_T + 5} \quad \text{(eq. 39)}$$

Where:
R_T is expressed in kΩ.
f_{sw} us expressed in kHz

FBP OPTIONS

The FBP pin is used to program the feedback voltage that sets the LED current. Typically a resistor divider is used from VREF to set the voltage between 0.5 V and 3.0 V. Additionally, to save component costs, the feedback voltage can be programmed with internal 0.8 V (±1.5%) by tying the FBP pin to ground.

FAULT DETECTION:

- Overvoltage Protection: A resistor divider from VOUT can be used to set the overvoltage protection on the OVP pin. When the OVP pin rises above 1.2 V the converter will shut off immediately and PWMout will be held high for 50 ms to discharge the output capacitor. After this time the device will enter standby mode requires a high to low transition on the STBY pin to restart.
- Short Circuit Protection: A resistor divider from VOUT can be used to set the short circuit protection on the OVP pin. When the OVP pin drops below 75 mV the converter will shut off immediately and enter standby mode. A high to low transition on the STBY pin is required to restart the device.
- Under Voltage Lockout (UVLO): The converter will immediately shut off and enter standby when the VIN pin voltage drops below 7.5 V. When the UVLO condition is cleared, a high to low transition on the STBY pin is required to restart the device.
- Temperature Shutdown: When the internal die temperature reaches 150°C, the device will behave the same as in the overvoltage condition.

Layout Guidance

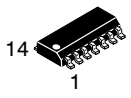
In switching converters it is important to use wide, short traces for components in the main switching path. Resistor RCS, which is in the main switching path through transistor Q1, should be connected to power ground (PGND). Compensation network components, resistor dividers, and bypass capacitors should be referenced to quiet ground (GND). Bypass capacitors should be connected as close to the IC as possible.

ORDERING INFORMATION

Device	Package	Shipping†
NCS29001DR2G	SOIC−14 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

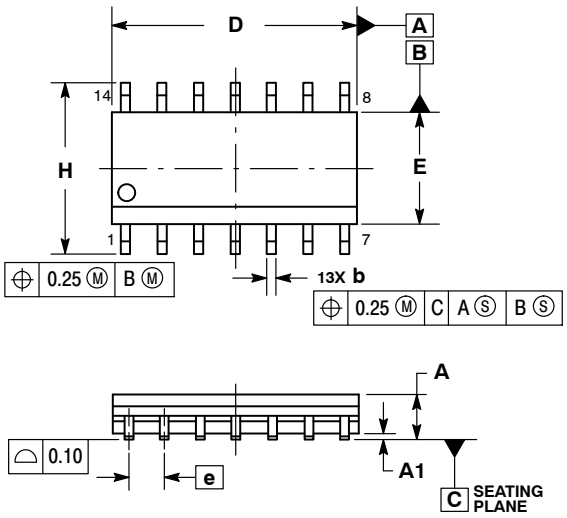
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

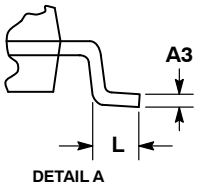


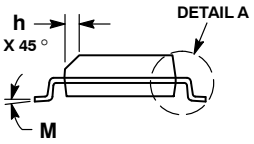
SCALE 1:1

SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



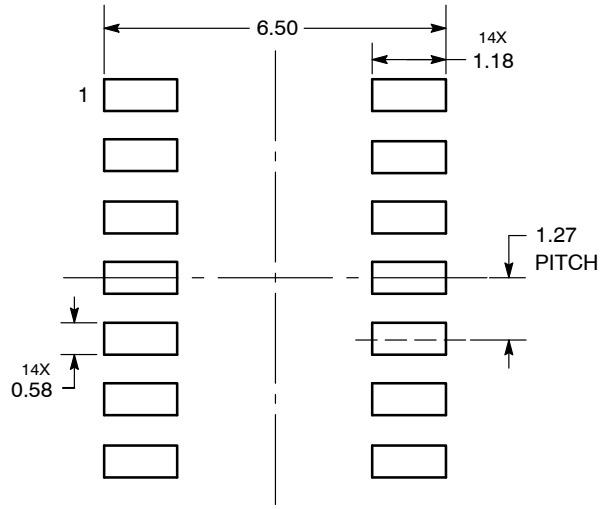




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

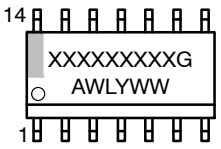
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−14 NB**		**PAGE 1 OF 2**

SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

PUBLICATION ORDERING INFORMATION

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