Dual MOSFET Gate Driver, High Performance

NCP81080

The NCP81080 is a high performance dual MOSFET gate driver optimized to drive half bridge N–Channel MOSFETs. The NCP81080 uses a bootstrap technique to ensure a proper drive of the high–side power switch. A high floating top driver design can accommodate HB voltage as high as 180 V. The NCP81080 has an internal anti–cross conduction circuit with a 135 ns fixed internal dead–time to prevent current shoot–through. The NCP81080 is available in 2x2mm DFN and SOIC packages.

Features
• Drives Two N–Channel MOSFETs in High–Side and Low–Side Configuration
• Floating Top Driver Accommodates Boost Voltage up to 180 V
• Switching Frequency up to 500 Khz
• Current Shoot–Through Protection
• 135 ns Fixed internal Dead–Time
• 44 ns Rising and 30 ns Falling Propagation Delay Times
• 0.5 A peak Source Current with 0.8 A Peak Sink Current
• 19 ns Rise/17 ns Fall Times with 1000–pF Load
• High–Side & Low–Side UVLO Protection

Applications
• Telecom and Datacom
• Isolated Non–Isolated Power Supply Architectures
• Class–D Audio Amplifiers
• Two Switch and Active Clamp Forward Converters
• Motor Drives

Figure 1. Typical Application Circuit
### Table 1. PIN DESCRIPTION TABLE

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VDD</td>
<td>Positive supply for the low-side driver</td>
</tr>
<tr>
<td>2</td>
<td>HI</td>
<td>High-Side Input</td>
</tr>
<tr>
<td>3</td>
<td>LI</td>
<td>Low-Side Input</td>
</tr>
<tr>
<td>4</td>
<td>VSS</td>
<td>Negative Supply Return</td>
</tr>
<tr>
<td>5</td>
<td>LO</td>
<td>Low-Side Output</td>
</tr>
<tr>
<td>6</td>
<td>HS</td>
<td>High-Side Source</td>
</tr>
<tr>
<td>7</td>
<td>HO</td>
<td>High-Side Output</td>
</tr>
<tr>
<td>8</td>
<td>HB</td>
<td>High-Side Bootstrap</td>
</tr>
<tr>
<td>9</td>
<td>EPAD</td>
<td>Connect EPAD to VSS</td>
</tr>
</tbody>
</table>

![Top View Diagram]

### Table 2. MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>−0.3 to 24</td>
<td>V</td>
</tr>
<tr>
<td>V_{HB} − V_{SS}</td>
<td>−0.3 to 200</td>
<td>V</td>
</tr>
<tr>
<td>V_{HO} − V_{HS}</td>
<td>DC −0.3 to V_{HB} + 0.3</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Repetitive Pulse &lt; 100 ns</td>
<td></td>
</tr>
<tr>
<td>V_{HS} − V_{SS}</td>
<td>DC −20 to 200 − VDD V_{HS}</td>
<td>V</td>
</tr>
<tr>
<td>V_{LO} − V_{SS}</td>
<td>DC −0.3 to VDD + 0.3</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Repetitive pulse &lt; 100 ns</td>
<td></td>
</tr>
<tr>
<td>V_{HI}, V_{LI}</td>
<td>−10 to 24</td>
<td>V</td>
</tr>
<tr>
<td>V_{HB} − V_{HS}</td>
<td>−0.3 to 24</td>
<td>V</td>
</tr>
<tr>
<td>I_{Diode}</td>
<td>AC (Peak current)</td>
<td>8 A</td>
</tr>
<tr>
<td>Operating virtual Junction Temp Range, T_{J}</td>
<td>−40 to 170</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature, T_{STG}</td>
<td>−65 to 150</td>
<td>°C</td>
</tr>
<tr>
<td>Lead Temperature (Soldering, 10 sec)</td>
<td>+300</td>
<td>°C</td>
</tr>
<tr>
<td>HBM</td>
<td>800</td>
<td>V</td>
</tr>
<tr>
<td>CDM</td>
<td>2000</td>
<td>V</td>
</tr>
</tbody>
</table>

### Table 3. RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{DD}</td>
<td>5.5</td>
<td>12</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>V_{HS}</td>
<td>−10</td>
<td></td>
<td>180</td>
<td></td>
</tr>
<tr>
<td>V_{HB}</td>
<td>V_{HS} + 5.5</td>
<td>V_{HS} + 20</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage Slew Rate on HS</td>
<td>30</td>
<td></td>
<td>V / ns</td>
<td></td>
</tr>
<tr>
<td>T_{J}</td>
<td>−40</td>
<td></td>
<td>+140</td>
<td>°C</td>
</tr>
</tbody>
</table>

www.onsemi.com
Table 4. ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Thermal Characteristic</th>
<th>DFN</th>
<th>SOIC</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \theta_{JA} ) Junction to Ambient thermal resistance</td>
<td>97</td>
<td>146</td>
<td>°C/W</td>
</tr>
<tr>
<td>( \theta_{JCT} ) Junction to case (Top) thermal resistance</td>
<td>181</td>
<td>72</td>
<td></td>
</tr>
<tr>
<td>( \theta_{JCB} ) Junction to case (Bottom) thermal resistance</td>
<td>1.9</td>
<td>67</td>
<td></td>
</tr>
<tr>
<td>( \psi_{JT} ) Junction to top characterization parameter</td>
<td>2.2</td>
<td>7.2</td>
<td></td>
</tr>
<tr>
<td>( \psi_{JB} ) Junction to board characterization parameter</td>
<td>2.0</td>
<td>64</td>
<td></td>
</tr>
<tr>
<td>Moisture Sensitivity Level – QFN Package</td>
<td>MSL</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

*The maximum package power dissipation must be observed.
2) JESD 51–5 (1S2P Direct–Attach Method) with 0 LFM
3) JESD 51–7 (1S2P Direct–Attach Method) with 0 LFM
*All signals referenced to VSS unless otherwise noted.

Table 5. ELECTRICAL CHARACTERISTICS

Unless otherwise stated: \( T_a = T_j = -40°C \) to 140°C; VDD = VHB = 12 V, VHS = VSS = 0 V, No load on LO or HO

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SUPPLY CURRENTS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{DD} ) VDD quiescent current</td>
<td>( V_{LI} = V_{HI} = 0 )</td>
<td>0.85</td>
<td>1.6</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>( I_{DDO} ) VDD operating current</td>
<td>( f = 500 \text{kHz}, C_{LOAD} = 0 )</td>
<td>5.1</td>
<td>9.0</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( f = 300 \text{kHz}, C_{LOAD} = 0 )</td>
<td>3.5</td>
<td>6.5</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>( I_{HB} ) Boot voltage quiescent current</td>
<td>( V_{LI} = V_{HI} = 0 \text{V} )</td>
<td>0.65</td>
<td>1.6</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>( I_{HBO} ) Boot voltage operating current</td>
<td>( f = 500 \text{kHz}, C_{LOAD} = 0 )</td>
<td>4.8</td>
<td>9.0</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( f = 300 \text{kHz}, C_{LOAD} = 0 )</td>
<td>3.4</td>
<td>6.5</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>( I_{HBS} ) HB to Vss quiescent current</td>
<td>( V_{HS} = V_{HB} = 110 \text{V} )</td>
<td>8.0</td>
<td>100</td>
<td>( \mu )A</td>
<td></td>
</tr>
<tr>
<td>( I_{HBSO} ) HB to Vss operating current</td>
<td>( f = 500 \text{kHz}, C_{LOAD} = 0 )</td>
<td>0.2</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td><strong>INPUT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{HIH}, V_{LIH} ) Input voltage high</td>
<td></td>
<td>2.0</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{HIL}, V_{LIL} ) Input voltage low</td>
<td></td>
<td>0.8</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( R_{IN} ) Input Pulldown Resistance</td>
<td></td>
<td>100</td>
<td>175</td>
<td>350</td>
<td>kΩ</td>
</tr>
<tr>
<td><strong>UNDERVOLTAGE PROTECTION (UVLO)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VDD</td>
<td>VDD rising threshold</td>
<td>3.4</td>
<td>4.4</td>
<td>5.4</td>
<td>V</td>
</tr>
<tr>
<td>VDD</td>
<td>VDD Threshold hysteresis</td>
<td></td>
<td>0.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VHB</td>
<td>VHB rising threshold</td>
<td>3.4</td>
<td>4.4</td>
<td>5.4</td>
<td>V</td>
</tr>
<tr>
<td>VHB</td>
<td>VHB Threshold hysteresis</td>
<td></td>
<td>0.35</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td><strong>BOOTSTRAP DIODE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_F ) Low–current forward voltage</td>
<td>( I_{VDD} = \text{HB} = 100 \text{mA} )</td>
<td>0.61</td>
<td>0.85</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{FI} ) High–current forward voltage</td>
<td>( I_{VDD} = \text{HB} = 100 \text{ mA} )</td>
<td>0.93</td>
<td>1.1</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( R_D ) Dynamic resistance, ( \Delta V_F/\Delta I )</td>
<td>( I_{VDD} = \text{HB} = 100 \text{mA} and 80 \text{mA} )</td>
<td>2.1</td>
<td>3.5</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td><strong>LO GATE DRIVER</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{LOL} ) Low level output voltage</td>
<td>( I_{LO} = 100 \text{mA} )</td>
<td>0.31</td>
<td>1.2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{LOH} ) High level output voltage</td>
<td>( I_{LO} = \text{HB} = 100 \text{mA}, V_{LOH} = V_{DD} - V_{LO} )</td>
<td>0.75</td>
<td>1.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Peak Pull–Up Current</td>
<td>( V_{LO} = 0 \text{V} )</td>
<td>0.55</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>Peak Pull–Down Current</td>
<td>( V_{LO} = 12 \text{V} )</td>
<td>0.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( R_O ), Unbiased</td>
<td>VCC = VSS</td>
<td>20k</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
</tbody>
</table>
### Table 5. ELECTRICAL CHARACTERISTICS

Unless otherwise stated: $T_A = T_J = -40^\circ C$ to $140^\circ C$; $VDD = VHB = 12 V$, $VHS = VSS = 0 V$, No load on LO or HO

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>HO GATE DRIVER</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{HOL}$ Low level output voltage</td>
<td>$I_{HO} = 100 mA$</td>
<td>0.3</td>
<td>1.2</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{HOH}$ High level output voltage</td>
<td>$I_{HO} = -100 mA, V_{HOH} = V_{HB} - V_{HO}$</td>
<td>0.71</td>
<td>1.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Peak Pull-Up Current</td>
<td>$V_{HO} = 0 V$</td>
<td>0.55</td>
<td></td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Peak Pull-Down Current</td>
<td>$V_{HO} = 12 V$</td>
<td>0.8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_O$, Unbiased</td>
<td>HB – HS = 0 V</td>
<td>20k</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
</tbody>
</table>

### PROPAGATION DELAYS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{DLFF}$ PWM falling to VLO falling</td>
<td>$C_{LOAD} = 0$</td>
<td>30</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{DHFF}$ PWM falling to VHO falling</td>
<td>$C_{LOAD} = 0$</td>
<td>30</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{DLRR}$ PWM rising to VLO rising</td>
<td>$C_{LOAD} = 0$</td>
<td>44</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{DHRR}$ PWM rising to VHO rising</td>
<td>$C_{LOAD} = 0$</td>
<td>44</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### DEAD–TIME

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fixed Deadtime</td>
<td>Internal Fixed Dead–Time</td>
<td>135</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

### DEAD–TIME MATCHING

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{DTM}$ LI OFF, HI ON</td>
<td></td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

### OUTPUT RISE AND FALL TIME

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_R$ LO, HO</td>
<td>$C_{LOAD} = 1000 pF$</td>
<td>19</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_F$ LO, HO</td>
<td>$C_{LOAD} = 1000 pF$</td>
<td>17</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### MISCELLANEOUS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum input pulse width that changes the output</td>
<td></td>
<td>30</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Bootstrap diode turn–off time</td>
<td>$I_F = 20 mA, I_{REV} = 0.5 A$ (Notes 1, 2)</td>
<td>50</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Typical values for $T_A = 25^\circ C$
2. $I_F$: Forward current applied to bootstrap diode, $I_{REV}$: Reverse current applied to bootstrap diode.
Figure 2. Internal Block Diagram

Figure 3. Timing Diagram

NOTE: The NCP81080 has a fixed internal dead-time of 135 ns.
Figure 5. Dead-Time Matching

Figure 6. Propagation Delays
TYPICAL CHARACTERISTICS

Figure 7. Propagation Delays vs. Supply Voltage

Figure 8. Propagation Delays vs. Temperature

Figure 9. Input Thresholds vs. Supply Voltage

Figure 10. Input Thresholds vs. Temperature

Figure 11. Supply Current vs. Frequency

Figure 12. Diode Current vs. Diode Voltage
TYPICAL CHARACTERISTICS

Figure 13. Quiescent Current vs. Supply Voltage

Figure 14. Quiescent Current vs. Supply Voltage

Figure 15. Quiescent Current vs. Supply Voltage

Figure 16. Quiescent Current vs. Supply Voltage
The NCP81080 is a high performance dual MOSFET gate driver optimized to drive half bridge N–Channel MOSFETs. A high and a Low input signals are all that is required to properly drive the power stage. The input signals are independently controlled and monitored by an anti–cross conduction circuit in order to prevent current shoot through. The NCP81080 has UVLO protections for the high–side and low–side drivers forcing the outputs low if the bias supplies drop below the specified UVLO thresholds. The NCP81080 also features an on–chip high voltage bootstrap diode which reduces the external component count. The NCP81080 has a fixed internal dead–time of 135 ns.

Driver Supply Voltage

As a general rule of thumb the local bypass should be 20 times the bootstrap capacitor. It is recommended to use a 4.7 μF bypass capacitor on VDD to VSS. The bootstrap capacitor is recharged on a cycle by cycle basis through the bootstrap diode from the VDD bypass capacitor. The charging cycle involves bursts in peak currents that require careful considerations by keeping a tight layout and short loops to avoid reliability issues.

If for any reason the application requires the VDD voltage to discharge to ground at rapid rates (3 + V/μs) the user is required to add an external diode between the supply voltage and the bypass capacitor.

![Figure 17. VDD Diode](image)

Low–Side Driver

The low side driver is designed to drive low RDS_{ON} N–channel MOSFETs. The typical output resistances for the driver are 7.5 ohms for sourcing and 3.1 ohms for sinking gate current. The bias to the low side driver is internally connected to the VDD supply and VSS. When the driver is enabled, the driver’s output is in phase with LI. When the NCP81080 is disabled, the low side gate is held low.

High–Side Driver

The high side driver is designed to drive a floating low RDS_{ON} N–channel MOSFET. The output resistances for the driver are 7.1 ohms for sourcing and 3.1 ohms for sinking gate current. The bias voltage for the high side driver is realized by an external bootstrap supply circuit which is connected between the HB and HS Pins.

Table 6. TYPICAL EXTERNAL CURRENT LIMITING RESISTOR VALUES

<table>
<thead>
<tr>
<th>VDD (V)</th>
<th>Bootstrap Capacitor (μF)</th>
<th>External Resistor (ohms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>0.1</td>
<td>2</td>
</tr>
<tr>
<td>12</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>18</td>
<td>0.1</td>
<td>3</td>
</tr>
</tbody>
</table>

![Figure 18. External Current Limiting Resistor](image)

UVLO (Under Voltage Lockout)

The bias supplies of the high–side and low–side drivers have UVLO protection. The VDD UVLO disables both drivers when the VDD voltage crosses the specified threshold. The typical rising threshold is 4.4 V with 0.4 V hysteresis. The VHB UVLO disables only the high–side driver when the VHB to VHS is below the specified...
threshold. The typical VHB UVLO rising threshold is 4.4 V with 0.35 V hysteresis.

At power up, when the supply voltage ramps up to set VDD and crosses the UVLO thresholds, users must take into account a 20 μs delay before the output drivers can react to a logic input. The 20 μs delay applies to both High–side and Low–side drivers. Figure 4 only shows the delay for the low–side channel.

**Input Stage**

The input stage of the NCP81080 is TTL compatible. The logic rising threshold level is 2.0 V and the logic falling threshold is 0.8 V.

**Cross–Conduction Protection**

The NCP81080’s inputs HI & LI are controlled independently. In order to prevent the power stage MOSFETs from turning on at the same time an internal logic circuit is implemented to monitor the state of HI & LI. If both input signals are high at the same time, the output signals HO & LO are forced low. (See Timing Diagram)

**UVLO Crossing**

When VDD & VHB cross their respective UVLO thresholds if HI and LI were already set the NCP81080 will keep HO pulled Low until it detects a rising edge on HI, however LO will follow LI allowing the Low–Side FET to turn on. (Refer to Figure 4)

**Layout Guidelines**

Gate drivers experience high di/dt during the switching transitions. So, the inductance at the gate drive traces must be minimized to avoid excessive ringing on the switch node. Gate drive traces should be kept as short and wide (>20 mil) as practical. The input capacitor must be placed as close as possible to the IC. Connect the VSS pin of the NCP81080 as close as possible to the source of the lower MOSFET. The use of vias is highly desirable to maximize thermal conduction away from driver.
For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**NOTES:**
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

**RECOMMENDED SOLDERING FOOTPRINT***

**GENDER MARKING DIAGRAM***

XX = Specific Device Code
M = Date Code
* = Pb−Free Device

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “*”, may or may not be present. Some products may not follow the Generic Marking.

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**DOCUMENT NUMBER:** 98AON18658D

**DESCRIPTION:** DFN8, 2.0X2.0, 0.5MM PITCH

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SOIC–8 NB
CASE 751–07
ISSUE AK

DATE 16 FEB 2011

NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

<table>
<thead>
<tr>
<th>DIMENSIONS</th>
<th>MILLIMETERS</th>
<th>INCHES</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>4.80–5.00</td>
<td>0.189–0.197</td>
</tr>
<tr>
<td>B</td>
<td>3.80–4.00</td>
<td>0.150–0.157</td>
</tr>
<tr>
<td>C</td>
<td>1.35–1.75</td>
<td>0.053–0.069</td>
</tr>
<tr>
<td>D</td>
<td>0.53–0.51</td>
<td>0.021–0.020</td>
</tr>
<tr>
<td>G</td>
<td>1.27 BSC</td>
<td>0.050 BSC</td>
</tr>
<tr>
<td>H</td>
<td>0.10–0.25</td>
<td>0.004–0.010</td>
</tr>
<tr>
<td>J</td>
<td>0.19–0.25</td>
<td>0.007–0.010</td>
</tr>
<tr>
<td>K</td>
<td>0.40–1.27</td>
<td>0.016–0.050</td>
</tr>
<tr>
<td>M</td>
<td>0–8</td>
<td>0–0.312</td>
</tr>
<tr>
<td>N</td>
<td>0.25–0.50</td>
<td>0.010–0.020</td>
</tr>
<tr>
<td>S</td>
<td>5.80–6.20</td>
<td>0.228–0.244</td>
</tr>
</tbody>
</table>

SCALE 1:1

SOLDERING FOOTPRINT*

Discrete

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
Pb-Free Package

Discrete (Pb–Free)

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “*”, may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2
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**CASE 751–07**  
**ISSUE AK**  

**STYLE 1:**  
1. **EMITTER**  
2. **COLLECTOR**  
3. **SOURCE**  
4. **GATE**  
5. **ELECTROMAGNETIC EMISSION**  
6. **BASE**  
7. **DRAIN**  
8. **EMITTER**

**STYLE 2:**  
1. **COLLECTOR, DIE, #1**  
2. **COLLECTOR, DIE, #2**  
3. **SOURCE**  
4. **GATE**

**STYLE 3:**  
1. **DRAIN**  
2. **INPUT**  
3. **GROUND**  
4. **VCC**  
5. **BASE**  
6. **SOURCE**  
7. **EMITTER**

**STYLE 4:**  
1. **ANODE**  
2. **BASE, DIE #1**  
3. **BASE, DIE #2**  
4. **COLLECTOR, #2**

**STYLE 5:**  
1. **INPUT**  
2. **EXTERNAL BYPASS**  
3. **GROUND**

**STYLE 6:**  
1. **SOURCE**  
2. **DRAIN**  
3. **GROUND**

**STYLE 7:**  
1. **SECOND STAGE Vd**  
2. **SOURCE**  
3. **GATE**  
4. **DRAIN**

**STYLE 8:**  
1. **COLLECTOR, DIE #1**  
2. **BASE, DIE #1**  
3. **BASE, DIE #2**  
4. **COLLECTOR, #2**

**STYLE 9:**  
1. **N.C.**  
2. **SOURCE**  
3. **GROUND**  
4. **DRAIN**

**STYLE 10:**  
1. **VCC**  
2. **VCC**  
3. **GROUND**  
4. **DRAIN**

**STYLE 11:**  
1. **ILIMIT**  
2. **ENABLE**  
3. **GATE**  
4. **SOURCE**

**STYLE 12:**  
1. **ANODE**  
2. **BASE, DIE #1**  
3. **BASE, DIE #2**  
4. **COLLECTOR, #2**

**STYLE 13:**  
1. **N.C.**  
2. **SOURCE**  
3. **GROUND**  
4. **DRAIN**

**STYLE 14:**  
1. **VCC**  
2. **VCC**  
3. **GROUND**  
4. **DRAIN**

**STYLE 15:**  
1. **ILIMIT**  
2. **ENABLE**  
3. **GATE**  
4. **SOURCE**

**STYLE 16:**  
1. **ANODE**  
2. **BASE, DIE #1**  
3. **BASE, DIE #2**  
4. **COLLECTOR, #2**

**STYLE 17:**  
1. **VCC**  
2. **VCC**  
3. **GROUND**  
4. **DRAIN**

**STYLE 18:**  
1. **ILIMIT**  
2. **ENABLE**  
3. **GATE**  
4. **SOURCE**

**STYLE 19:**  
1. **VCC**  
2. **VCC**  
3. **GROUND**  
4. **DRAIN**

**STYLE 20:**  
1. **ANODE**  
2. **BASE, DIE #1**  
3. **BASE, DIE #2**  
4. **COLLECTOR, #2**

**STYLE 21:**  
1. **CATHODE 1**  
2. **CATHODE 2**  
3. **CATHODE 3**  
4. **CATHODE 4**  
5. **CATHODE 5**  
6. **COMMON ANODE**  
7. **COMMON ANODE**  
8. **CATHODE 6**

**STYLE 22:**  
1. **I/O LINE 1**  
2. **COMMON CATHODE/VCC**  
3. **COMMON CATHODE/VCC**  
4. **I/O LINE 3**  
5. **COMMON ANODE/GND**  
6. **I/O LINE 4**  
7. **COMMON ANODE/GND**  
8. **I/O LINE 5**

**STYLE 23:**  
1. **LINE 1 IN**  
2. **COMMON ANODE/GND**  
3. **COMMON ANODE/GND**  
4. **LINE 2 IN**  
5. **LINE 2 OUT**  
6. **COMMON ANODE/GND**  
7. **COMMON ANODE/GND**  
8. **LINE 1 OUT**

**STYLE 24:**  
1. **BASE**  
2. **EMITTER**  
3. **COLLECTOR/ANODE**  
4. **COLLECTOR/ANODE**  
5. **CATHODE**  
6. **CATHODE**  
7. **COLLECTOR/ANODE**  
8. **COLLECTOR/ANODE**

**STYLE 25:**  
1. **VIN**  
2. **N/C**  
3. **REXT**  
4. **GND**  
5. **IOUT**  
6. **IOUT**  
7. **IOUT**  
8. **IOUT**

**STYLE 26:**  
1. **GND**  
2. **ILIMIT**  
3. **SOURCE**  
4. **SOURCE**

**STYLE 27:**  
1. **ILIMIT**  
2. **ENABLE**  
3. **SOURCE**  
4. **SOURCE**

**STYLE 28:**  
1. **SW_TO_GND**  
2. **DASIC_OFF**  
3. **DASIC_SW_DET**  
4. **GND**  
5. **V_MON**  
6. **VBULK**  
7. **VBULK**  
8. **VIN**

**STYLE 29:**  
1. **BASE, DIE #1**  
2. **EMITTER, #1**  
3. **BASE, #2**  
4. **EMITTER, #2**  
5. **COLLECTOR, #2**  
6. **COLLECTOR, #2**  
7. **COLLECTOR, #1**  
8. **COLLECTOR, #1**

**STYLE 30:**  
1. **DRAIN**  
2. **DRAIN**  
3. **DRAIN**  
4. **SOURCE**  
5. **SOURCE**  
6. **SOURCE**  
7. **SOURCE**  
8. **GATE**

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**DOCUMENT NUMBER:** 98ASB42564B  
**DESCRIPTION:** SOIC–8 NB  
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