Dual MOSFET Gate Driver, High Performance

NCP81080

The NCP81080 is a high performance dual MOSFET gate driver optimized to drive half bridge N-Channel MOSFETs. The NCP81080 uses a bootstrap technique to ensure a proper drive of the high-side power switch. A high floating top driver design can accommodate HB voltage as high as 180 V. The NCP81080 has an internal anti-cross conduction circuit with a 135 ns fixed internal dead-time to prevent current shoot-through. The NCP81080 is available in 2x2mm DFN and SOIC packages.

Features

• Drives Two N-Channel MOSFETs in High-Side and Low-Side Configuration
• Floating Top Driver Accommodates Boost Voltage up to 180 V
• Switching Frequency up to 500 KHz
• Current Shoot-Through Protection
• 135 ns Fixed Internal Dead-Time
• 44 ns Rising and 30 ns Falling Propagation Delay Times
• 0.5 A peak Source Current with 0.8 A Peak Sink Current
• 19 ns Rise/17 ns Fall Times with 1000-pF Load
• High-Side & Low-Side UVLO Protection

Applications

• Telecom and Datacom
• Isolated Non-Isolated Power Supply Architectures
• Class-D Audio Amplifiers
• Two Switch and Active Clamp Forward Converters
• Motor Drives

Figure 1. Typical Application Circuit
### Table 1. PIN DESCRIPTION TABLE

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VDD</td>
<td>Positive supply for the low-side driver</td>
</tr>
<tr>
<td>2</td>
<td>HI</td>
<td>High-Side Input</td>
</tr>
<tr>
<td>3</td>
<td>LI</td>
<td>Low-Side Input</td>
</tr>
<tr>
<td>4</td>
<td>VSS</td>
<td>Low-Side Input</td>
</tr>
<tr>
<td>5</td>
<td>LO</td>
<td>Low-Side Output</td>
</tr>
<tr>
<td>6</td>
<td>HS</td>
<td>High-Side Source</td>
</tr>
<tr>
<td>7</td>
<td>HO</td>
<td>High-Side Output</td>
</tr>
<tr>
<td>8</td>
<td>HB</td>
<td>High-Side Bootstrap</td>
</tr>
<tr>
<td>9</td>
<td>EPAD</td>
<td>Connect EPAD to VSS</td>
</tr>
</tbody>
</table>

### Table 2. MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>−0.3</td>
<td>to</td>
<td>24</td>
<td>V</td>
</tr>
<tr>
<td>V_{HB} − V_{SS}</td>
<td>−0.3</td>
<td>to</td>
<td>200</td>
<td>V</td>
</tr>
<tr>
<td>V_{HO} − V_{HS}</td>
<td>DC</td>
<td>−0.3</td>
<td>to V_{HB} + 0.3</td>
<td>V</td>
</tr>
<tr>
<td>Repetitive Pulse &lt; 100 ns</td>
<td>−2 to V_{HB} + 0.3, (V_{HB} − V_{HS} &lt;20)</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{HS} − V_{SS}</td>
<td>DC</td>
<td>−20</td>
<td>to 200 − VDD</td>
<td>V</td>
</tr>
<tr>
<td>Repetitive pulse &lt; 100 ns</td>
<td>−0.3 to VDD + 0.3</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{HI}, V_{LI}</td>
<td>−10</td>
<td>to</td>
<td>24</td>
<td>V</td>
</tr>
<tr>
<td>V_{HB} − V_{HS}</td>
<td>−0.3</td>
<td>to</td>
<td>24</td>
<td>V</td>
</tr>
<tr>
<td>(I_{Diode})</td>
<td>AC (Peak current)</td>
<td>8</td>
<td>A</td>
<td></td>
</tr>
</tbody>
</table>

Operating virtual Junction Temp Range, \(T_J\)  
Storage Temperature, \(T_{STG}\)  
Lead Temperature (Soldering, 10 sec)  
HBM  
CDM

### Table 3. RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{DD})</td>
<td>Supply Voltage Range</td>
<td>5.5</td>
<td>12</td>
<td>20</td>
</tr>
<tr>
<td>(V_{HS})</td>
<td>Voltage on HS (DC)</td>
<td>−10</td>
<td>180</td>
<td></td>
</tr>
<tr>
<td>(V_{HB})</td>
<td>Voltage on HB</td>
<td>(V_{HS} + 5.5)</td>
<td>(V_{HS} + 20)</td>
<td></td>
</tr>
<tr>
<td>Voltage Slew Rate on HS</td>
<td>30</td>
<td>V / ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(T_J)</td>
<td>Operating Junction Temperature Range</td>
<td>−40</td>
<td>+140</td>
<td>°C</td>
</tr>
</tbody>
</table>
Table 4. ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Thermal Characteristic</th>
<th>DFN</th>
<th>SOIC</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\theta_{JA}$ Junction to Ambient thermal resistance</td>
<td>97</td>
<td>146</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\theta_{JCT}$ Junction to case (Top) thermal resistance</td>
<td>181</td>
<td>72</td>
<td></td>
</tr>
<tr>
<td>$\theta_{JCB}$ Junction to case (Bottom) thermal resistance</td>
<td>1.9</td>
<td>67</td>
<td></td>
</tr>
<tr>
<td>$\psi_{JT}$ Junction to top characterization parameter</td>
<td>2.2</td>
<td>7.2</td>
<td></td>
</tr>
<tr>
<td>$\psi_{JB}$ Junction to board characterization parameter</td>
<td>2.0</td>
<td>64</td>
<td></td>
</tr>
<tr>
<td>Moisture Sensitivity Level – QFN Package</td>
<td>MSL</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

*The maximum package power dissipation must be observed.

2) JESD 51–5 (1S2P Direct–Attach Method) with 0 LFM
3) JESD 51–7 (1S2P Direct–Attach Method) with 0 LFM

*All signals referenced to VSS unless otherwise noted.

Table 5. ELECTRICAL CHARACTERISTICS

Unless otherwise stated: $T_A = T_J = -40^\circ C$ to $140^\circ C$; $VDD = VHB = 12 V$, $VHS = VSS = 0 V$, No load on LO or HO

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{DD}$</td>
<td>VDD quiescent current $V_{LI} = V_{HI} = 0$</td>
<td>0.85</td>
<td>1.6</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_{DDO}$</td>
<td>VDD operating current $f = 500 kHz$, $C_{LOAD} = 0$</td>
<td>5.1</td>
<td>9.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f = 300 kHz$, $C_{LOAD} = 0$</td>
<td>3.5</td>
<td>6.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{HB}$</td>
<td>Boot voltage quiescent current $V_{LI} = V_{HI} = 0 V$</td>
<td>0.65</td>
<td>1.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{HBO}$</td>
<td>Boot voltage operating current $f = 500 kHz$, $C_{LOAD} = 0$</td>
<td>4.8</td>
<td>9.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f = 300 kHz$, $C_{LOAD} = 0$</td>
<td>3.4</td>
<td>6.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{HBS}$</td>
<td>HB to Vss quiescent current $V_{HS} = V_{HB} = 110 V$</td>
<td>8.0</td>
<td>100</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$I_{HBSO}$</td>
<td>HB to Vss operating current $f = 500 kHz$, $C_{LOAD} = 0$</td>
<td>0.2</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>

INPUT

| $V_{HIH}$, $V_{LIH}$ | Input voltage high | 2.0 |     | V    |
| $V_{HIL}$, $V_{LIL}$ | Input voltage low |     | 0.8 |      |
| $R_{IN}$ | Input Pulldown Resistance | 100 | 175 | 350 | kΩ   |

UNDERVOLTAGE PROTECTION (UVLO)

| $V_{DD}$ | VDD rising threshold | 3.4 | 4.4 | 5.4 | V |
| $V_{HDB}$ | VDD Threshold hysteresis |     | 0.4 |     |   |
| $V_{HBB}$ | VHB rising threshold | 3.4 | 4.4 | 5.4 | V |
| $V_{HBS}$ | VHB Threshold hysteresis |     |     | 0.35 | |

BOOTSTRAP DIODE

| $V_F$ | Low–current forward voltage $I_{VDD} – HB = 100 \mu A$ | 0.61 | 0.85 | V |
| $V_{FI}$ | High–current forward voltage $I_{VDD} – HB = 100 mA$ | 0.93 | 1.1 |   |
| $R_D$ | Dynamic resistance, $\Delta V_F/\Delta I$ $I_{VDD} – HB = 100 mA and 80 mA$ | 2.1 | 3.5 | Ω |

LO GATE DRIVER

| $V_{LOL}$ | Low level output voltage $I_{LO} = 100 mA$ | 0.31 | 1.2 | V |
| $V_{LOH}$ | High level output voltage $I_{LO} = -100 mA$, $V_{LOH} = V_{DD} – V_{LO}$ | 0.75 | 1.6 |   |
| Peak Pull–Up Current | $V_{LO} = 0 V$ | 0.55 |     | A |
| Peak Pull–Down Current | $V_{LO} = 12 V$ | 0.8 |     |   |
| $R_{O, \text{Unbiased}}$ | $\text{VCC = VSS}$ | 20k |     | Ω |
Table 5. ELECTRICAL CHARACTERISTICS
Unless otherwise stated: $T_A = T_J = -40^\circ C$ to $140^\circ C$; $VDD = VHB = 12\, V$, $VHS = VSS = 0\, V$, No load on LO or HO

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{HOL}$ Low level output voltage</td>
<td>$I_HO = 100, mA$</td>
<td>0.3</td>
<td>1.2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{H0H}$ High level output voltage</td>
<td>$I_HO = -100, mA, V_{H0H} = V_{HB} - V_{HO}$</td>
<td>0.71</td>
<td>1.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Peak Pull-Up Current</td>
<td>$V_{HO} = 0, V$</td>
<td>0.55</td>
<td>A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Peak Pull-Down Current</td>
<td>$V_{HO} = 12, V$</td>
<td>0.8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_O$, Unbiased</td>
<td>$HB - HS = 0, V$</td>
<td>20k</td>
<td>k</td>
<td>Ω</td>
<td></td>
</tr>
</tbody>
</table>

PROPAGATION DELAYS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{DLFF}$ PWM falling to $V_{LO}$ falling</td>
<td>$C_{LOAD} = 0$</td>
<td>30</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{DHFF}$ PWM falling to $V_{HO}$ falling</td>
<td>$C_{LOAD} = 0$</td>
<td>30</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{DLRR}$ PWM rising to $V_{LO}$ rising</td>
<td>$C_{LOAD} = 0$</td>
<td>44</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{DHRR}$ PWM rising to $V_{HO}$ rising</td>
<td>$C_{LOAD} = 0$</td>
<td>44</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

DEAD–TIME

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fixed Deadtime</td>
<td>Internal Fixed Dead–Time</td>
<td>135</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

DEAD–TIME MATCHING

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{DTM}$ Li OFF, Hi ON</td>
<td></td>
<td>10</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

OUTPUT RISE AND FALL TIME

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_R$ LO, HO</td>
<td>$C_{LOAD} = 1000, pF$</td>
<td>19</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_F$ LO, HO</td>
<td>$C_{LOAD} = 1000, pF$</td>
<td>17</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

MISCELLANEOUS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum input pulse width that changes the output</td>
<td></td>
<td>30</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bootstrap diode turn–off time</td>
<td>$I_F = 20, mA, I_{REV} = 0.5, A$ (Notes 1, 2)</td>
<td>50</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Typical values for $T_A = 25^\circ C$
2. $I_F$: Forward current applied to bootstrap diode, $I_{REV}$: Reverse current applied to bootstrap diode.
NOTE: The NCP81080 has a fixed internal dead-time of 135 ns.
Figure 5. Dead–Time Matching

Figure 6. Propagation Delays
TYPICAL CHARACTERISTICS

Figure 7. Propagation Delays vs. Supply Voltage

Figure 8. Propagation Delays vs. Temperature

Figure 9. Input Thresholds vs. Supply Voltage

Figure 10. Input Thresholds vs. Temperature

Figure 11. Supply Current vs. Frequency

Figure 12. Diode Current vs. Diode Voltage
TYPICAL CHARACTERISTICS

Figure 13. Quiescent Current vs. Supply Voltage

Figure 14. Quiescent Current vs. Supply Voltage

Figure 15. Quiescent Current vs. Supply Voltage

Figure 16. Quiescent Current vs. Supply Voltage
The NCP81080 is a high performance dual MOSFET gate driver optimized to drive half bridge N–Channel MOSFETs. A high and a Low input signals are all that is required to properly drive the power stage. The input signals are independently controlled and monitored by an anti–cross conduction circuit in order to prevent current shoot through. The NCP81080 has UVLO protections for the high–side and low–side drivers forcing the outputs low if the bias supplies drop below the specified UVLO thresholds. The NCP81080 also features an on–chip high voltage bootstrap diode which reduces the external component count. The NCP81080 has a fixed internal dead–time of 135 ns.

Driver Supply Voltage
As a general rule of thumb the local bypass should be 20 times the bootstrap capacitor. It is recommended to use a 4.7 μF bypass capacitor on VDD to VSS. The bootstrap capacitor is recharged on a cycle by cycle basis through the bootstrap diode from the VDD bypass capacitor. The charging cycle involves bursts in peak currents that require careful considerations by keeping a tight layout and short loops to avoid reliability issues.

If for any reason the application requires the VDD voltage to discharge to ground at rapid rates (3 + V/μs) the user is required to add an external diode between the supply voltage and the bypass capacitor.

High–Side Driver
The high side driver is designed to drive a floating low RDS\textsubscript{ON} N–channel MOSFET. The output resistances for the driver are 7.1 ohms for sourcing and 3.1 ohms for sinking gate current. The bias to the high side driver is externally connected to the VDD and VSS. When the driver is enabled, the driver’s output is in phase with HI. When the NCP81080 is disabled, the high side gate is held low.

UVLO (Under Voltage Lockout)
The bias supplies of the high–side and low–side drivers have UVLO protection. The VDD UVLO disables both drivers when the VDD voltage crosses the specified threshold. The typical rising threshold is 4.4 V with 0.4 V hysteresis. The VHB UVLO disables only the high–side driver when the VHB to VHS is below the specified
threshold. The typical VHB UVLO rising threshold is 4.4 V with 0.35 V hysteresis.

At power up, when the supply voltage ramps up to set VDD and crosses the UVLO thresholds, users must take into account a 20 µs delay before the output drivers can react to a logic input. The 20 µs delay applies to both High-side and Low-side drivers. Figure 4 only shows the delay for the low-side channel.

**Input Stage**

The input stage of the NCP81080 is TTL compatible. The logic rising threshold level is 2.0 V and the logic falling threshold is 0.8 V.

**Cross-Conduction Protection**

The NCP81080’s inputs HI & LI are controlled independently. In order to prevent the power stage MOSFETs from turning on at the same time an internal logic circuit is implemented to monitor the state of HI & LI. If both input signals are high at the same time, the output signals HO & LO are forced low. (See Timing Diagram)

**UVLO Crossing**

When VDD & VHB cross their respective UVLO thresholds if HI and LI were already set the NCP81080 will keep HO pulled Low until it detects a rising edge on HI, however LO will follow LI allowing the Low-Side FET to turn on. (Refer to Figure 4)

**Layout Guidelines**

Gate drivers experience high di/dt during the switching transitions. So, the inductance at the gate drive traces must be minimized to avoid excessive ringing on the switch node. Gate drive traces should be kept as short and wide (>20 mil) as practical. The input capacitor must be placed as close as possible to the IC. Connect the VSS pin of the NCP81080 as close as possible to the source of the lower MOSFET. The use of vias is highly desirable to maximize thermal conduction away from driver.
For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**NOTES:**
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

**RECOMMENDED SOLDERING FOOTPRINT**

**DIMENSIONS: MILLIMETERS**

- **MIN**
  - A: 0.50
  - B: 0.24
  - D: 2.00
  - E: 0.25
  - e: 0.50
  - K: 0.25
  - L: 0.30
  - L1: 0.10
- **MAX**
  - A: 0.80
  - A1: 0.00
  - A3: 0.05
  - B: 0.30
  - D: 2.00
  - E: 0.50
  - 8X: 0.50
  - L: 0.35

**NOTES:**
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4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

**FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.**
MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

SOIC–8 NB
CASE 751–07
ISSUE AK

DATE 16 FEB 2011

NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

SCALE 1:1

SOLDERING FOOTPRINT*

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2
SOIC–8 NB
CASE 751–07
ISSUE AK

DATE 16 FEB 2011

STYLe 1:
PIN 1. EMITTER
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. GATE
7. SOURCE
8. SOURCE

STYLe 2:
PIN 1. COLLECTOR, DIE #1
2. N–GATE
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLe 3:
PIN 1. DRAIN, DIE #1
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLe 4:
PIN 1. ANODE
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. ANODE
8. COMMON CATHODE

STYLe 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. SOURCE
6. GATE
7. SOURCE
8. SOURCE

STYLe 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLe 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLe 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. ANODE
8. COMMON CATHODE

STYLe 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLe 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLe 11:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. SOURCE
5. GATE
6. DRAIN
7. DRAIN
8. DRAIN

STYLe 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. SOURCE
5. GATE
6. DRAIN
7. DRAIN
8. DRAIN

STYLe 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. SOURCE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLe 14:
PIN 1. N–SOURCE
2. N–GATE
3. P–SOURCE
4. P–GATE
5. P–DRAIN
6. P–DRAIN
7. N–DRAIN
8. N–DRAIN

STYLe 15:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. SOURCE
5. SOURCE
6. SOURCE
7. SOURCE
8. SOURCE

STYLe 16:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. SOURCE
5. SOURCE
6. SOURCE
7. SOURCE
8. SOURCE

STYLe 17:
PIN 1. VCC
2. V2OUT
3. VOUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLe 18:
PIN 1. LINE 1 IN
2. LINE 1 IN
3. LINE 1 IN
4. LINE 1 IN
5. LINE 2 IN
6. LINE 3 IN
7. LINE 4 IN
8. LINE 5 IN

STYLe 19:
PIN 1. LINE 1 OUT
2. LINE 1 OUT
3. LINE 1 OUT
4. LINE 1 OUT
5. LINE 2 OUT
6. LINE 3 OUT
7. LINE 4 OUT
8. LINE 5 OUT

STYLe 20:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLe 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLe 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. COMMON ANODE/GND
8. COMMON ANODE/GND

STYLe 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. COMMON ANODE/GND

STYLe 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. COLLECTOR
5. COLLECTOR
6. COLLECTOR
7. COLLECTOR
8. COLLECTOR

STYLe 25:
PIN 1. VIN
2. N/C
3. RXE
4. GND
5. IOU
6. IOU
7. IOU
8. IOU

STYLe 26:
PIN 1. GND
2. GND
3. GND
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. GND

STYLe 27:
PIN 1. ILIMIT
2. GND
3. GND
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. GND

STYLe 28:
PIN 1. SW_TO_GND
2. GND
3. GND
4. V_MON
5. V_BULK
6. V_BULK
7. V_BULK
8. GND

STYLe 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLe 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

STYLe 31:
PIN 1. Input 1
2. Input 1
3. Input 1
4. Input 1
5. Input 1
6. Input 1
7. Input 1
8. Input 1

STYLe 32:
PIN 1. Output 1
2. Output 1
3. Output 1
4. Output 1
5. Output 1
6. Output 1
7. Output 1
8. Output 1

STYLe 33:
PIN 1. OVLO
2. OVLO
3. OVLO
4. OVLO
5. OVLO
6. OVLO
7. OVLO
8. OVLO

STYLe 34:
PIN 1. GND
2. GND
3. GND
4. GND
5. GND
6. GND
7. GND
8. GND

STYLe 35:
PIN 1. Source
2. Source
3. Source
4. Source
5. Source
6. Source
7. Source
8. Source

STYLe 36:
PIN 1. Collector
2. Collector
3. Collector
4. Collector
5. Collector
6. Collector
7. Collector
8. Collector

STYLe 37:
PIN 1. Emitter
2. Emitter
3. Emitter
4. Emitter
5. Emitter
6. Emitter
7. Emitter
8. Emitter

STYLe 38:
PIN 1. Drain
2. Drain
3. Drain
4. Drain
5. Drain
6. Drain
7. Drain
8. Drain

STYLe 39:
PIN 1. Gate
2. Gate
3. Gate
4. Gate
5. Gate
6. Gate
7. Gate
8. Gate

STYLe 40:
PIN 1. Base
2. Base
3. Base
4. Base
5. Base
6. Base
7. Base
8. Base

STYLe 41:
PIN 1. Collector
2. Collector
3. Collector
4. Collector
5. Collector
6. Collector
7. Collector
8. Collector

STYLe 42:
PIN 1. Source
2. Source
3. Source
4. Source
5. Source
6. Source
7. Source
8. Source

STYLe 43:
PIN 1. Emitter
2. Emitter
3. Emitter
4. Emitter
5. Emitter
6. Emitter
7. Emitter
8. Emitter

STYLe 44:
PIN 1. Drain
2. Drain
3. Drain
4. Drain
5. Drain
6. Drain
7. Drain
8. Drain

STYLe 45:
PIN 1. Gate
2. Gate
3. Gate
4. Gate
5. Gate
6. Gate
7. Gate
8. Gate

STYLe 46:
PIN 1. Base
2. Base
3. Base
4. Base
5. Base
6. Base
7. Base
8. Base

STYLe 47:
PIN 1. Collector
2. Collector
3. Collector
4. Collector
5. Collector
6. Collector
7. Collector
8. Collector

STYLe 48:
PIN 1. Source
2. Source
3. Source
4. Source
5. Source
6. Source
7. Source
8. Source

STYLe 49:
PIN 1. Emitter
2. Emitter
3. Emitter
4. Emitter
5. Emitter
6. Emitter
7. Emitter
8. Emitter

STYLe 50:
PIN 1. Drain
2. Drain
3. Drain
4. Drain
5. Drain
6. Drain
7. Drain
8. Drain

STYLe 51:
PIN 1. Gate
2. Gate
3. Gate
4. Gate
5. Gate
6. Gate
7. Gate
8. Gate

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