NCP6922C

4 Channels PMIC, 2 x DC-to-DC Converters, 2 x LDOs

The NCP6922C integrated circuit is part of the ON Semiconductor mini power management IC family (PMIC). It is optimized to supply battery powered portable application sub−systems such as camera function, microprocessors. This device integrates 2 high efficiency 800 mA Step−down DC−to−DC converters with DVS (Dynamic Voltage Scale) and 2 low dropout (LDO) voltage regulators in a 4x4 mm WQFN package.

Features

- 2 DC−to−DC Converters (3 MHz, 1 μH / 10 μF, 800 mA)
  - Peak Efficiency 95%
  - Programmable Output Voltage from 0.6 V to 3.3 V by 12.5 mV Steps
- 2 Low Noise − Low Drop Out Regulators (2.2 μF, 150 mA)
  - Programmable Output Voltage from 1.0 V to 3.3 V by 50 mV Steps
  - 50 μVrms Typical Low Output Noise
- Control
  - 400 kHz / 3.4 MHz I^2C Compatible
  - Independent Enable Pins, I^2C Enable Control Bits
  - Power Good Output Pin
  - Customizable Power Up Sequence
- Extended Input Voltage Range from 2.3 V to 5.5 V
- 82 μA Low Quiescent Current at No Load
- Less than 7 μA Sleep Mode Current
- Footprint: 4.0 x 4.0 mm WQFN 0.5 mm Pitch
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Cellular Phones, Tablets
- Digital Cameras

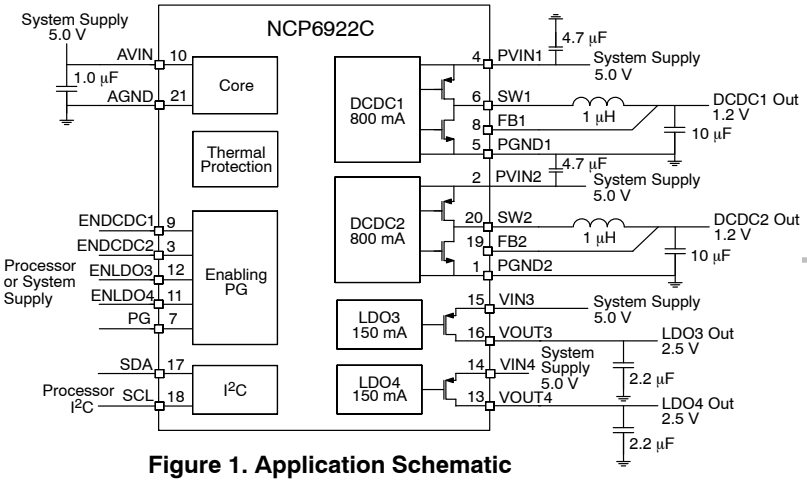


Figure 1. Application Schematic

ON Semiconductor®

http://onsemi.com

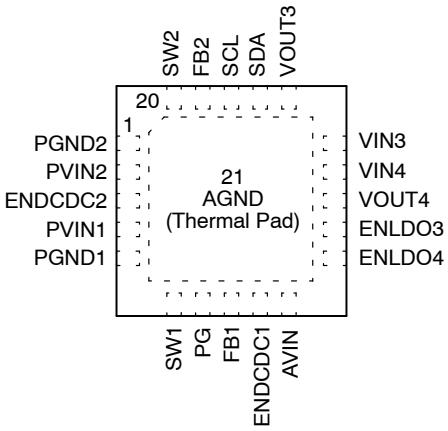
MARKING DIAGRAM

WQFN20
CASE 510AV

xxxxxx = 22CB2: NCP6922CB prototype
= 22CC2: NCP6922CC prototype
= 6922CB: NCP6922CB
= 6922CC: NCP6922CC
= 6922CD: NCP6922CD
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.)

PIN OUT



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information page 40 of this data sheet.

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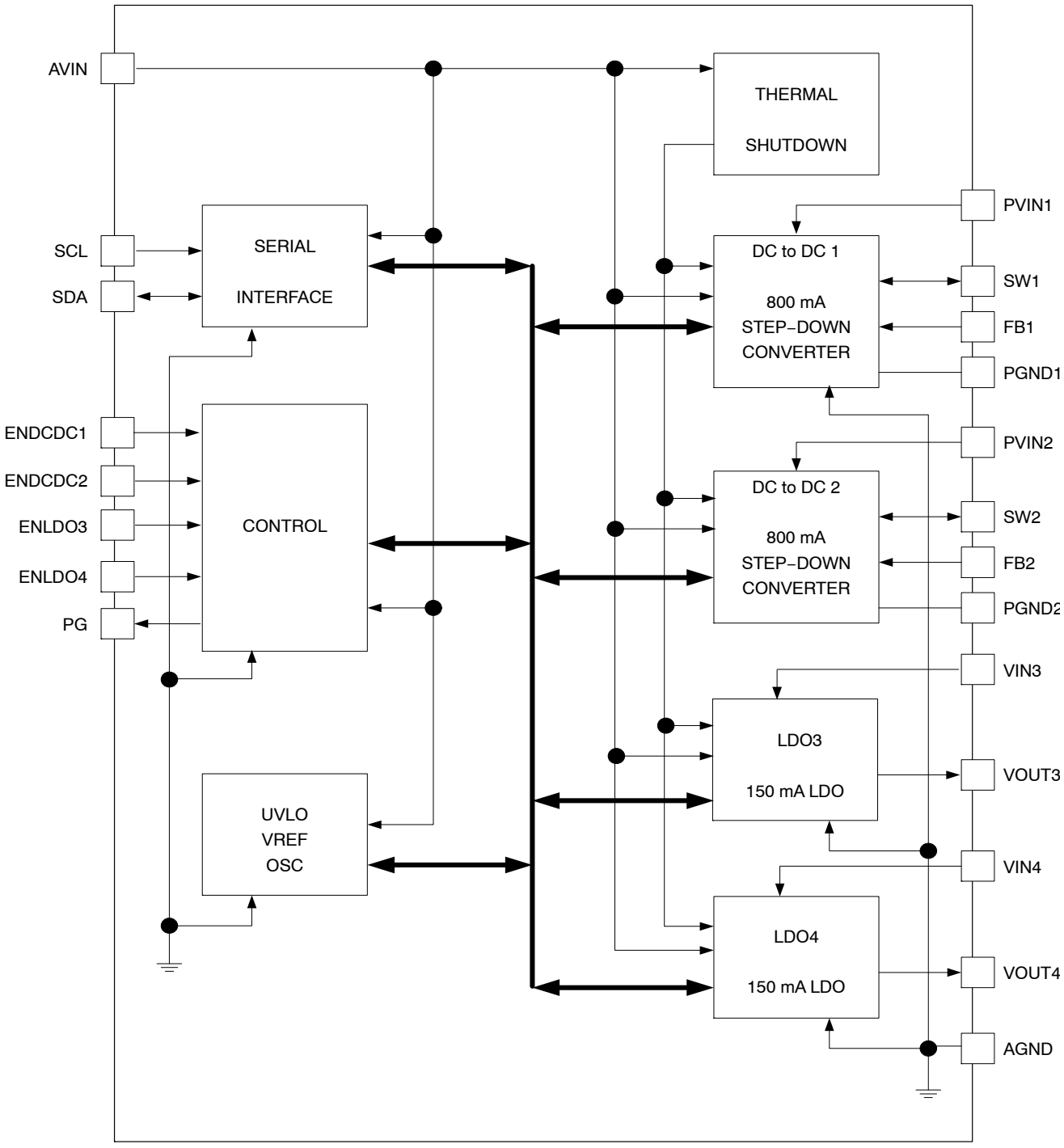


Figure 2. Functional Block Diagram

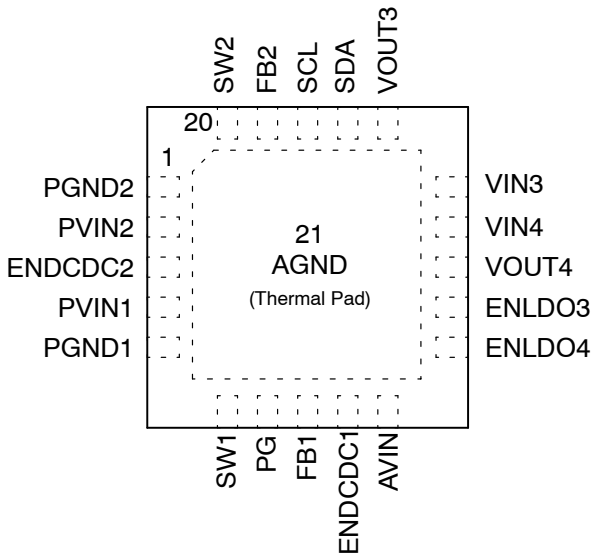


Figure 3. Pin Out (Top View)

Table 1. PIN FUNCTION DESCRIPTION

Pin	Name	Type	Description
SUPPLY			
10	AVIN	Analog Input	Analog Supply. This pin is the device analog and digital supply. A 1.0 μF ceramic capacitor or larger must bypass this input to ground. This capacitor should be placed as close as possible to this pin.
21	AGND	Analog Ground	Analog Ground. Analog and digital modules ground. Must be connected to the system ground.
I/O			
9	ENDCDC1	Digital Input	DCDC1 Enable, high level will enable DCDC1; there is internal pull down resistor on this pin.
3	ENDCDC2	Digital Input	DCDC2 Enable, high level will enable DCDC2; there is internal pull down resistor on this pin.
12	ENLDO3	Digital Input	LDO3 Enable, high level will enable LDO 3; there is internal pull down resistor on this pin.
11	ENLDO4	Digital Input	LDO4 Enable, high level will enable LDO 4; there is internal pull down resistor on this pin.
18	SCL	Digital Input	I^2C interface Clock
17	SDA	Digital Input	I^2C interface Data
7	PG	Digital Output	Power Good open drain output.
DC−DC CONVERTERS			
4	PVIN1	Power Input	DCDC1 Power Supply. This pin must be decoupled to ground by a 4.7 μF ceramic capacitor. This capacitor should be placed as close a possible to this pin.
6	SW1	Power Output	DCDC1 Switch Power. This pin connects the power transistors to one end of the inductor. Typical application uses 1.0 μH inductor; refer to application section for more information.
8	FB1	Analog Input	DCDC1 Feedback Voltage. This pin is the input to the error amplifier and must be connected to the output capacitor.
5	PGND1	Power Ground	DCDC1 Power Ground. This pin is the power ground and carries the high switching current. A high quality ground must be provided to prevent noise spikes. A local ground plane is recommended to avoid high−density current flow in a limited PCB track.
2	PVIN2	Power Input	DCDC2 Power Supply. This pin must be decoupled to ground by a 4.7 μF ceramic capacitor. This capacitor should be placed as close a possible to this pin.
20	SW2	Power Output	DCDC2 Switch Power. This pin connects the power transistors to one end of the inductor. Typical application uses 1.0 μH inductor; refer to application section for more information.
19	FB2	Analog Input	DCDC2 Feedback Voltage. This pin is the input to the error amplifier and must be connected to the output capacitor.
1	PGND2	Power Ground	DCDC2 Power Ground. This pin is the power ground and carries the high switching current. A high quality ground must be provided to prevent noise spikes. A local ground plane is recommended to avoid high−density current flow in a limited PCB track.
LDO REGULATORS			
15	VIN3	Power Input	LDO3 Power Supply

Table 1. PIN FUNCTION DESCRIPTION

Pin	Name	Type	Description
LDO REGULATORS			
16	VOUT3	Power Output	LDO3 Output Power. This pin requires a 2.2 μF decoupling capacitor.
14	VIN4	Power Input	LDO4 Power Supply
13	VOUT4	Power Output	LDO4 Output Power. This pin requires a 2.2 μF decoupling capacitor.

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Analog and power pins: AVIN, PVIN1, SW1, PVIN2, SW2, VIN3, VIN4, VOUT3, VOUT4, PG, FB1, FB2	V_A	−0.3 to + 6.0	V
Digital pins: SCL, SDA, ENDCDC1,ENDCDC2, ENLDO3, ENLDO4: Input Voltage Input Current	 VDG IDG	 −0.3 to VA +0.3 ≤ 6.0 10	 V mA
Human Body Model (HBM) ESD Rating are (Note 1)	ESD HBM	2000	V
Charged Device Model (CDM) ESD Rating are (Note 1)	ESD CDM	750	V
Latch up Current: (Note 2) Digital pins All other pins	ILU	±10 ±100	mA
Storage Temperature Range	TSTG	−65 to + 150	°C
Maximum Junction Temperature	TJMAX	−40 to +150	°C
Moisture Sensitivity (Note 3)	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AV_{IN} PV_{IN}	Analog and Power Supply	(Note 12)	2.3	–	5.5	V
LDO_{VIN}	LDO Input Voltage range		1.7	–	5.5	V
T_A	Ambient Temperature Range		−40	25	+85	°C
T_J	Junction Temperature Range (Note 5)		−40	25	+125	°C
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 6)	WQFN−20 on Demo−board	–	40	–	°C/W
P_D	Power Dissipation Rating (Note 7)	$T_A \le 85°C$	–	1000	–	mW
P_D	Power Dissipation Rating (Note 7)	$T_A = 40°C$	–	2125	–	mW
L	Inductor for DC−to−DC converters (Note 4)		0.47	1	2.2	μH
Co	Output Capacitor for DC−to−DC Converters (Note 4)		–	10	–	μF
	Output Capacitors for LDO (Note 4)		1.2	2.2	–	μF
Cin	Input Capacitor for DC−to−DC Converters (Note 4)		–	4.7	–	μF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114,
   Charged Device Model (CDM) ±750 V per JEDEC standard: JESD22−C101.
2. Latch up Current per JEDEC standard: JESD78 class II.
3. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.
4. Refer to the Application Information section of this data sheet for more details.
5. The thermal shutdown set to 150°C (typical) avoids potential irreversible damage on the device due to power dissipation.
6. The $R_{\theta JA}$ is dependent of the PCB heat dissipation. Board used to drive this data was a 2″ x 2″ NCP6922CEVB board. It is a multilayer board with 1−once internal power and ground planes and 2−once copper traces on top and bottom of the board.
7. The maximum power dissipation (P_D) is dependent by input voltage, maximum output current and external components selected.

$$R_{\theta JA} = \frac{125 - T_A}{P_D}$$

Table 4. ELECTRICAL CHARACTERISTICS (Min and Max limits apply for T_A = −40°C to +85°C, AV_{IN} = PV_{IN1} = PV_{IN2} = V_{IN3} = V_{IN4} = 5.0 V and default configuration, unless otherwise specified. Typical values are referenced to T_A = + 25°C, AV_{IN} = PV_{IN1} = PV_{IN2} = V_{IN3} = V_{IN4} = 5.0 V and default configuration) (Note 9).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY CURRENT: PINS AVIN – PVIN1 – PVIN2						
I_Q	Operating Quiescent Current	DCDCs & LDO4 Off LDO3 on – no load	–	17	30	μA
		DCDC1 on – no load – PFM DCDC2 & LDOs off	–	36	70	
		DCDCs on – no load – PFM LDOs on – no load	–	82	150	
I_{SLEEP}	Sleep Mode Current	All DCDC and LDOs off	–	7	15	μA
DCDC1&2 STEP DOWN CONVERTERS						
$PV_{IN1,2}$	Input Voltage Range	V_{OUT} ≤ 2.1 V (Note 11)	2.3	5.0	5.5	V
		V_{OUT} > 2.1 V	V_{OUT}+0.2V	5.0	5.5	
I_{OUTMAX}	Maximum Output Current		0.8	–	–	A
ΔV_{OUT}	Output Voltage DC Error	Forced PWM mode, V_{IN} range, I_{OUT} from 0 mA and 100 mA	−1	–	1	%
		Forced PWM mode, VIN range, IOUT up to I_{OUTMAX} (Note 10)	−1	–	1	
		Auto mode, V_{IN} range, I_{OUT} up to I_{OUTMAX} (Note 10)	−1	–	2	
F_{SW}	Switching Frequency	Forced PWM	2.7	3	3.3	MHz
R_{ONHS}	P−Channel MOSFET On Resistance	From PVIN1 / PVIN2 pins to SW1 / SW2 pins	–	270	400	mΩ
R_{ONLS}	N−Channel MOSFET On Resistance	From SW1 / SW2 pins to PGND1 / PGND2 pins	–	190	300	mΩ
I_{PK}	Peak Inductor Current	Open loop	1.0	1.3	1.6	A
DC_{LOAD}	Load Regulation	I_{OUT} from 100 mA to I_{OUTMAX}	–	5	–	mV/A
DC_{LINE}	Line Regulation	PV_{IN} = PV_{INMIN} to 5.0 V, I_{OUT} = 100 mA	–	0.5	–	%
D	Maximum Duty Cycle		–	100	–	%
t_{START}	Soft−Start Time	Time from I^2C command ACK to 90% of Output Voltage	–	–	0.6	ms
$R_{DISDCDC}$	DCDC Active Output Discharge		–	7	–	Ω
LDO3 and LDO4						
V_{IN3}, V_{IN4}	LDO3 and LDO4 Input Voltage	V_{OUT} <= 1.5 V, I_{OUT} = 150 mA	1.7	–	5.5	V
		V_{OUT} > 1.5 V, I_{OUT} = 150 mA	Vout+V_{DROP}	–	5.5	V
I_{OUT}	Maximum Output Current		150	–	–	mA
I_{SC}	Short Circuit Protection (foldback)	V_{IN} = 3.6 V	–	70	–	mA
I_{LIMIT}	Current Limit	V_{IN} = 3.6 V	200	–	500	
ΔV_{OUT}	Output Voltage Accuracy	I_{OUT} = 75 mA	−1	V_{NOM}	+1	%
		V_{IN} range, I_{OUT} = 0 mA and 150 mA (Note 10)	−2	V_{NOM}	+2	
DC_{LOAD}	Load Regulation	I_{OUT} = 0 mA to 150 mA	–	0.5	–	%
DC_{LINE}	Line Regulation	V_{IN} = V_{INMIN} to 5.5 V, I_{OUT} = 150 mA	–	0.5	–	%

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Devices that use non−standard supply voltages which do not conform to the intent I^2C bus system levels must relate their input levels to the V_{DD} voltage to which the pull−up resistors R_P are connected.
9. Refer to the Application Information section of this data sheet for more details.
10. Guaranteed by design and characterized.
11. Operation above 5.5 V input voltage for extended periods may affect device reliability.

Table 4. ELECTRICAL CHARACTERISTICS (Min and Max limits apply for T_A = −40°C to +85°C, AV_{IN} = PV_{IN1} = PV_{IN2} = V_{IN3} = V_{IN4} = 5.0 V and default configuration, unless otherwise specified. Typical values are referenced to T_A = + 25°C, AV_{IN} = PV_{IN1} = PV_{IN2} = V_{IN3} = V_{IN4} = 5.0 V and default configuration) (Note 9).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LDO3 and LDO4						
V_{DROP}	Dropout Voltage	V_{OUT} = V_{NOM} − 2%, I_{OUT} = 150 mA	–	95	180	mV
		V_{OUT} = 1.15 V, I_{OUT} = 150 mA (Driven by V_{INMIN})		550	–	mV
PSRR	Ripple Rejection	F = 1 kHz, I_{OUT} 75% max load, V_{OUT}=1.8 V	–	−65	–	dB
		F = 10 kHz I_{OUT} 75% max load, V_{OUT}=1.8 V	–	−55	–	
Noise		10 Hz → 100 kHz, $V_{OUT3,4}$ = 1.8 V	–	55	–	μV
$R_{DISLDO3,4}$	LDO Active Output Discharge		–	20	–	Ω
ENx						
V_{IH}	High input voltage		1.1	–	–	V
V_{IL}	Low input voltage		–	–	0.4	V
t_{EN}	Enable Filter	Enable pins rising / falling (Note 10)	4	–	18	μs
I_{PD}	Enable Pins Pull−Down (input bias current)		–	0.1	1.0	uA
POWER GOOD						
V_{PGL}	Power Good Low Threshold	Falling edge as a percentage of nominal output voltage	86	90 of V_{NOM}	95	%
V_{PGHYS}	Power Good detection level		0.2	3	5	%
t_{RT}	Power Good Reaction Time	Falling (Note 10) Rising (Note 10)	– 3	3 –	– 14	μs
V_{PGL}	Power Good low output voltage	I_{PG} = 5 mA	–	–	0.2	V
PG_{LK}	Power Good leakage current	3.6V at PG pin when power good valid	–	–	100	nA
V_{PGH}	Power Good high output voltage	Open drain	–	–	5.5	V
I^2C						
V_{I2CINT}	High level at SCL/SDA line		–	–	5.5	V
V_{I2CIL}	SCL, SDA low input voltage	SCL, SDA pin (Note 9 and 10)	–	–	0.5	V
V_{I2CIH}	SCL, SDA high input voltage	SCL, SDA pin (Note 9 and 10)	0.8xV_{I2CINT}	–	–	V
V_{I2COL}	SCL, SDA low output voltage	I_{SINK} = 3 mA (Note10)	–	–	0.4	V
F_{SCL}	I^2C clock frequency	(Note 10)	–	–	3.4	MHz
TOTAL DEVICE						
V_{UVLO}	Under Voltage Lockout	V_{IN} falling	–	–	2.3	V
V_{UVLOH}	Under Voltage Lockout Hysteresis	V_{IN} rising	60	–	200	mV
T_{SD}	Thermal Shut Down Protection			150		°C
$T_{WARNING}$	Warning Rising Edge			135		°C
T_{SDHYS}	Thermal Shut Down Hysteresis			35		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Devices that use non−standard supply voltages which do not conform to the intent I^2C bus system levels must relate their input levels to the V_{DD} voltage to which the pull−up resistors R_P are connected.
9. Refer to the Application Information section of this data sheet for more details.
10. Guaranteed by design and characterized.
11. Operation above 5.5 V input voltage for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS

(AV_{IN} = PV_{IN1} = PV_{IN2} = V_{IN3} = V_{IN4} = 5.0 V (Unless otherwise noted). T_A = +25°C, DCDC1 = 1.20 V, DCDC2 = 3.30 V, LDO3 = 1.15 V LDO4 = 2.5 V, C_{LDO} = 2.2 μF 0603, L_{DCDC} = 1.0 μF (SPM3012−1R0M) − C_{DCDC} = 10 μF 0603)

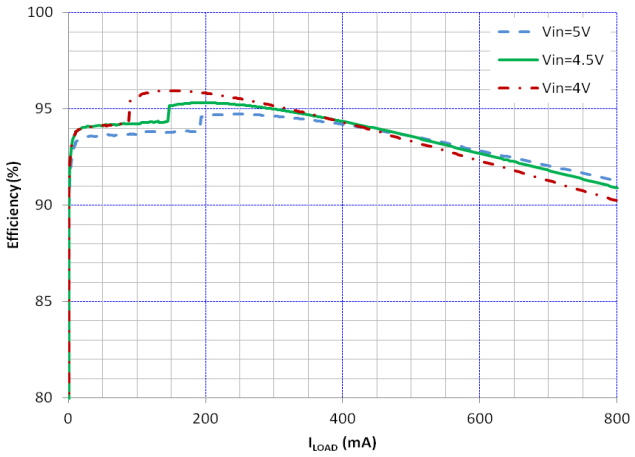


Figure 4. Efficiency vs I_{LOAD} and V_{IN} V_{OUT} = 3.30 V, SPM6530 Inductor

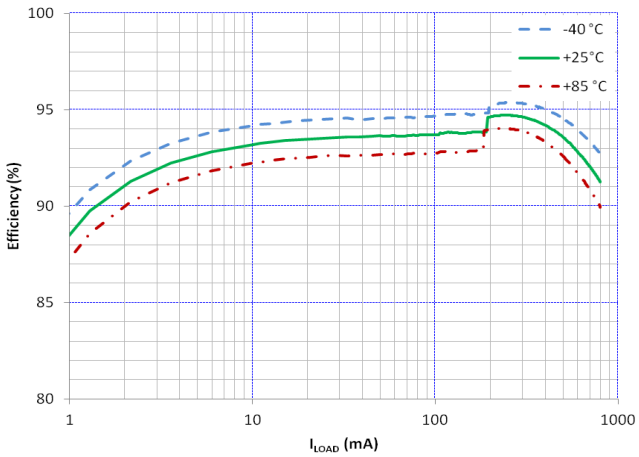


Figure 5. Efficiency vs I_{LOAD} and Temperature V_{OUT} = 3.30 V, SPM6530 Inductor

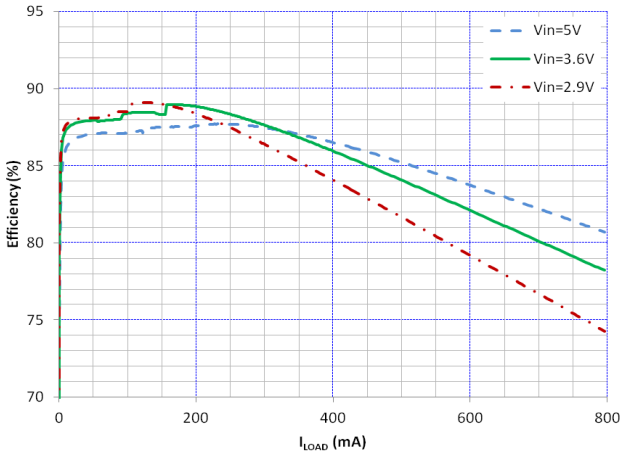


Figure 6. Efficiency vs I_{LOAD} and V_{IN} V_{OUT} = 1.20 V, SPM6530 Inductor

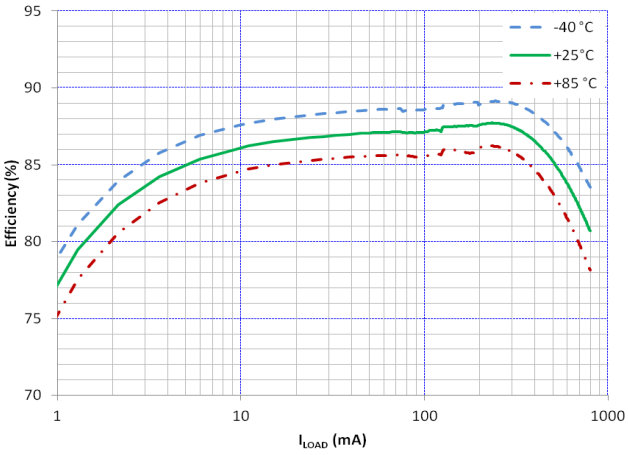


Figure 7. Efficiency vs I_{LOAD} and Temperature V_{OUT} = 1.20 V, SPM6530 Inductor

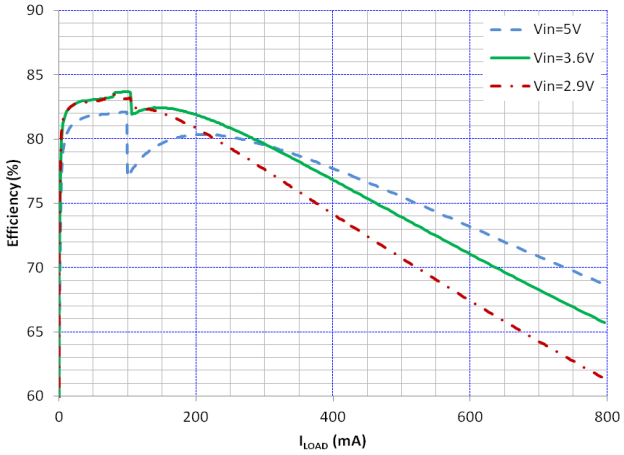


Figure 8. Efficiency vs I_{LOAD} and V_{IN} V_{OUT} = 0.60 V, SPM6530 Inductor

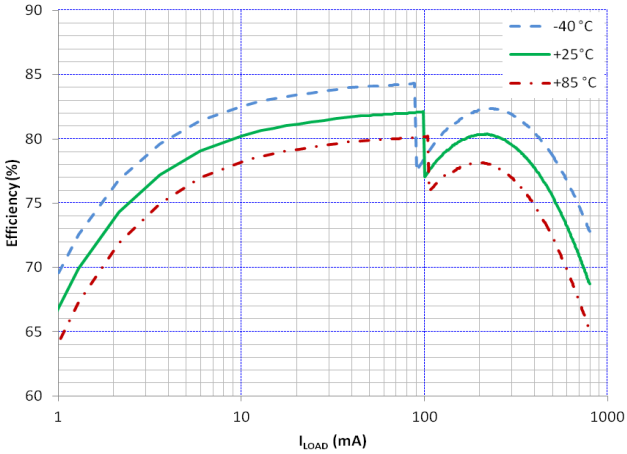


Figure 9. Efficiency vs I_{LOAD} and Temperature V_{OUT} = 0.60 V, SPM6530 Inductor

TYPICAL CHARACTERISTICS

(AV_{IN} = PV_{IN1} = PV_{IN2} = V_{IN3} = V_{IN4} = 5.0 V (Unless otherwise noted). T_A = +25°C, DCDC1 = 1.20 V, DCDC2 = 3.30 V, LDO3 = 1.15 V LDO4 = 2.5 V, C_{LDO} = 2.2 μF 0603, L_{DCDC} = 1.0 μF (SPM3012−1R0M) − C_{DCDC} = 10 μF 0603)

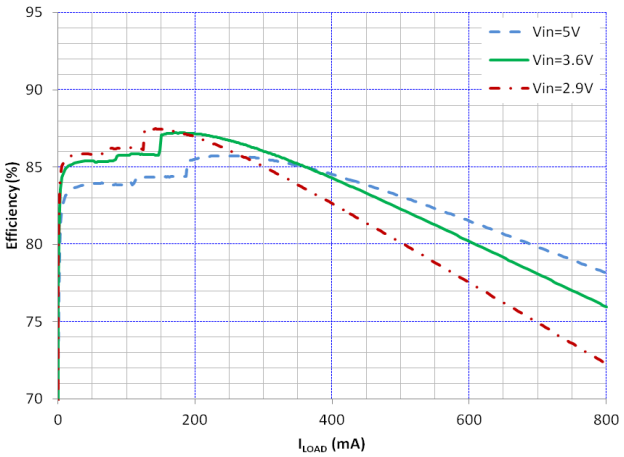


Figure 10. Efficiency vs I_{LOAD} and V_{IN} DCDC1, V_{OUT} = 1.20 V, SPM3012 Inductor

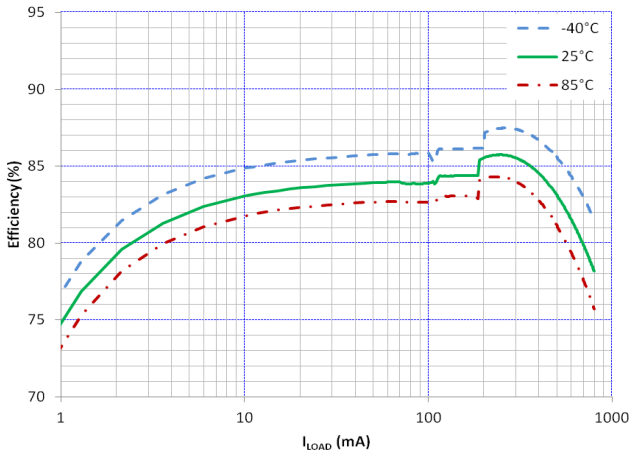


Figure 11. Efficiency vs I_{LOAD} and Temperature DCDC1, V_{OUT} = 1.20 V, SPM3012 Inductor

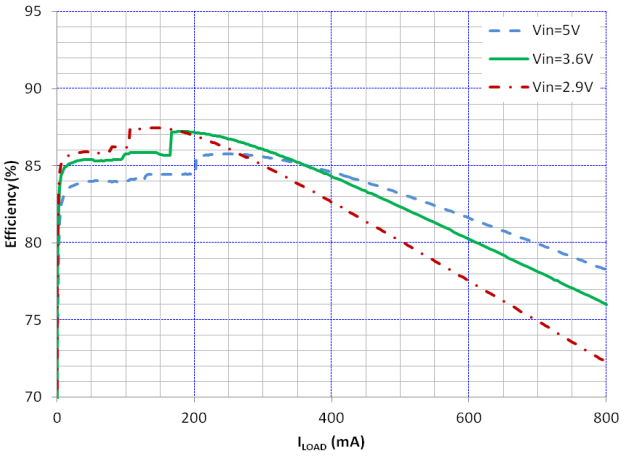


Figure 12. Efficiency vs I_{LOAD} and V_{IN} DCDC2 − V_{OUT} = 1.20 V, SPM3012 Inductor

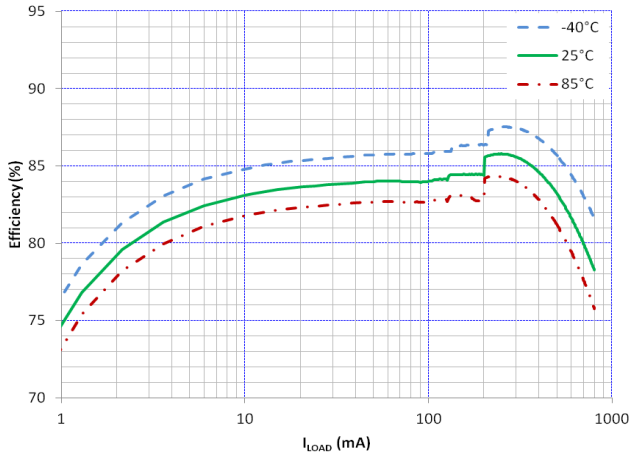


Figure 13. Efficiency vs I_{LOAD} and Temperature DCDC2, V_{OUT} = 1.20 V, SPM3012 Inductor

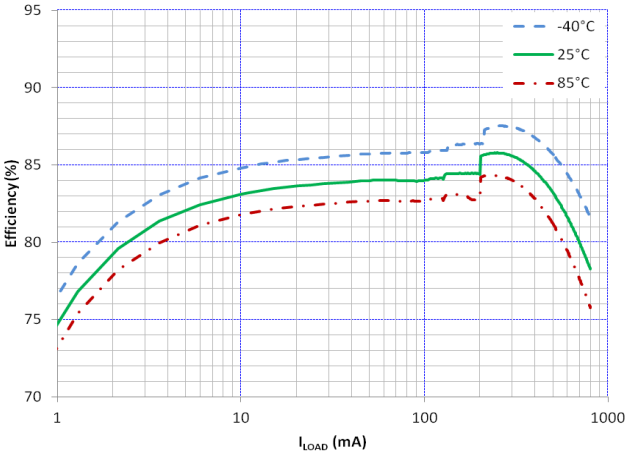


Figure 14. Efficiency vs I_{LOAD} and V_{IN} DCDC2 − V_{OUT} = 3.30 V, SPM3012 Inductor

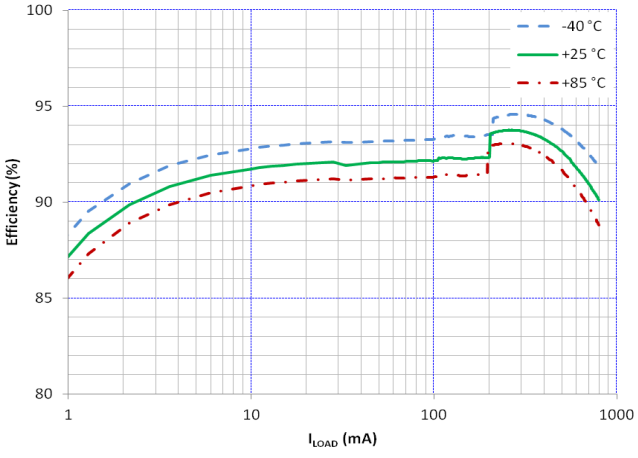


Figure 15. Efficiency vs I_{LOAD} and Temperature DCDC2, V_{OUT} = 3.30 V, SPM3012 Inductor

TYPICAL CHARACTERISTICS

(AV_{IN} = PV_{IN1} = PV_{IN2} = V_{IN3} = V_{IN4} = 5.0 V (Unless otherwise noted). T_A = +25°C, DCDC1 = 1.20 V, DCDC2 = 3.30 V, LDO3 = 1.15 V LDO4 = 2.5 V, C_{LDO} = 2.2 μF 0603, L_{DCDC} = 1.0 μF (SPM3012−1R0M) − C_{DCDC} = 10 μF 0603)

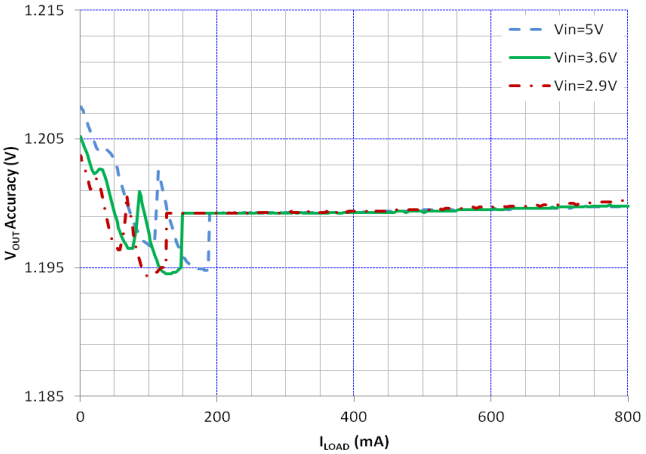


Figure 16. V_{OUT} accuracy (mV) vs I_{LOAD} and V_{IN} DCDC1, V_{OUT} = 1.20 V

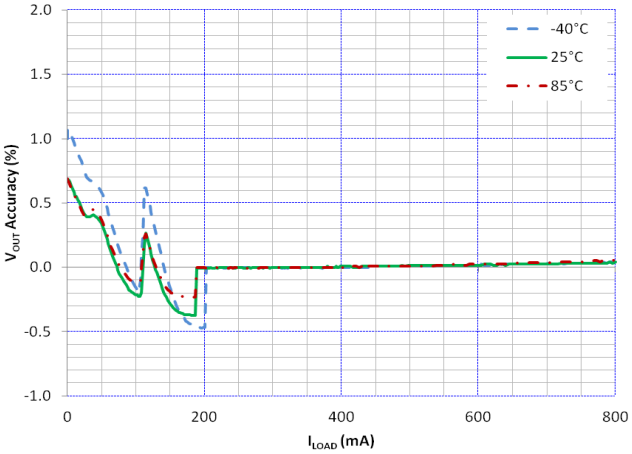


Figure 17. V_{OUT} accuracy (%) vs I_{LOAD} and Temperature DCDC1, V_{OUT} = 1.20 V

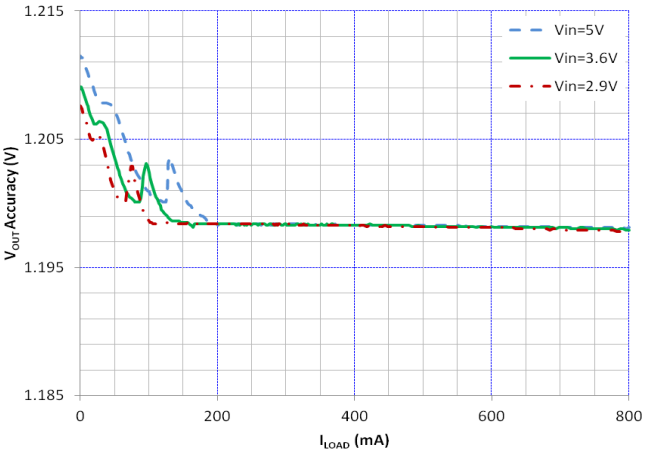


Figure 18. V_{OUT} accuracy (mV) vs I_{LOAD} and V_{IN} DCDC2, V_{OUT} = 1.20 V

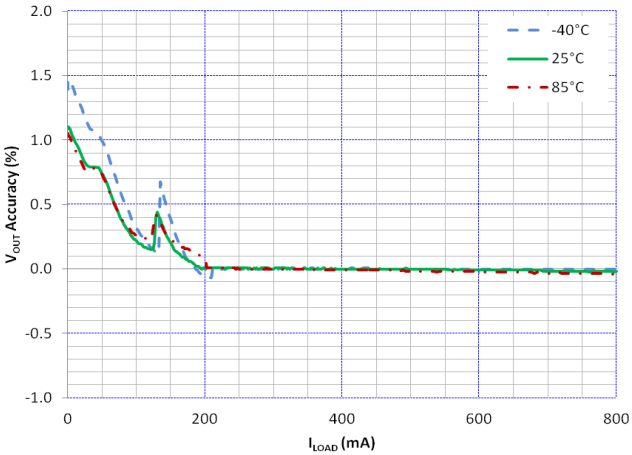


Figure 19. V_{OUT} accuracy (%) vs I_{LOAD} and Temperature DCDC1, V_{OUT} = 1.20 V

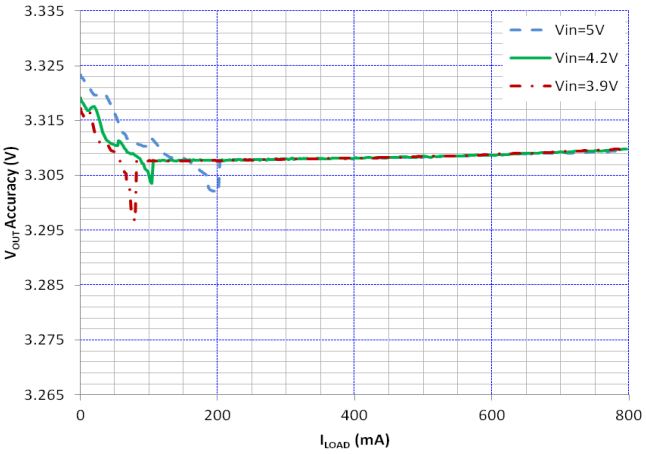


Figure 20. V_{OUT} accuracy (mV) vs I_{LOAD} and V_{IN} DCDC2, V_{OUT} = 3.30 V

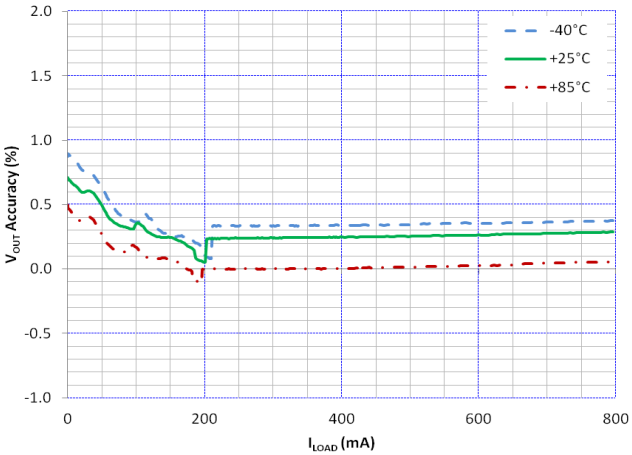


Figure 21. V_{OUT} accuracy (%) vs I_{LOAD} and Temperature DCDC2, V_{OUT} = 3.30 V

TYPICAL CHARACTERISTICS

(AV_{IN} = PV_{IN1} = PV_{IN2} = V_{IN3} = V_{IN4} = 5.0 V (Unless otherwise noted). T_A = +25°C, DCDC1 = 1.20 V, DCDC2 = 3.30 V, LDO3 = 1.15 V LDO4 = 2.5 V, C_{LDO} = 2.2 μF 0603, L_{DCDC} = 1.0 μF (SPM3012−1R0M) − C_{DCDC} = 10 μF 0603)

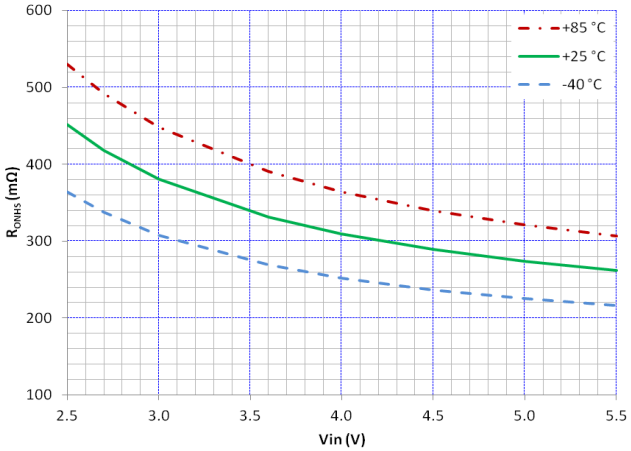


Figure 22. DCDC1 HSS R_{ON} vs V_{IN} and Temperature

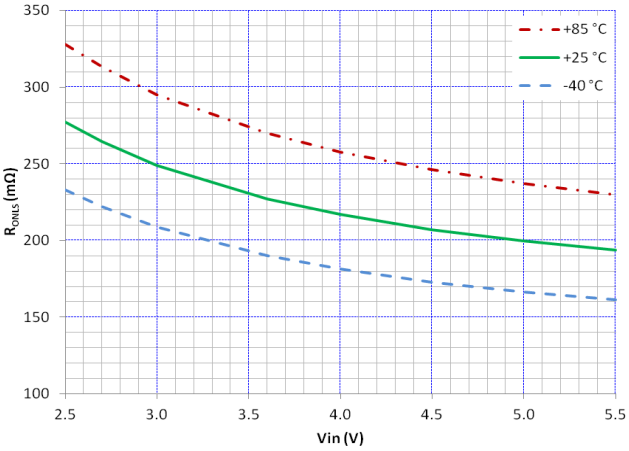


Figure 23. DCDC1 LSS R_{ON} vs V_{IN} and Temperature

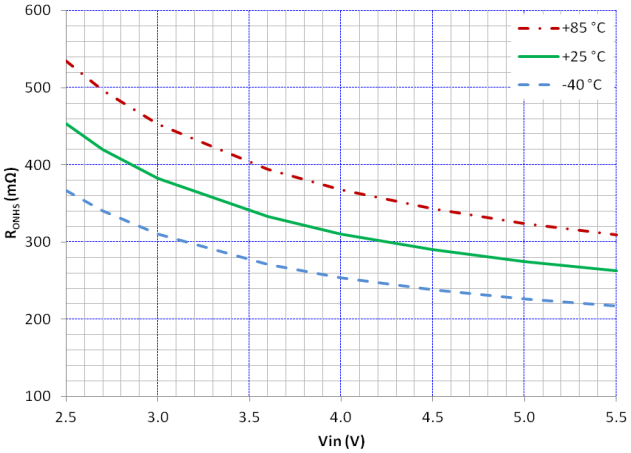


Figure 24. DCDC2 HSS R_{ON} vs V_{IN} and Temperature

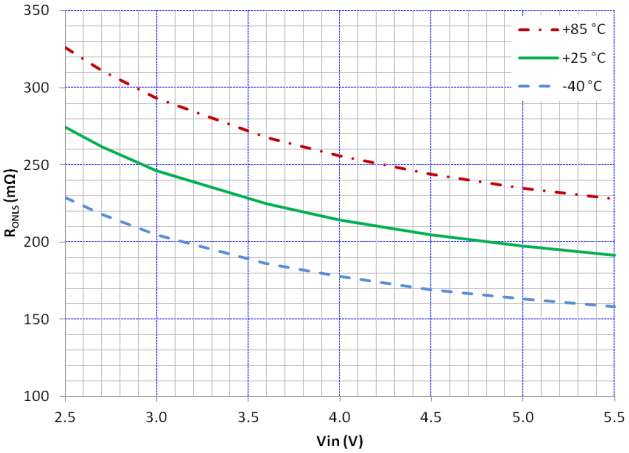


Figure 25. DCDC2 LSS R_{ON} vs V_{IN} and Temperature

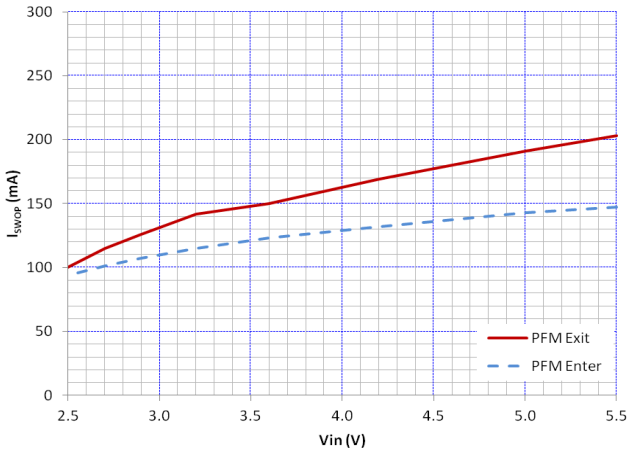


Figure 26. DCDC1 Switchover Point V_{OUT} = 1.20V

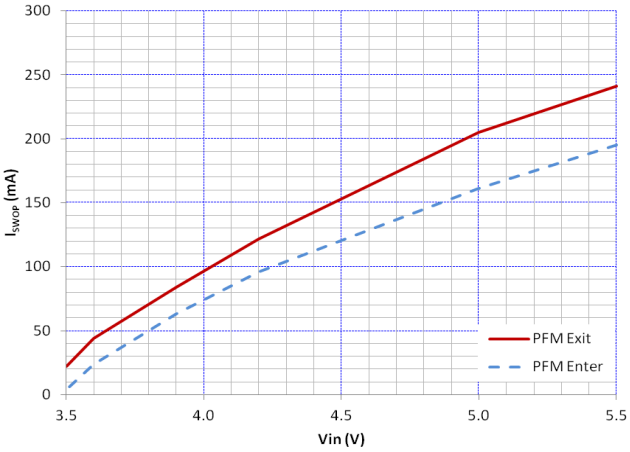


Figure 27. DCDC2 Switchover Point V_{OUT} = 3.30V

TYPICAL CHARACTERISTICS

(AV_{IN} = PV_{IN1} = PV_{IN2} = V_{IN3} = V_{IN4} = 5.0 V (Unless otherwise noted). T_A = +25°C, DCDC1 = 1.20 V, DCDC2 = 3.30 V, LDO3 = 1.15 V LDO4 = 2.5 V, C_{LDO} = 2.2 μF 0603, L_{DCDC} = 1.0 μF (SPM3012−1R0M) − C_{DCDC} = 10 μF 0603)

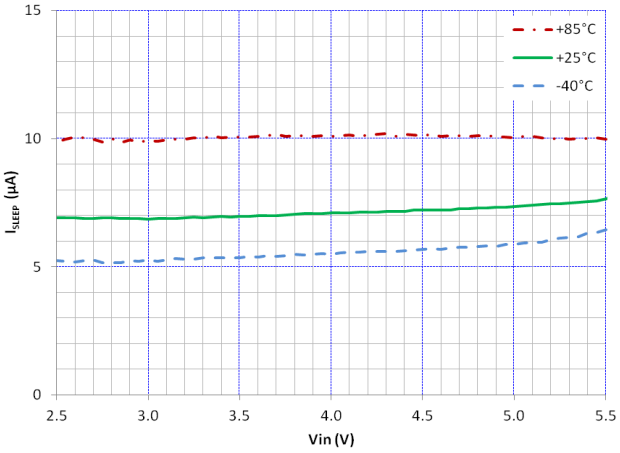


Figure 28. I_{SLEEP} vs VIN and Temperature

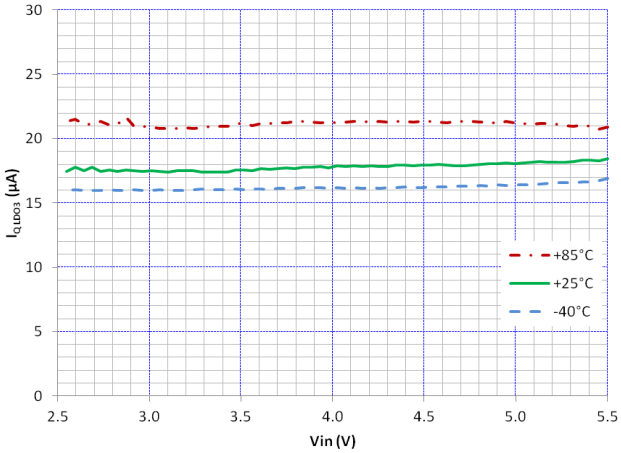


Figure 29. $I_{Q\ LDO3}$ vs VIN and Temperature

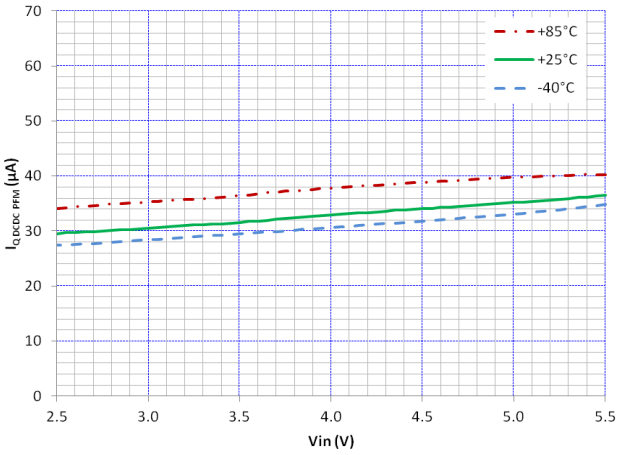


Figure 30. $I_{Q\ PFM}$ vs VIN and Temperature

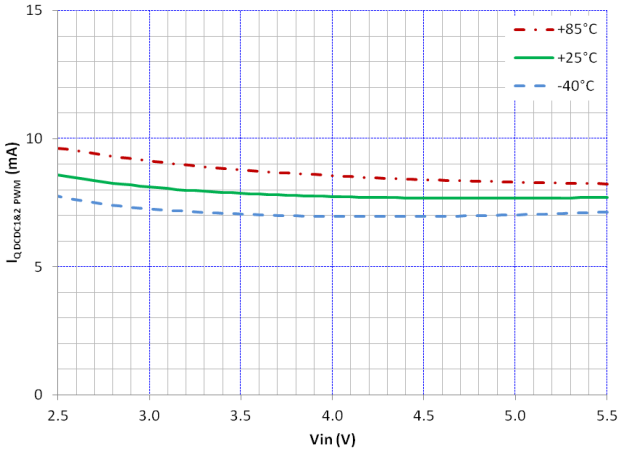


Figure 31. $I_{Q\ PWM}$ vs VIN and Temperature

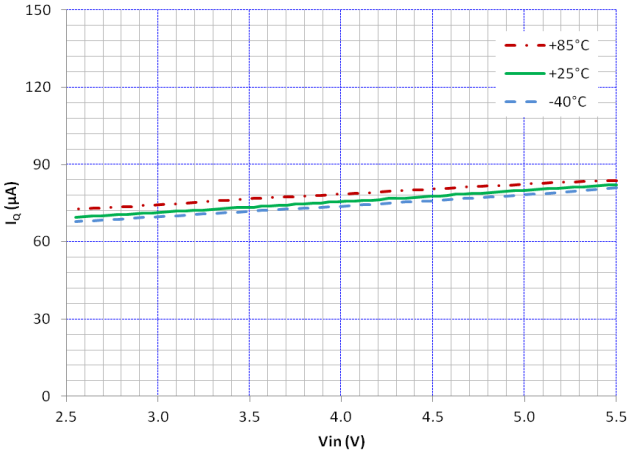


Figure 32. I_Q vs VIN and Temperature

TYPICAL CHARACTERISTICS

(AV_{IN} = PV_{IN1} = PV_{IN2} = V_{IN3} = V_{IN4} = 5.0 V (Unless otherwise noted). T_A = +25°C, DCDC1 = 1.20 V, DCDC2 = 3.30 V, LDO3 = 1.15 V LDO4 = 2.5 V, C_{LDO} = 2.2 μF 0603, L_{DCDC} = 1.0 μF (SPM3012−1R0M) − C_{DCDC} = 10 μF 0603)

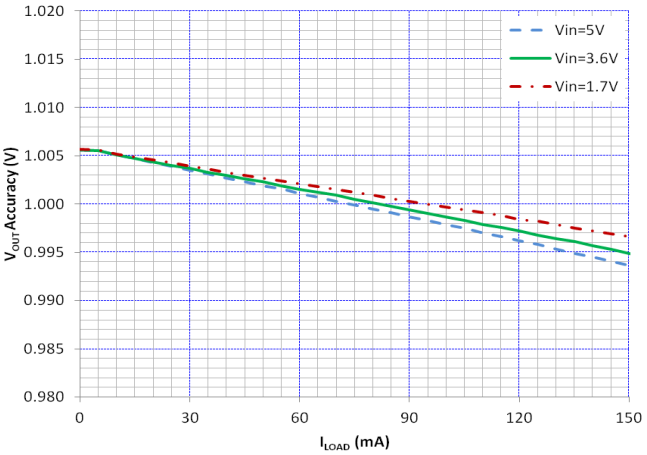


Figure 33. V_{OUT} accuracy (mV) vs I_{LOAD} and V_{IN} LDO3, V_{OUT} = 1.15 V

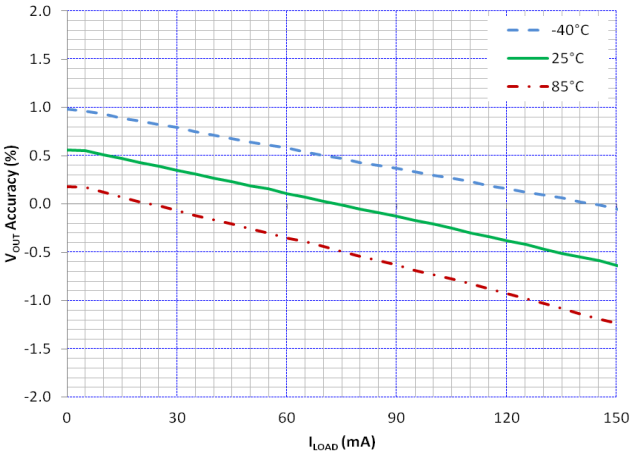


Figure 34. V_{OUT} accuracy (%) vs I_{LOAD} and V_{IN} LDO3, V_{OUT} = 1.15 V

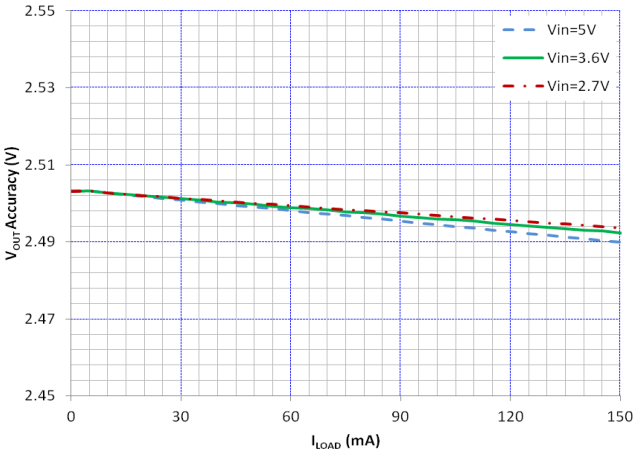


Figure 35. V_{OUT} accuracy (mV) vs I_{LOAD} and V_{IN} LDO3, V_{OUT} = 2.50 V

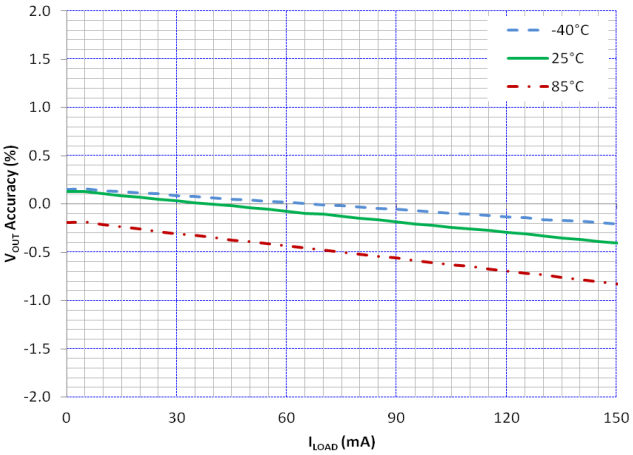


Figure 36. V_{OUT} accuracy (%) vs I_{LOAD} and V_{IN} LDO3, V_{OUT} = 2.50 V

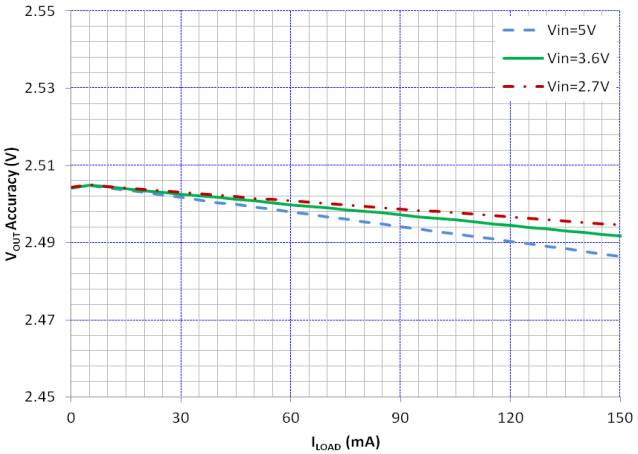


Figure 37. V_{OUT} accuracy (mV) vs I_{LOAD} and V_{IN} LDO4, V_{OUT} = 2.50 V

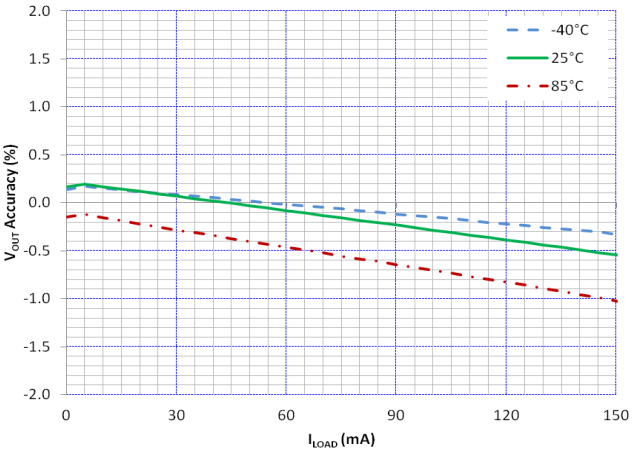


Figure 38. V_{OUT} accuracy (%) vs I_{LOAD} and V_{IN} LDO4, V_{OUT} = 2.50 V

TYPICAL CHARACTERISTICS

(AV_{IN} = PV_{IN1} = PV_{IN2} = V_{IN3} = V_{IN4} = 5.0 V (Unless otherwise noted). T_A = +25°C, DCDC1 = 1.20 V, DCDC2 = 3.30 V, LDO3 = 1.15 V LDO4 = 2.5 V, C_{LDO} = 2.2 μF 0603, L_{DCDC} = 1.0 μF (SPM3012−1R0M) − C_{DCDC} = 10 μF 0603)

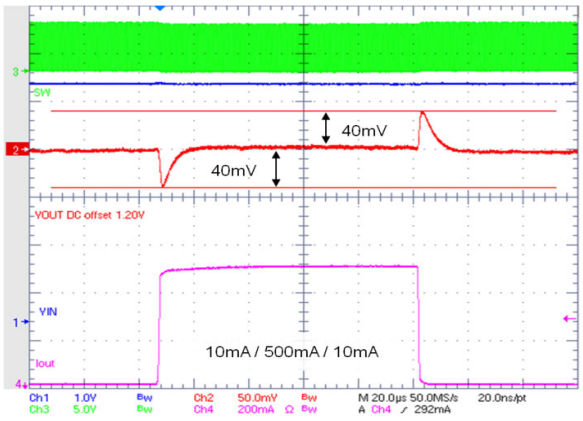


Figure 39. Load transient response DCDC1 FPWM, V_{OUT} = 1.20 V

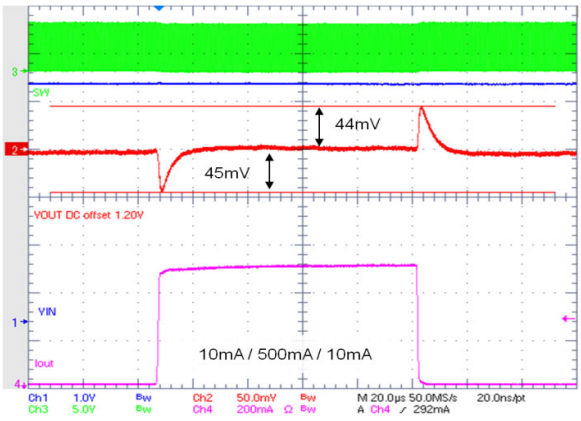


Figure 40. Load transient response DCDC2 FPWM, V_{OUT} = 1.20 V

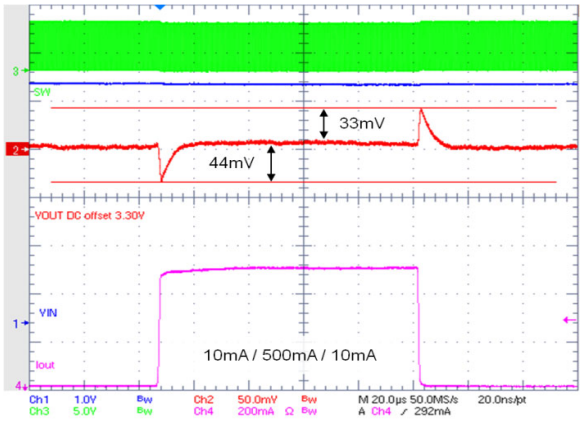


Figure 41. Load transient response DCDC2 FPWM, V_{OUT} = 3.30 V

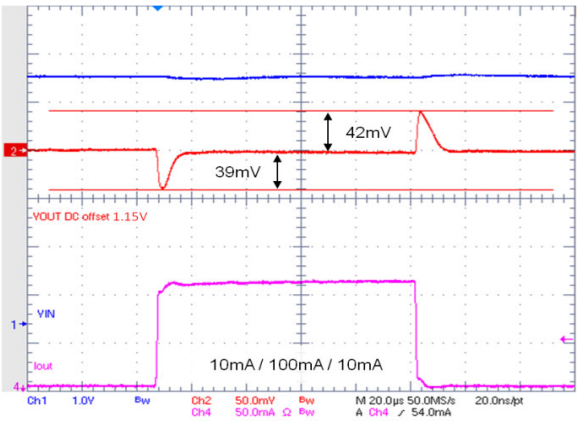


Figure 42. Load transient response LDO3, V_{OUT} = 1.35 V

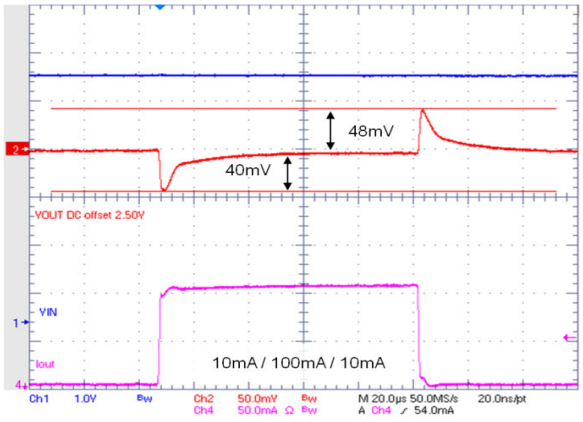


Figure 43. Load transient response LDO3, V_{OUT} = 2.50 V

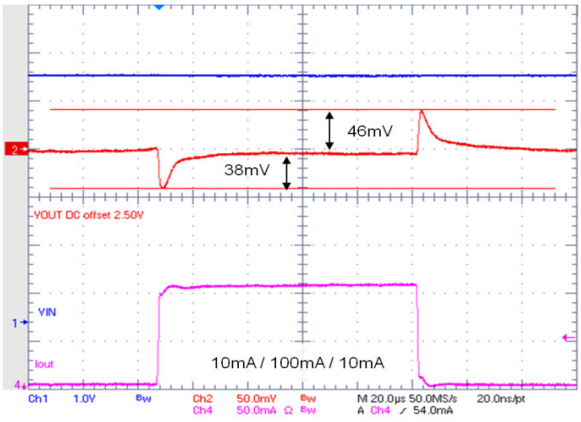


Figure 44. Load transient response LDO4, V_{OUT} = 2.50 V

TYPICAL CHARACTERISTICS

(AV_{IN} = PV_{IN1} = PV_{IN2} = V_{IN3} = V_{IN4} = 5.0 V (Unless otherwise noted). T_A = +25°C, DCDC1 = 1.20 V, DCDC2 = 3.30 V, LDO3 = 1.15 V LDO4 = 2.5 V, C_{LDO} = 2.2 μF 0603, L_{DCDC} = 1.0 μF (SPM3012−1R0M) − C_{DCDC} = 10 μF 0603)

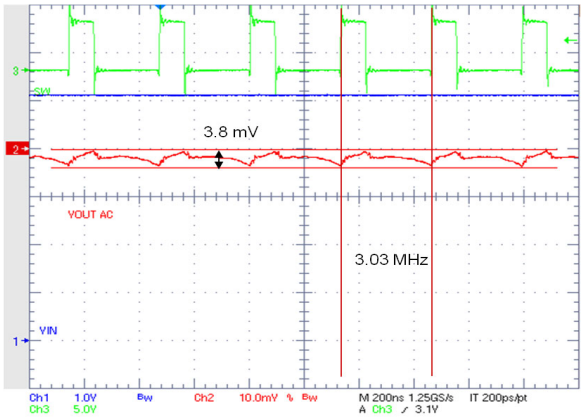


Figure 45. Ripple voltage in PWM mode DCDC1, V_{OUT} = 1.35 V, I_{OUT}=200mA

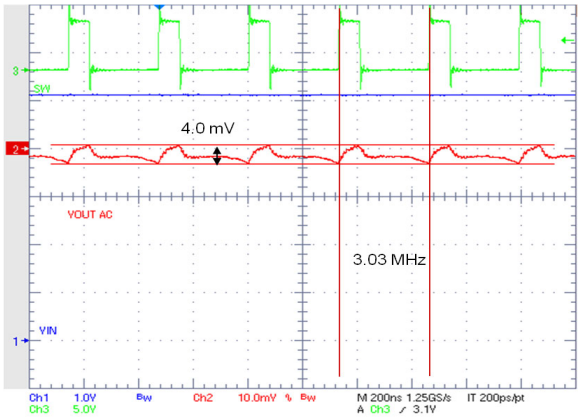


Figure 46. Ripple voltage in PWM mode DCDC2, V_{OUT} = 1.20 V, I_{OUT}=200mA

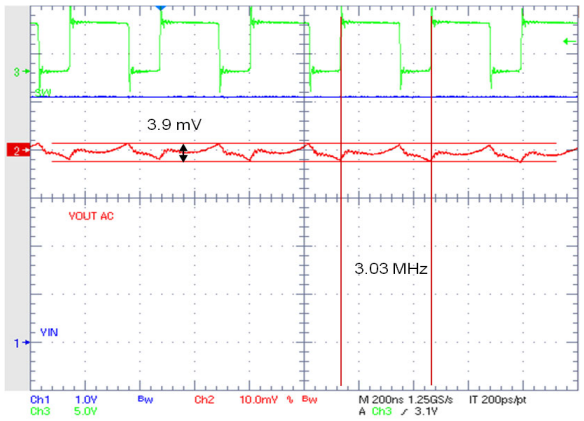


Figure 47. Ripple voltage in PWM mode DCDC2, V_{OUT} = 3.30 V, I_{OUT}=200mA

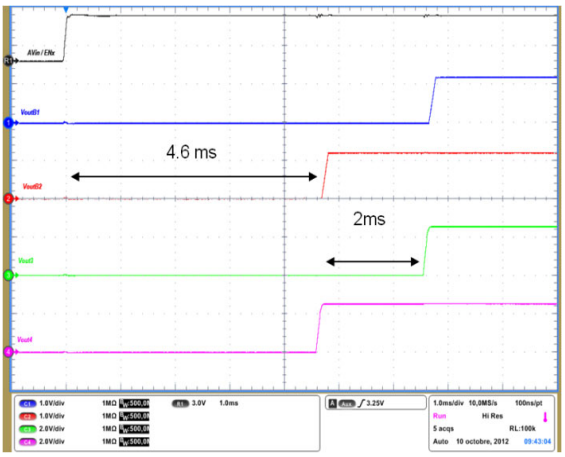


Figure 48. NCP6922CB Power−up Sequence All Enable pins high

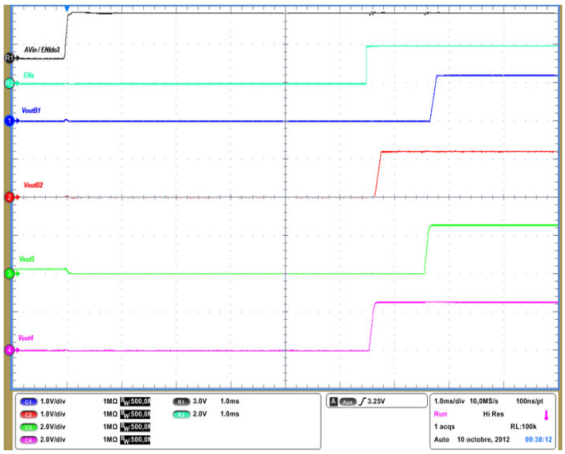


Figure 49. NCP6922CB power−up sequence ENLDO4 high first then others enable

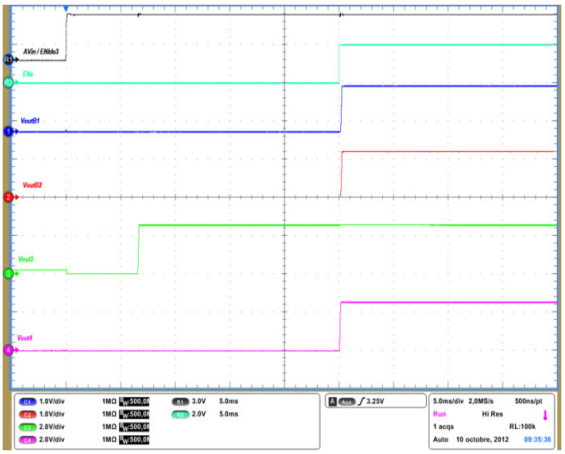


Figure 50. NCP6922CB power−up sequence All ENx after the power up sequence

TYPICAL CHARACTERISTICS

(AV_{IN} = PV_{IN1} = PV_{IN2} = V_{IN3} = V_{IN4} = 5.0 V (Unless otherwise noted). T_A = +25°C, DCDC1 = 1.20 V, DCDC2 = 3.30 V, LDO3 = 1.15 V LDO4 = 2.5 V, C_{LDO} = 2.2 μF 0603, L_{DCDC} = 1.0 μF (SPM3012−1R0M) − C_{DCDC} = 10 μF 0603)

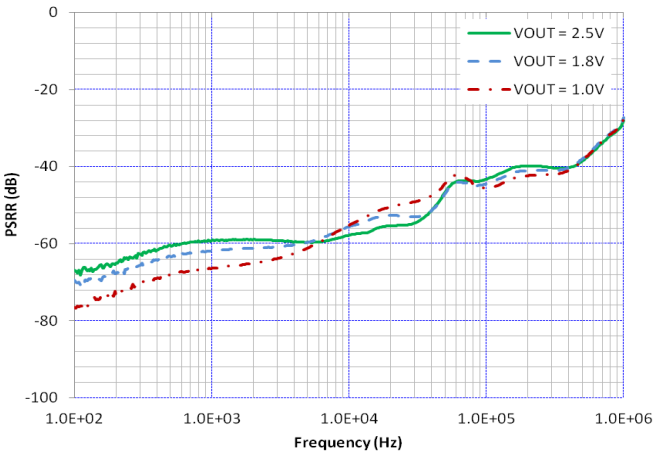


Figure 51. LDO3 PSRR I_{OUT} = 100 mA

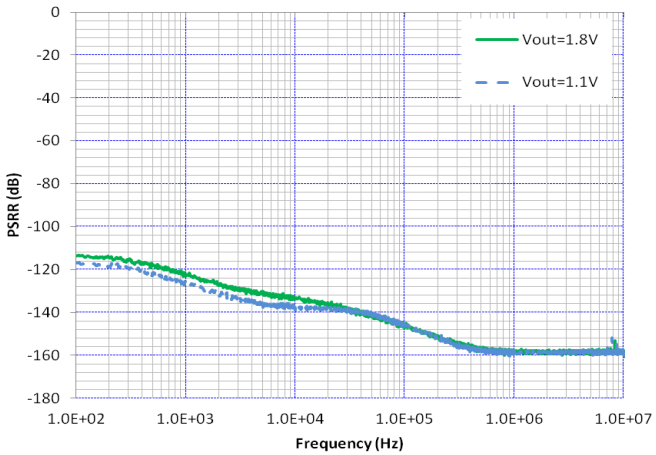


Figure 52. LDO3 Noise V_{IN} = 3.8 V, I_{OUT} = 10 mA

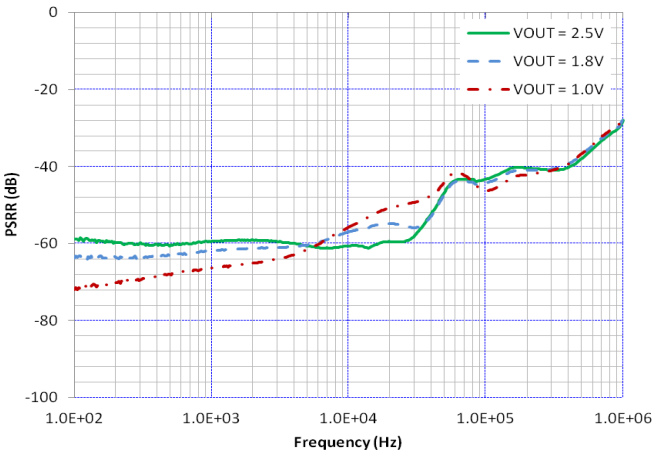


Figure 53. LDO4 PSRR I_{OUT} = 100 mA

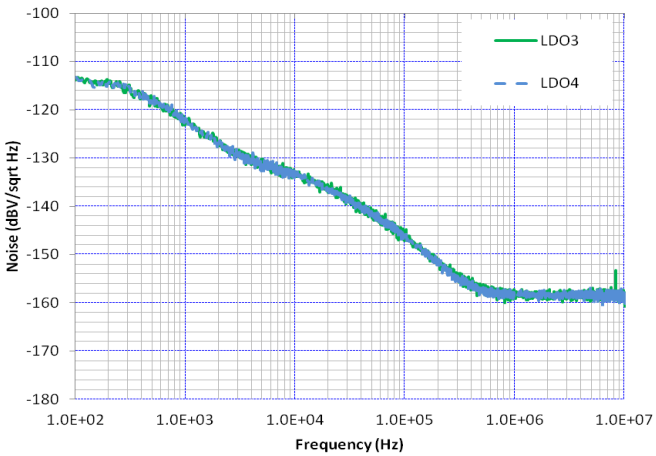


Figure 54. LDO3 vs LDO4 Noise V_{IN} = 3.8 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA

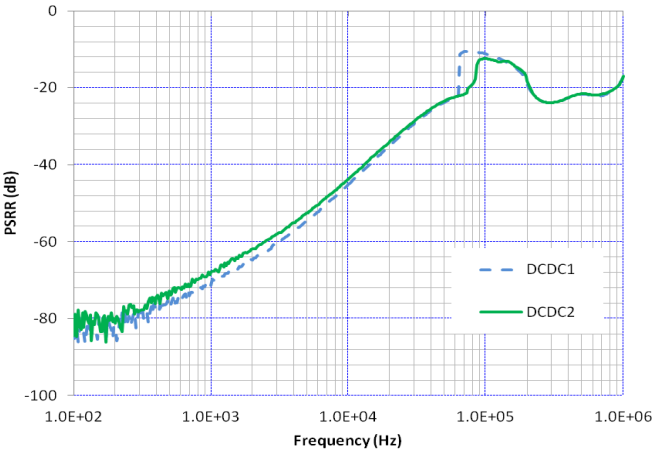


Figure 55. DCDC PSRR V_{IN} = 3.8V, V_{OUT} = 1.2 V, I_{OUT} = 200 mA

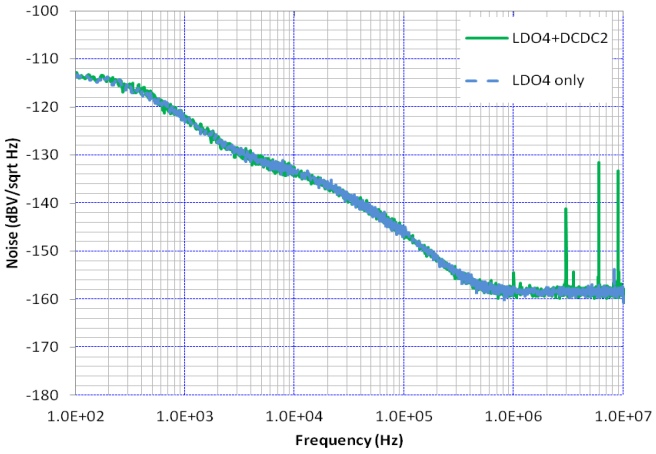


Figure 56. LDO4 noise with or without DCDC2 LDO4 V_{OUT} = 2.50 V, DCDC2 V_{OUT} = 1.80 V

GENERAL DESCRIPTION

The NCP6922C mini power management integrated circuit is optimized to supply different sub systems of battery powered portable applications. The IC can be supplied directly from the latest technology single cell batteries such as Lithium−Polymer as well as from triple alkaline cells. Alternatively, the IC can be supplied from a pre−regulated supply rail in case of multi−cell or mains powered applications.

It integrates two switched mode DC−to−DC converters and two low dropout linear regulators. The IC is widely programmable through an I^2C interface and includes low level IO signaling. An analog core provides the necessary references for the IC while a digital core ensures proper control.

The output voltage range, current capabilities and performance of the switched mode DC−to−DC converters are well suited to supply the different peripherals in the system as well as to supply processor cores. To reduce overall power consumption of the application, Dynamic Voltage Scaling (DVS) is supported on the DC−to−DC converters. For PWM operation, the converters run on a local 3 MHz clock. A low power PFM mode ensures that, even at low loads, high efficiency can be achieved. All the switching components are integrated including the compensation networks and synchronous rectifier. Only a small size 1 μH inductor and 10 μF bypass capacitor are required for typical applications.

The general purpose low dropout regulators can be used to supply the lower power rails in the application. To improve the overall application standby current, regulators bias current is very low. The regulators have their own input supply pin to be able to connect them independently to either the system supply rail or to the DC−to−DC converter output, in the application. The regulators are bypassed with a small size 2.2 μF capacitor.

All IC feature can be controlled by I^2C interface. In addition to this bus, digital control pins including individual enable (ENx) and power good (PG) are provided.

UNDER VOLTAGE LOCKOUT

The core does not operate for voltages below the Under Voltage lock Out (UVLO) level. Below UVLO threshold, all internal circuitry (both analog and digital) is held in reset.

NCP6922C operation is guaranteed down to VUVLO when battery voltage is dropping down. To avoid erratic on / off behaviour, a maximum 200 mV hysteresis is implemented. Restart is guaranteed at 2.5 V when VBAT voltage is recovering or rising up.

THERMAL SHUTDOWN

The thermal capabilities of the device can be exceeded due to the output power capabilities of the on chip step down converters and low drop out regulators. A thermal protection circuit is therefore implemented to prevent the part from being damaged. This protection circuit is only activated when the core is in active mode (at least one output channel is enabled). During thermal shutdown, all outputs of the NCP6922C are off. When the NCP6922C returns from thermal shutdown mode, it cans re−start in three different configurations depending on REARM[1:0] bits:

1. If REARM[1:0] = 00 then NCP6922C re−starts with default register values,
2. If REARM[1:0] = 01 it re−starts with register values set prior to thermal shutdown,
3. Finally if REARM[1:0] = 10, NCP6922C does not re−start automatically, a toggle of HWEN or ENx pins is needed.

In addition, a thermal warning is implemented which can inform the processor through an interrupt (if not masked) that NCP6922C is close to its thermal shutdown so that preventive measurement can be taken by software.

ACTIVE OUTPUT DISCHARGE

Active output discharge can be independently enabled / disabled by the appropriate settings in the DIS register (refer to the register definition section). However to prevent any disturbances on the power−up sequence, a quick active output discharge is done during the start−up sequence for all output channels. When the IC is turned off through HWEN pin (or ENx pins) or AVIN drops down below UVLO threshold, no shut down sequence is expected, all supplies are disabled and outputs discharged simultaneously if discharge enabled.

ENABLING

By default when applying a valid AVIN with all Enable pins (ENx) low, all supply rails will remain off. Each power rail can be independently enabled by making the ENx pins high or by setting the related enable bit in the ENABLE register, see Table 2. The voltage of the supply rails can be programmed through I^2C before enabling. A built−in pull−down resistor disables supply rail if the corresponding EN pin is left unconnected.

Power Up Sequence and ENx

When applying a valid AVIN with all ENx pins high, the part will start up in the default configuration that is factory programmed. This default configuration determines the order of enabling and the output voltage.

During the power−up sequence, the state of a LDO/DC−to−DC is defined by its corresponding EN pin, its I^2C EN bit and its TAP position in the sequence. The LDO/DC−to−DC will be enabled as soon as the sequencer passes its TAP, AND the corresponding EN pin OR I^2C EN bit is high.

Any order and output voltage setting can be factory programmed upon request.

Two different power−up sequences are pre−defined:

Table 5. NCP6922CB POWER UP SEQUENCE

Rail	Sequencer	Default Vprog	Default Mode – ON/OFF
DCDC1	T2	1.20 V	Forced PWM – OFF
DCDC2	T1	1.20 V	Forced PWM – OFF
LDO3	T2	2.50 V	OFF
LDO4	T1	2.50 V	OFF

Table 6. NCP6922CC POWER UP SEQUENCE

Rail	Sequencer	Default Vprog	Default Mode – ON/OFF
DCDC1	T3	1.35 V	Forced PWM – OFF
DCDC2	T0	3.30 V	Auto mode – OFF
LDO3	T0	1.15 V	OFF
LDO4	T0	2.50 V	OFF

Table 7. NCP6922CD POWER UP SEQUENCE

Rail	Sequencer	Default Vprog	Default Mode – ON/OFF
DCDC1	T2	1.50 V	Auto Mode – ON
DCDC2	T4	1.10 V	Auto Mode – ON
LDO3	T1	1.80 V	ON
LDO4	T3	3.30 V	ON

NCP6922CB power−up diagrams are depicted in Figures 57, 58, 59:

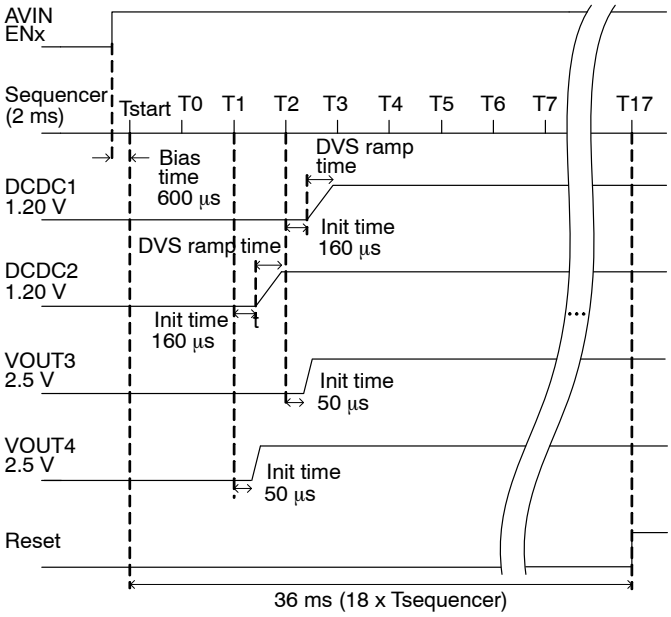


Figure 57. NCP6922CB Power Up Sequence with All ENx Pins High

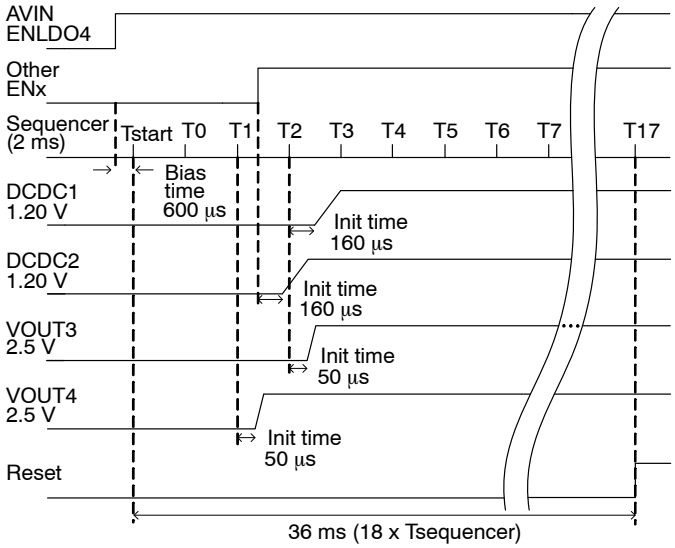


Figure 58. NCP6922CB Power−up Sequence with Only ENLDO4 High First then Others Enable

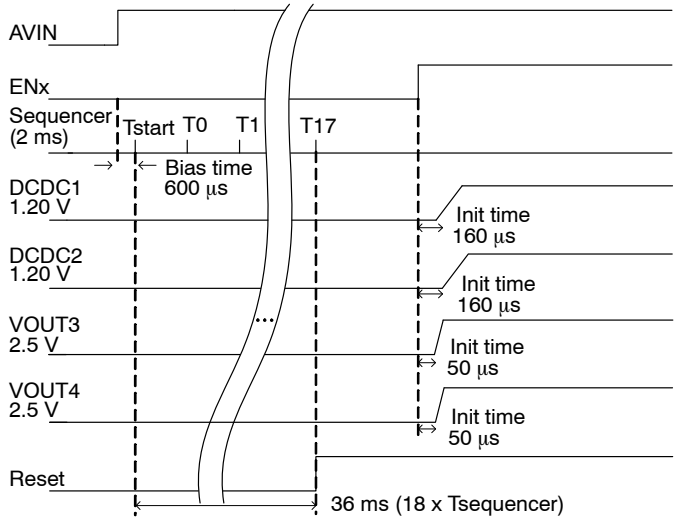


Figure 59. NCP6922CB Power−up Sequence with All ENx After the Power Up Sequence

I^{2}C registers can be read and written while ENx pins are low. By programming the appropriate registers (see registers description section), the power up sequence can be modified.

Reset to the factory default configuration can be achieved either by hardware reset (all power supplies removed) or by writing through the I^{2}C in the RESET register.

Enable Control

Table 8. TRUTH TABLE OF ENABLE/DISABLE CONTROL

Enable Pin	Enable bit	Output
L	0	Disabled
L	1	Enabled
H	0	Enabled
H	1	Enabled

Note that each enable pin has a corresponding sense bit reflecting the state of the pin: sense bit is 1 when pin is high (filtered) and 0 when the pin is low (filtered).

Shutdown

When shutting down the device (AVIN falls below the Under Voltage threshold VUVLO), no shut down sequence is applied. All supplies are disabled and outputs are discharged simultaneously, and PG open drain output is low.

DYNAMIC VOLTAGE SCALING (DVS)

The step down converters support dynamic voltage scaling (DVS). This means output voltage can be individually reprogrammed by I^{2}C commands to provide the different voltages required by the processor. Change between two different voltages is managed in a smooth manner without disturbing the operation of the processor.

When programming a higher voltage, the reference of the switcher and therefore the output is raised in equidistant steps per defined time period such that the dV/dt is controlled (by default 12.5 mV / 1.33 μs). When programming a lower voltage the output voltage will decrease accordingly. The DVS step is fixed and the speed is programmable.

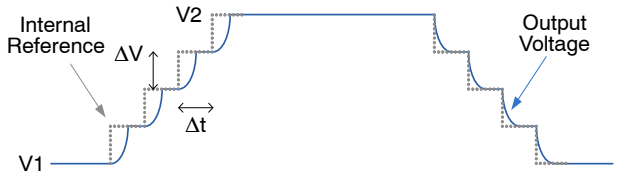


Figure 60. Default Dynamic Voltage Scaling Effect Timing Diagram

Programmability

DC−to−DC converter output voltage can be controlled by GOx bit (TIME register) with VPROGDCDCx[7:0] and VDVSDCDCx[7:0] registers. Available output levels are listed in table VPROGDCDCx[7:0] and VDVSDCDCx[7:0] in register description.

GOx bit determines whether DC−to−DC output voltage value is set in VPROGDCDCx[7:0] register or in VDVSDCDCx[7:0] register.

Table 9. GO BIT DESCRIPTION

GOx	Bit Description
0	Output voltage is set to VPROGDCDCx
1	Output voltage is set to VDVSDCDCx

The two DVS bits in the TIME register determine the ramp up time per each voltage step.

Table 10. DVS BITS DESCRIPTION

DVS [1:0]	Bit Description
00	1.33 μs per step (default)
01	2.67 μs per step
10	5.33 μs per step
11	10.67 μs per step

There are two ways of I^2C registers programming to switch the DC−to−DC converters output voltages between different levels:

1. Preset VPROGDCDCx[7:0] and VDVSDCDCx[7:0] registers, and start DVS sequence by changing GOx bit state.
2. GOx bit remains unchanged, change output voltage value in either VPROGDCDCx[7:0] or VDVSDCDCx[7:0] register.

For example, the device needs to supply either 1.2 V or 0.9 V depending on working conditions. If using method 1, VPROGDCDCx[7:0] and VDVSDCDCx[7:0] should be set as shown in Table 11. GOx bit should be programmed to 1 to change DCDCx Output Voltage from 1.2 V to 0.9 V, and be programmed to 0 to move back from 0.9 V to 1.2 V.

Table 11. VPROGDCDCX / VDVSDCDCX SETTINGS FOR VDCDCX SWITCHING BETWEEN 1.2 V AND 0.9 V

Register Name	Values	Target VDCDC (V)
VPROGDCDCx	0$30	1.2
VDVSDCDCx	0$18	0.9

DC−to−DC CONVERTERS AND LDOS POWER GOOD

To indicate the output of a converter is established, a power good signal is available for each output channel (routed in the INT_SEN1 register). The power good signal is high when the channel is off and goes low when enabling the channel. Once the output voltage reaches the expected output level, the power good signal becomes high again.

When during operation the output gets below 90% of the expected level, the power good signal goes low which indicates a power failure. When the voltage rises again above 95% the power good signal goes high again.

Note that these PG Sense bits are independent of PGASSIGN_x and PGGATE_x bits.

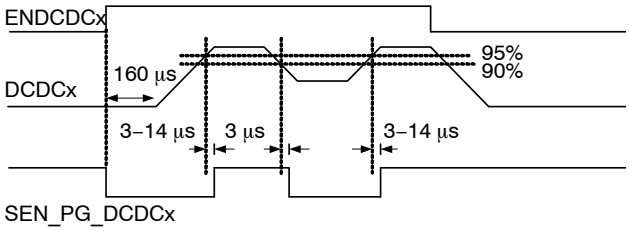


Figure 61. DCDCx Channel Internal Power Good Signal

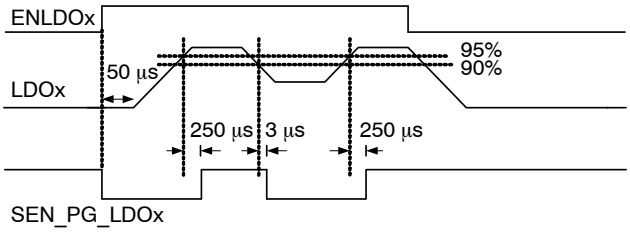


Figure 62. DCDCx Channel Internal Power Good Signal

Power Good Assignment and Gating

Each power good sense signal can be individually assigned to the PG pin through PGASSIGN_x bits of PGOOD1 register. In addition, 3 other signals can be assigned to the PG pin: the internal reset signal and the DCDC DVS signals through the PGOOD1 register. By assigning the internal reset signal, the PG pin is held low throughout the power up sequence and the reset period (by default). By assigning the DVS signal of a converter, the PG pin is made low during the period the output voltage is being

raised to the new setting as shown in Figure 63. The PG pin state is an AND combination of assigned signals.

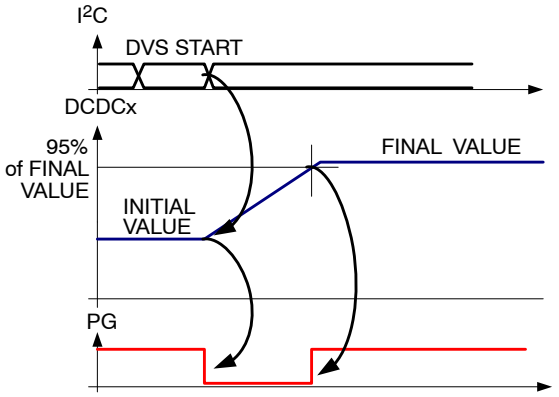


Figure 63. PG Operation in DVS Sequence

Moreover PGGATE_x bits of the PGOOD2 register force the PG pin low when the channel is off.

POWER GOOD PIN

The PG pin is an open drain output. By default, the power good signal of DCDC2 converter and reset signal are assigned to the PG pin and DCDC2 gates PG pin.

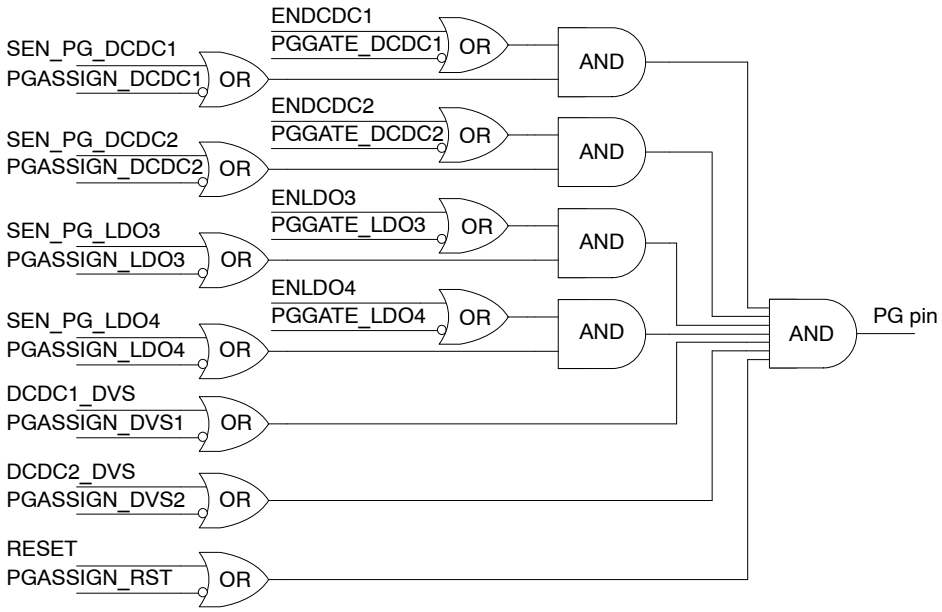


Figure 64. PG Pin Description Behavior

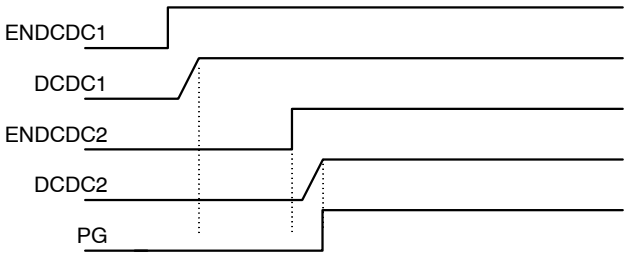


Figure 65. Power Good Behavior in Case of DCDC2 Monitoring and DCDC2 Gating

Power Good Delay

A delay can be programmed between the moment the AND result of the assigned internal power good signals becomes high and the moment the PG pin is released. The delay is set from 0 ms to 512 ms through the TOR[2:0] bits in the TIME register. The default delay is 0 ms could be change upon request

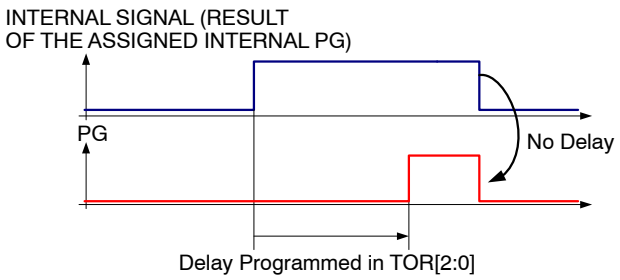


Figure 66. PG Delay

Interrupt

The interrupt controller continuously monitors internal interrupt sources, generating an interrupt signal when a system status change is detected (dual/rising edge monitoring). The interrupt sources include:

Table 12. INTERRUPT SOURCES

Interrupt	Description
PG_DCDC1	DCDC1 Converter Power Good (dual edge)
PG_DCDC2	DCDC2 Converter Power Good (dual edge)
PG_LDO3	LDO3 Power Good (dual edge)
PG_LDO4	LDO4 Power Good (dual edge)
UVLO	UVLO state (dual edge)
IDCDC1	DCDC1 Converter Output Over Current (rising edge)
IDCDC2	DCDC2 Converter Output Over Current (rising edge)
ILDO3	LDO3 Output Over Current (dual edge)
ILDO4	LDO4 Output Over Current (dual edge)
WNRG	Thermal Warning (dual edge)
TSD	Thermal Shutdown (dual edge)

Individual bits generating interrupts will be set to 1 in the INT_ACK1/INT_ACK2 registers (I^2C read only registers), indicating the interrupt source. INT_ACK1/INT_ACK2 registers are reset by an I^2C read. INT_SEN1/INT_SEN2 registers (read only registers) are real time indicators of interrupt sources.

When the host reads the INT_ACK1/INT_ACK2 registers the interrupt registers INT_ACK1/INT_ACK2 are cleared.

Figure 67 shows how DCDC1 converter power good produces interrupt with INT_SEN1/INT_ACK1 and I^2C read access (assuming no other interrupt happens during this read period).

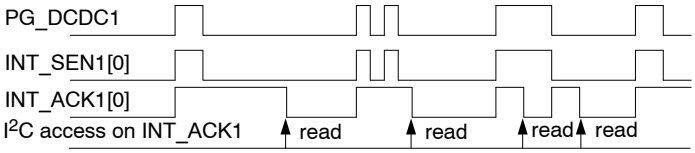


Figure 67. Interrupt Timing Chart Example of PG_DCDC1

Note that each enable pin has a corresponding sense bit reflecting the state of the pin, without interrupt associated.

LOW DROP OUT REGULATOR

The LDOs (low drop out regulator) are based on an embedded PMOS and requires no external stability components or feedback networks.

The low drop out regulators can be supplied from the systems supply rail such as a battery or from a step down convertor as available on the IC itself. The latter case provides a power efficient line up when the voltage drop allows such. When the output of the LDO gets out of regulation, due to for instance a short at the output, an interrupt is generated and optionally the LDO is automatically disabled.

Current Limitation

Both LDOs have foldback current limiter: the goal of the foldback current limit is to reduce the output voltage and the current in order to limit the power dissipation (see Figure 68). Under a short circuit, where the output voltage has reduced below ~30% nominal value, the current (I_{SC}) is typically limited to a small fraction of the maximum current (I_{LIMIT}).

Foldback also reduces power dissipation in the load in fault conditions, which can reduce the risks of fire and heat damage.

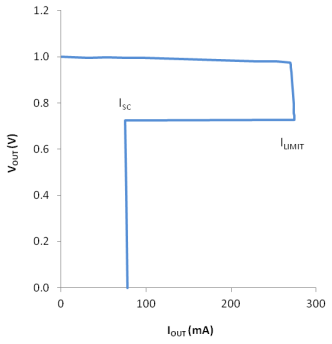


Figure 68. 1.0 V LDO Foldback Current Limit Principe

DC−to−DC STEP DOWN CONVERTERS

The DC−to−DC converters are synchronous rectifier type with both high side and low side integrated switches. Neither external transistor nor diodes are required for proper operation. Feedback and compensation network are also fully integrated.

The DC−to−DC converters can operate in two different modes: PWM and PFM. The transition between PWM/PFM modes can occur automatically or the switcher can be placed in forced PWM mode by I^2C programming. (MODEDCDC1 & MODEDCDC2 bits of ENABLE register)

PWM (Pulse Width Modulation) Operating Mode

In medium and high load conditions, DC−to−DCs operate in PWM mode from a fixed clock and adapts its duty cycle to regulate the desired output voltage. In this mode, the inductor current is in CCM and the voltage is regulated by PWM. The internal N−MOSFET switch operates as synchronous rectifier and is driven complementary to the P−MOSFET switch. In CCM, the lower switch (N−MOSFET) in a synchronous converter provides a lower voltage drop than the diode in an asynchronous converter, which provides less loss and higher efficiency.

PFM (Pulse Frequency Modulation) Operating Mode

In order to save power and improve efficiency at low loads the DC−to−DC converters operate in PFM mode as the inductor drops into DCM (Discontinuous Current Mode). The upper FET on time is kept constant and the switching frequency is variable. Output voltage is regulated by varying the switching frequency which becomes proportional to loading current. As it does in PWM mode, the internal N−MOSFET operates as synchronous rectifier after each P−MOSFET on−pulse with very small negative current limit. When load increases and current in inductor becomes continuous again, the controller automatically turns back to PWM fixed frequency mode.

Forced PWM

The DC−to−DC converters can be programmed to only use PWM and disable the transition to PFM.

Table 13. MODEDCDC1&2 BIT DESCRIPTION

MODEDCDC1&2	Bit Description
0	Auto switching PFM / PWM
1	Forced PWM

Inductor Peak Current Limitation

During normal operation, peak current limitation will monitor and limit the current through the inductor. This current limitation is particularly useful when size and/or height constrains inductor power

Soft Start

A soft start is provided to limit inrush currents when enabling the converter. After enabling and internal delays elapsed, the DC to DC converter output will gradually ramp up to the programmed voltage.

I²C COMPATIBLE INTERFACE

NCP6922C can support a subset of I²C protocol, below are detailed introduction for I²C programming.

I²C Communication Description

ON Semiconductor communication protocol is a subset of I²C protocol.

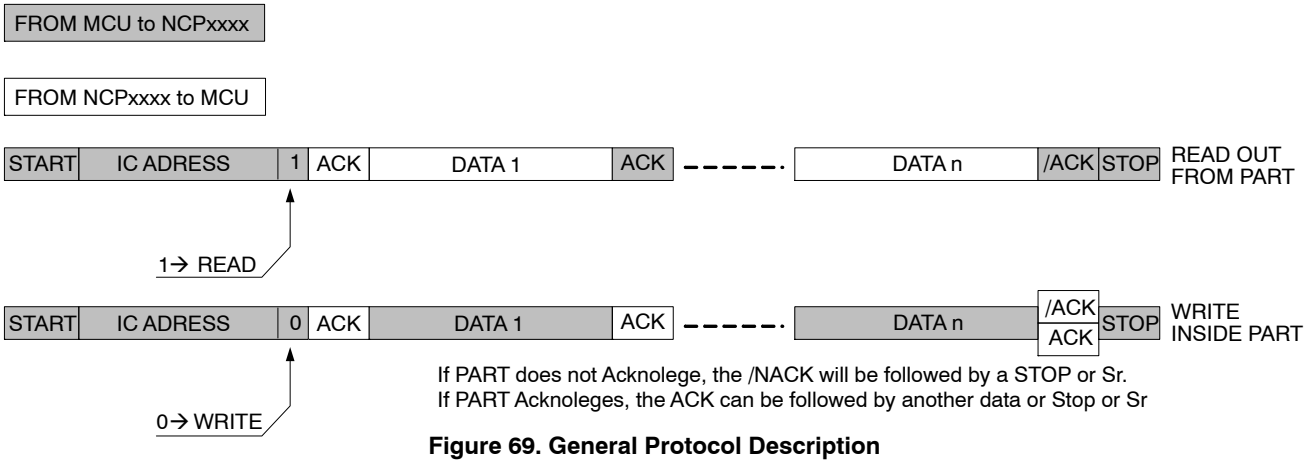


Figure 69. General Protocol Description

The first byte transmitted is the Chip address (with LSB bit sets to 1 for a read operation, or sets to 0 for a Write operation). Then the following data will be:

- In case of a Write operation, the register address (@REG) we want to write in followed by the data we will write in the chip. The writing process is incremental. So the first data will be written in @REG, the second one in @REG + 1... The data are optional.
- In case of read operation, the NCP6922C will output the data out from the last register that has been accessed by the last write operation. Like writing process, reading process is an incremental process.

Read Out from Part

The Master will first make a “Pseudo Write” transaction with no data to set the internal address register. Then, a stop then start or a Repeated Start will initiate the read transaction from the register address the initial write transaction has set:

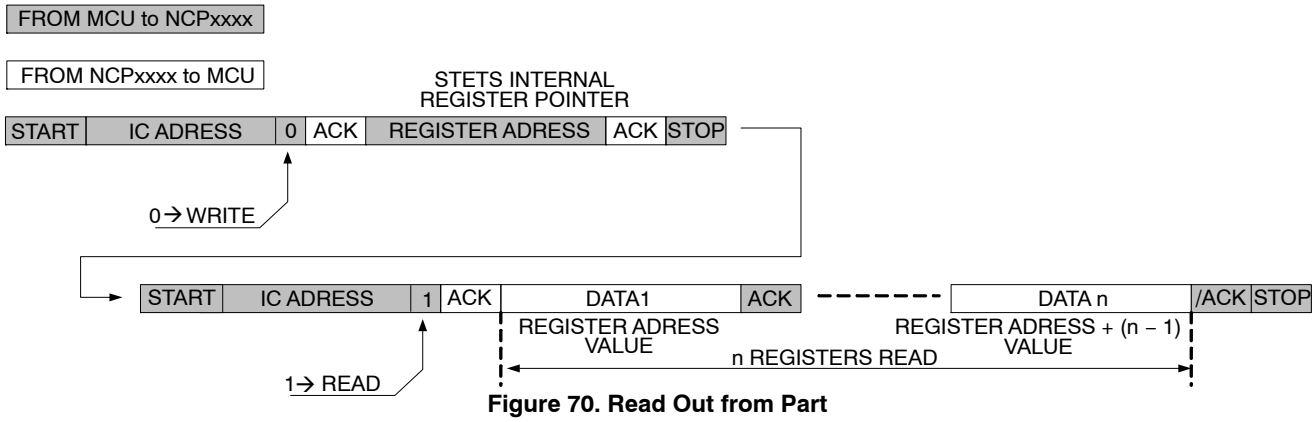


Figure 70. Read Out from Part

The first WRITE sequence will set the internal pointer on the register we want access to. Then the read transaction will start at the address the write transaction has initiated.

Transaction with Real Write then Read:

With Stop Then Start

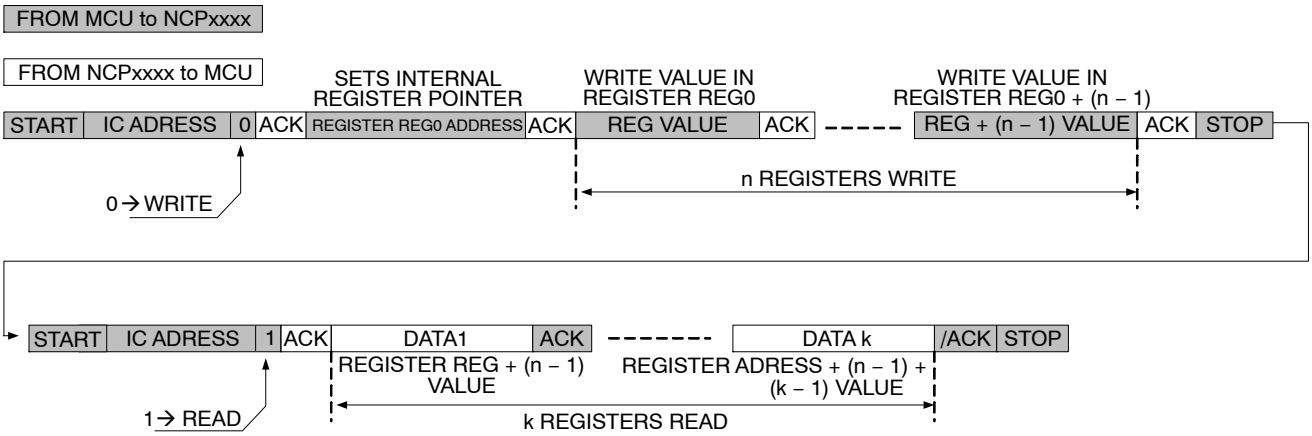


Figure 71. Write Followed by Read Transaction

Write In Part

Write operation will be achieved by only one transaction. After chip address, the MCU first data will be the internal register we want access to, then following data will be the data we want to write in Reg, Reg + 1, Reg + 2, ..., Reg +n.

Write n Registers:

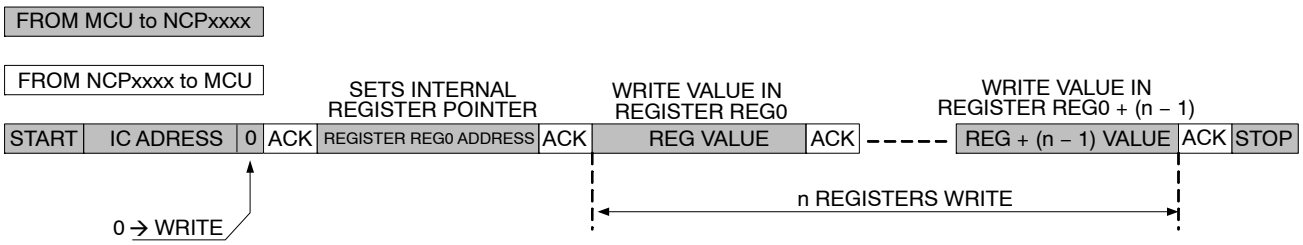


Figure 72. Write In n Registers

I²C Address

NCP6922C has fixed I²C (7 bit address, see below table A7~A1):

Table 14. NCP6922C I²C ADDRESS

I²C Address	Hex	A7	A6	A5	A4	A3	A2	A1	A0
NCP6922CBMTTXG	W 0x28 R 0x29	0	0	1	0	1	0	0	R/W
	Add	0x14							–
NCP6922CCMTTXG	W 0x30 R 0x31	0	0	1	1	0	0	0	R/W
	Add	0x18							–
NCP6922CDMTTXG	W 0x30 R 0x31	0	0	1	1	0	0	0	R/W
	Add	0x18							–

Register Map

Following register map describes I²C registers.

Registers can be:

R	Read only register
RC	Read then Clear
RW	Read and Write register
RWM	Read, Write and can be modified by the IC
Reserved	Address is reserved and register is not physically designed
Spare	Address is reserved and register is physically designed

Table 15. I²C REGISTER MAP NCP6922CB CONFIGURATION

Address	Register Name	Type	Default	Function
0x00	INT_ACK1	RC	0x00	Interrupt 1 Register, dual edge
0x01	INT_ACK2	RC	0x00	Interrupt 2 Register, rising edge and dual edge
0x02	INT_SEN1	R	0x03	Sense 1 Register, real time status
0x03	INT_SEN2	R	0x00	Sense 2 Register, real time status
0x04 to 0x0F	–	–	0x00	Reserved, do not access these registers
0x10	RESET	RW	0x10	Reset Register
0x11	PID	R	0x0C	Product Identification
0x12	RID / FID	R	0x3B	Revision Identification / Features Identification
0x13	–	–	0x00	Reserved, do not access these registers
0x14	ENABLE	RWM	fuse 0x05	Enable Register
0x15	DIS	RW	fuse 0x33	Active Output Discharge Register
0x16	PGOOD1	RW	fuse 0x42	Power Good Pin Assignment
0x17	PGOOD2	RW	fuse 0x02	Power Good Pin Gating
0x18	TIME	RW	0x00	Timing Definition
0x19	SEQUENCER1	RW	fuse 0x0A	Sequencer register for DCDC1 and DCDC2
0x1A	–	–	0x00	Reserved, do not access these registers
0x1B	SEQUENCER2	–	fuse 0x0A	Sequencer register for LDO3 and LDO4
0x1C to 0x1F	–	–	0x00	Reserved, do not access these registers
0x20	VPROGDCDC1	RW	fuse 0x30	DCDC1 Output Voltage Setting
0x21	VPROGDVS1	RW	fuse 0x30	DCDC1 DVS Output Voltage Setting
0x22	VPROGDCDC2	RW	fuse 0x30	DCDC2 Output Voltage Setting
0x23	VPROGDVS2	RW	fuse 0x30	DCDC2 DVS Output Voltage Setting
0x24 to 0x25	–	–	0x00	Reserved, do not access these registers
0x26	VPROGLDO3	RW	fuse 0x1E	LDO3 Output Voltage Setting
0x27	VPROGLDO4	RW	fuse 0x1E	LDO4 Output Voltage Setting
0x28 to 0x3F	–	–	0x00	Reserved, do not access these registers

Table 16. I²C REGISTER MAP NCP6922CC CONFIGURATION

Address	Register Name	Type	Default	Function
0x00	INT_ACK1	RC	0x00	Interrupt 1 Register, dual edge
0x01	INT_ACK2	RC	0x00	Interrupt 2 Register, rising edge and dual edge
0x02	INT_SEN1	R	0x03	Sense 1 Register, real time status
0x03	INT_SEN2	R	0x00	Sense 2 Register, real time status
0x04 to 0x0F	–	–	0x00	Reserved, do not access these registers
0x10	RESET	RW	0x10	Reset Register
0x11	PID	R	0x0C	Product Identification
0x12	RID / FID	R	0x3C	Revision Identification / Features Identification
0x13	–	–	0x00	Reserved, do not access these registers
0x14	ENABLE	RWM	fuse 0x01	Enable Register
0x15	DIS	RW	fuse 0x33	Active Output Discharge Register
0x16	PGOOD1	RW	fuse 0x42	Power Good Pin Assignment
0x17	PGOOD2	RW	fuse 0x02	Power Good Pin Gating
0x18	TIME	RW	0x00	Timing Definition
0x19	SEQUENCER1	RW	fuse 0x03	Sequencer register for DCDC1 and DCDC2
0x1A	–	–	0x00	Reserved, do not access these registers
0x1B	SEQUENCER2	–	fuse 0x00	Sequencer register for LDO3 and LDO4
0x1C to 0x1F	–	–	0x00	Reserved, do not access these registers
0x20	VPROGDCDC1	RW	fuse 0x3C	DCDC1 Output Voltage Setting
0x21	VPROGDVS1	RW	fuse 0x3C	DCDC1 DVS Output Voltage Setting
0x22	VPROGDCDC2	RW	fuse 0xD8	DCDC2 Output Voltage Setting
0x23	VPROGDVS2	RW	fuse 0xD8	DCDC2 DVS Output Voltage Setting
0x24 to 0x25	–	–	0x00	Reserved, do not access these registers
0x26	VPROGLDO3	RW	fuse 0x03	LDO3 Output Voltage Setting
0x27	VPROGLDO4	RW	fuse 0x1E	LDO4 Output Voltage Setting
0x28 to 0x3F	–	–	0x00	Reserved, do not access these registers

Table 17. I²C REGISTER MAP NCP6922CD CONFIGURATION

Address	Register Name	Type	Default	Function
0x00	INT_ACK1	RC	0x00	Interrupt 1 Register, dual edge
0x01	INT_ACK2	RC	0x00	Interrupt 2 Register, rising edge and dual edge
0x02	INT_SEN1	R	0x03	Sense 1 Register, real time status
0x03	INT_SEN2	R	0x00	Sense 2 Register, real time status
0x04 to 0x0F	–	–	0x00	Reserved, do not access these registers
0x10	RESET	RW	0x10	Reset Register
0x11	PID	R	0x0C	Product Identification
0x12	RID / FID	R	0x2C	Revision Identification / Features Identification
0x13	–	–	0x00	Reserved, do not access these registers
0x14	ENABLE	RWM	fuse 0xCA	Enable Register
0x15	DIS	RW	fuse 0x33	Active Output Discharge Register
0x16	PGOOD1	RW	fuse 0x73	Power Good Pin Assignment
0x17	PGOOD2	RW	fuse 0x00	Power Good Pin Gating
0x18	TIME	RW	0x00	Timing Definition
0x19	SEQUENCER1	RW	fuse 0x22	Sequencer register for DCDC1 and DCDC2
0x1A	–	–	0x00	Reserved, do not access these registers
0x1B	SEQUENCER2	–	fuse 0x19	Sequencer register for LDO3 and LDO4
0x1C to 0x1F	–	–	0x00	Reserved, do not access these registers
0x20	VPROGDCDC1	RW	fuse 0x48	DCDC1 Output Voltage Setting
0x21	VPROGDVS1	RW	fuse 0x48	DCDC1 DVS Output Voltage Setting
0x22	VPROGDCDC2	RW	fuse 0x28	DCDC2 Output Voltage Setting
0x23	VPROGDVS2	RW	fuse 0x28	DCDC2 DVS Output Voltage Setting
0x24 to 0x25	–	–	0x00	Reserved, do not access these registers
0x26	VPROGLDO3	RW	fuse 0x10	LDO3 Output Voltage Setting
0x27	VPROGLDO4	RW	fuse 0x2E	LDO4 Output Voltage Setting
0x28 to 0x3F	–	–	0x00	Reserved, do not access these registers

Registers Description

Table 18. INT_ACK1 REGISTER

Name: INT_ACK1				Address: 0x00			
Type: RC				Default: 0x00			
D7	D6	D5	D4	D3	D2	D1	D0
spare=0	spare=0	ACK_PG_LDO4	ACK_PG_LDO3	spare=0	spare=0	ACK_PG_DCDC2	ACK_PG_DCDC1

Table 19. BIT DESCRIPTION OF INT_ACK1 REGISTER

Bit	Bit Description
ACK_PG_DCDC1	DCDC1 Power Good Sense Acknowledgement 0: Cleared 1: DCDC1 Power Good Event detected
ACK_PG_DCDC2	DCDC2 Power Good Sense Acknowledgement 0: Cleared 1: DCDC2 Power Good Event detected
ACK_PG_LDO3	LDO3 Power Good Sense Acknowledgement 0: Cleared 1: LDO3 Power Good Event detected
ACK_PG_LDO4	LDO4 Power Good Sense Acknowledgement 0: Cleared 1: LDO4 Power Good Event detected
ACK_UVLO	Under Voltage Sense Acknowledgement 0: Cleared 1: Under Voltage Event detected

Table 20. INT_ACK2 REGISTER

Name: INT_ACK2				Address: 0x01			
Type: RC				Default: 0x00			
D7	D6	D5	D4	D3	D2	D1	D0
ACK_TSD	ACK_WNRG	ACK_ILDO4	ACK_ILDO3	spare=0	ACK_UVLO	ACK_IDCDC2	ACK_IDCDC 1

Table 21. BIT DESCRIPTION OF INT_ACK2 REGISTER

Bit	Bit Description
ACK_IDCDC1	DCDC1 Over Current Sense Acknowledgement 0: Cleared 1: DCDC1 Over Current Event detected
ACK_IDCDC2	DCDC2 Over Current Sense Acknowledgement 0: Cleared 1: DCDC2 Over Current Event detected
ACK_UVLO	Under Voltage Sense Acknowledgement 0: Cleared 1: Under Voltage Event detected
ACK_ILDO3	LDO3 Over Current Sense Acknowledgement 0: Cleared 1: LDO3 Over Current Event detected
ACK_ILDO4	LDO4 Over Current Sense Acknowledgement 0: Cleared 1: LDO4 Over Current Event detected
ACK_WNRG	Thermal Warning Sense Acknowledgement 0: Cleared 1: Thermal Warning Event detected
ACK_TSD	Thermal Shutdown Sense Acknowledgement 0: Cleared 1: Thermal Shutdown Event detected

Table 22. INT_SEN1 REGISTER

Name: INT_SEN1				Address: 0x02			
Type: R				Default: 0x00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
SEN_ENLDO4	SEN_ENLDO3	SEN_PG_LDO4	SEN_PG_LDO3	SEN_ENDCDC2	SEN_ENDCDC1	SEN_PG_DCDC2	SEN_PG_DCDC1

Table 23. BIT DESCRIPTION OF INT_SEN1 REGISTER

Bit	Bit Description
SEN_PG_DCDC1	DCDC1 Power Good Sense 0: DCDC1 Output Voltage below target 1: DCDC1 Output Voltage within nominal range
SEN_PG_DCDC2	DCDC2 Power Good Sense 0: DCDC2 Output Voltage below target 1: DCDC2 Output Voltage within nominal range
SEN_ENDCDC1	ENDCDC1 pin Sense 0: ENDCDC1 pin is low 1: ENDCDC1 pin is high
SEN_ENDCDC2	ENDCDC2 pin Sense 0: ENDCDC2 pin is low 1: ENDCDC2 pin is high
SEN _PG_LDO3	LDO3 Power Good Sense 0: LDO3 Output Voltage below target 1: LDO3 Output Voltage within nominal range
SEN _PG_LDO4	LDO4 Power Good Sense 0: LDO4 Output Voltage below target 1: LDO4 Output Voltage within nominal range
SEN_ENLDO3	ENLDO3 pin Sense 0: ENLDO3 pin is low 1: ENLDO3 pin is high
SEN_ENLDO4	ENLDO4 pin Sense 0: ENLDO4 pin is low 1: ENLDO4 pin is high

Table 24. INT_SEN2 REGISTER

Name: INT_SEN2				Address: 0x03			
Type: R				Default: 0x00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
SEN_TSD	SEN_WNRG	SEN_ILDO4	SEN_ILDO3	spare=0	SEN_UVLO	SEN_IDCDC2	SEN_IDCDC1

Table 25. BIT DESCRIPTION OF INT_SEN2 REGISTER

Bit	Bit Description
SEN _IDCDC1	DCDC1 Over Current Sense 0: DCDC1 Output Current below limit 1: DCDC1 Output Current over limit
SEN _IDCDC2	DCDC2 Over Current Sense 0: DCDC2 Output Current below limit 1: DCDC2 Output Current over limit
SEN _UVLO	Under Voltage Sense 0: Input Voltage higher than UVLO threshold 1: Input Voltage lower than UVLO threshold
SEN _ILDO3	LDO3 Over Current Sense 0: LDO3 Output Current below limit 1: LDO3 Output Current over limit
SEN _ILDO4	LDO4 Over Current Sense 0: LDO4 Output Current below limit 1: LDO4 Output Current over limit
SEN _WNRG	Thermal Warning Sense 0: Junction temperature below thermal warning limit 1: Junction temperature over thermal warning limit
SEN _TSD	Thermal Shutdown Sense 0: Junction temperature below thermal shutdown limit 1: Junction temperature over thermal shutdown limit

Table 26. RESET REGISTER

Name: RESET				**Address: 0x10**			
Type: RW				**Default: 0x10**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
FORCERST	spare=0	spare=0	RSTSTATUS	spare=0	spare=0	REARM	

Table 27. BIT DESCRIPTION OF RESET REGISTER

Bit	Bit Description
REARM[1:0]	Rearming of device after TSD 00: Re−arming active after TSD with reset of I^2C registers: new power−up sequence is initiated with default I^2C registers values (default) 01: Re−arming active after TSD with no reset of I^2C registers: new power−up sequence is initiated with I^2C registers values 10: No re−arming after TSD 11: N / A
RSTSTATUS	Reset Indicator Bit 0: Must be written to 0 after register reset 1: Default (loaded after Registers reset)
FORCERST	Force Reset Bit 0: Default 1: Force reset of internal registers to default

Table 28. PID (Product Identification) REGISTER

Name: PID				**Address: 0x11**			
Type: R				**Default: 0x0C**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PID7	PID6	PID5	PID4	PID3	PID2	PID1	PID0

Table 29. RID/FID: (Revision Identification / Features Identification) REGISTER

Name: RID/FID				Address: 0x12			
Type: R				Default: see register map			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RID3	RID2	RID1	RID0	FID3	FID2	FID1	FID0

Table 30. BIT DESCRIPTION OF RID/FID REGISTER

Bit	Bit Description
RID[3:0]	Revision Identification 0001: Pass 1.0 0010: Pass 1.1 0011: Production
FID[3:0]	Feature identification Pass 0.0 (first prototype : NCP6924C) 0000 Pass 1.x 1011: NCP6922CB 1100: NCP6922CC 1101: NCP6922CD

Table 31. ENABLE REGISTER

Name: ENABLE				Address: 0x14			
Type: RWM				Default: see register map			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
ENLDO4	ENLDO3	spare = 0	spare=0	ENDCDC2	MODEDCDC2	ENDCDC1	MODEDCDC1

Table 32. BIT DESCRIPTION OF ENABLE REGISTER

Bit	Bit Description
MODEDCDC1	DCDC1 Operating Mode 0: Auto switching PFM / PWM 1: Forced PWM (default)
ENDCDC1	DCDC1 Enabling 0: Disabled 1: Enabled
MODEDCDC2	DCDC2 Operating Mode 0: Auto switching PFM / PWM 1: Forced PWM (default)
ENDCDC2	DCDC2 Enabling 0: Disabled 1: Enabled
ENLDO3	LDO3 Enabling 0: Disabled 1: Enabled
ENLDO4	LDO4 Enabling 0: Disabled 1: Enabled

Table 33. DIS REGISTER

Name: DIS				Address: 0x15			
Type: RW				Default: 0x33			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
spare=0	spare=0	DISLDO4	DISLDO3	spare=0	spare=0	DISDCDC2	DISDCDC1

Table 34. BIT DESCRIPTION OF DIS REGISTER

Bit	Bit Description
DISDCDC1	DCDC1 Active Output Discharge 0: Disabled 1: Enabled
DISDCDC2	DCDC2 Active Output Discharge 0: Disabled 1: Enabled
DISLDO3	LDO3 Active Output Discharge 0: Disabled 1: Enabled
DISLDO4	LDO4 Active Output Discharge 0: Disabled 1: Enabled

Table 35. PGOOD1 REGISTER

Name: PGOOD1				**Address: 0x16**			
Type: RW				**Default: 0x42**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare=0	PGASSIGN_ RST	PGASSIGN_ LDO4	PGASSIGN_ LDO3	PGASSIGN_ DVS2	PGASSIGN_ DVS1	PGASSIGN_ DCDC2	PGASSIGN_ DCDC1

Table 36. BIT DESCRIPTION OF PGOOD1 REGISTER

Bit	Bit Description
PGASSIGN_DCDC1	DCDC1 Power Good Assignment 0: Not assigned 1: Assigned to PG pin
PGASSIGN_DCDC2	DCDC2 Power Good Assignment 0: Not assigned 1: Assigned to PG pin
PGASSIGN_DVS1	DCDC1 DVS Assignment 0: Not assigned 1: Assigned to PG pin
PGASSIGN_DVS2	DCDC2 DVS Assignment 0: Not assigned 1: Assigned to PG pin
PGASSIGN_LDO3	LDO3 Power Good Assignment 0: Not assigned 1: Assigned to PG pin
PGASSIGN_LDO4	LDO4 Power Good Assignment 0: Not assigned 1: Assigned to PG pin
PGASSIGN_RST	Internal Reset Signal Assignment 0: Not assigned 1: Assigned to PG pin

Table 37. PGOOD2 REGISTER

Name: PGOOD2				**Address: 0x17**			
Type: RW				**Default: 0x02**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare=0	Spare=0	PGGATE_LDO4	PGGATE_LDO3	Spare=0	Spare=0	PGGATE_DCDC2	PGGATE_DCDC1

Table 38. BIT DESCRIPTION OF PGOOD2 REGISTER

Bit	Bit Description
PGGATE_DCDC1	DCDC1 Power Good Gating 0: DCDC1 state does not gate PG pin 1: DCDC1 state gates PG pin
PGGATE_DCDC2	DCDC2 Power Good Gating 0: DCDC2 state does not gate PG pin 1: DCDC2 state gates PG pin
PGGATE_LDO3	LDO3 Power Good Gating 0: LDO3 state does not gate PG pin 1: LDO3 state gates PG pin
PGGATE_LDO4	LDO4 Power Good Gating 0: LDO4 state does not gate PG pin 1: LDO4 state gates PG pin

Table 39. TIME REGISTER

Name: TIME				**Address: 0x18**			
Type: RW				**Default: 0x00**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
GO2	GO1	spare=0	DVS[1:0]		TOR[2:0]		

Table 40. BIT DESCRIPTION OF TIME REGISTER

Bit	Bit Description
TOR[2:0]	Power Good Out of Reset Delay Time (ms) 000: 0(default) 001: 8 010: 16 011: 32 100: 64 101: 128 110: 256 111: 512
DVS[1:0]	DVS Timing (μs) 00: 1.33 μs (default) 01: 2.67 μs 10: 5.33us 11: 10.67us
GO1	0: DCDC1 Output Voltage set to VPROGDCDC1[7:0] 1: DCDC1 Output Voltage set to VDVSDCDC1[7:0]
GO2	0: DCDC2 Output Voltage set to VPROGDCDC2[7:0] 1: DCDC2 Output Voltage set to VDVSDCDC2[7:0]

Table 41. SEQUENCER1 REGISTER

Name: SEQUENCER1				**Address: 0x19**			
Type: RW				**Default: see register map**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
spare=0	spare=0	DCDC2_T[2:0]			DCDC1_T[2:0]		

Table 42. SEQUENCER2 REGISTER

Name: SEQUENCER2				**Address: 0x1B**			
Type: RW				**Default: see register map**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
spare=0	spare=0	LDO4_T[2:0]			LDO3_T[2:0]		

Table 43. START−UP DELAY

LDOx_T[2:0] / DCDCx_T[2:0]	Start−up Delay
000	T0
001	T1
010	T2
011	T3
100	T4
101	T5
110	T6
111	T7

Table 44. VPROGDCDC1[7:0] REGISTER

Name: VPROGDCDC1				Address: 0x20			
Type: RW				Default: see register map			
D7	D6	D5	D4	D3	D2	D1	D0
VPROGDCDC1[7:0]							

Table 45. VDVSDCDC1[7:0] REGISTER

Name: VDVSDCDC1				Address: 0x21			
Type: RW				Default: see register map			
D7	D6	D5	D4	D3	D2	D1	D0
VDVSDCDC1[7:0]							

Table 46. VPROGDCDC2[7:0] REGISTER

Name: VPROGDCDC2				Address: 0x22			
Type: RW				Default: see register map			
D7	D6	D5	D4	D3	D2	D1	D0
VPROGDCDC2[7:0]							

Table 47. VDVSDCDC2[7:0] REGISTER

Name: VDVSDCDC2				Address: 0x23			
Type: RW				Default: see register map			
D7	D6	D5	D4	D3	D2	D1	D0
VDVSDCDC2[7:0]							

Table 48. VPROGDCDCx[7:0] and VDVSDCDCx[7:0] BIT DESCRIPTION

Bit[7:0]	V_{OUT}(V)	Bit [7:0]	V_{OUT}(V)	Bit [7:0]	V_{OUT}(V)	Bit [7:0]	V_{OUT}(V)
0x00	0.6000	0x40	1.4000	0x80	2.2000	0xC0	3.0000
0x01	0.6125	0x41	1.4125	0x81	2.2125	0xC1	3.0125
0x02	0.6250	0x42	1.4250	0x82	2.2250	0xC2	3.0250
0x03	0.6375	0x43	1.4375	0x83	2.2375	0xC3	3.0375
0x04	0.6500	0x44	1.4500	0x84	2.2500	0xC4	3.0500
0x05	0.6625	0x45	1.4625	0x85	2.2625	0xC5	3.0625
0x06	0.6750	0x46	1.4750	0x86	2.2750	0xC6	3.0750
0x07	0.6875	0x47	1.4875	0x87	2.2875	0xC7	3.0875
0x08	0.7000	0x48	1.5000	0x88	2.3000	0xC8	3.1000
0x09	0.7125	0x49	1.5125	0x89	2.3125	0xC9	3.1125
0x0A	0.7250	0x4A	1.5250	0x8A	2.3250	0xCA	3.1250
0x0B	0.7375	0x4B	1.5375	0x8B	2.3375	0xCB	3.1375
0x0C	0.7500	0x4C	1.5500	0x8C	2.3500	0xCC	3.1500
0x0D	0.7625	0x4D	1.5625	0x8D	2.3625	0xCD	3.1625
0x0E	0.7750	0x4E	1.5750	0x8E	2.3750	0xCE	3.1750
0x0F	0.7875	0x4F	1.5875	0x8F	2.3875	0xCF	3.1875
0x10	0.8000	0x50	1.6000	0x90	2.4000	0xD0	3.2000
0x11	0.8125	0x51	1.6125	0x91	2.4125	0xD1	3.2125
0x12	0.8250	0x52	1.6250	0x92	2.4250	0xD2	3.2250
0x13	0.8375	0x53	1.6375	0x93	2.4375	0xD3	3.2375
0x14	0.8500	0x54	1.6500	0x94	2.4500	0xD4	3.2500
0x15	0.8625	0x55	1.6625	0x95	2.4625	0xD5	3.2625
0x16	0.8750	0x56	1.6750	0x96	2.4750	0xD6	3.2750
0x17	0.8875	0x57	1.6875	0x97	2.4875	0xD7	3.2875
0x18	0.9000	0x58	1.7000	0x98	2.5000	0xD8	3.3000
0x19	0.9125	0x59	1.7125	0x99	2.5125	0xD9	3.3000
0x1A	0.9250	0x5A	1.7250	0x9A	2.5250	0xDA	3.3000
0x1B	0.9375	0x5B	1.7375	0x9B	2.5375	0xDB	3.3000
0x1C	0.9500	0x5C	1.7500	0x9C	2.5500	0xDC	3.3000
0x1D	0.9625	0x5D	1.7625	0x9D	2.5625	0xDD	3.3000
0x1E	0.9750	0x5E	1.7750	0x9E	2.5750	0xDE	3.3000
0x1F	0.9875	0x5F	1.7875	0x9F	2.5875	0xDF	3.3000
0x20	1.0000	0x60	1.8000	0xA0	2.6000	0xE0	3.3000
0x21	1.0125	0x61	1.8125	0xA1	2.6125	0xE1	3.3000
0x22	1.0250	0x62	1.8250	0xA2	2.6250	0xE2	3.3000
0x23	1.0375	0x63	1.8375	0xA3	2.6375	0xE3	3.3000
0x24	1.0500	0x64	1.8500	0xA4	2.6500	0xE4	3.3000
0x25	1.0625	0x65	1.8625	0xA5	2.6625	0xE5	3.3000
0x26	1.0750	0x66	1.8750	0xA6	2.6750	0xE6	3.3000
0x27	1.0875	0x67	1.8875	0xA7	2.6875	0xE7	3.3000
0x28	1.1000	0x68	1.9000	0xA8	2.7000	0xE8	3.3000
0x29	1.1125	0x69	1.9125	0xA9	2.7125	0xE9	3.3000

Table 48. VPROGDCDCx[7:0] and VDVSDCDCx[7:0] BIT DESCRIPTION

Bit[7:0]	V_{OUT}(V)	Bit [7:0]	V_{OUT}(V)	Bit [7:0]	V_{OUT}(V)	Bit [7:0]	V_{OUT}(V)
0x2A	1.1250	0x6A	1.9250	0xAA	2.7250	0xEA	3.3000
0x2B	1.1375	0x6B	1.9375	0xAB	2.7375	0xEB	3.3000
0x2C	1.1500	0x6C	1.9500	0xAC	2.7500	0xEC	3.3000
0x2D	1.1625	0x6D	1.9625	0xAD	2.7625	0xED	3.3000
0x2E	1.1750	0x6E	1.9750	0xAE	2.7750	0xEE	3.3000
0x2F	1.1875	0x6F	1.9875	0xAF	2.7875	0xEF	3.3000
0x30	1.2000	0x70	2.0000	0xB0	2.8000	0xF0	3.3000
0x31	1.2125	0x71	2.0125	0xB1	2.8125	0xF1	3.3000
0x32	1.2250	0x72	2.0250	0xB2	2.8250	0xF2	3.3000
0x33	1.2375	0x73	2.0375	0xB3	2.8375	0xF3	3.3000
0x34	1.2500	0x74	2.0500	0xB4	2.8500	0xF4	3.3000
0x35	1.2625	0x75	2.0625	0xB5	2.8625	0xF5	3.3000
0x36	1.2750	0x76	2.0750	0xB6	2.8750	0xF6	3.3000
0x37	1.2875	0x77	2.0875	0xB7	2.8875	0xF7	3.3000
0x38	1.3000	0x78	2.1000	0xB8	2.9000	0xF8	3.3000
0x39	1.3125	0x79	2.1125	0xB9	2.9125	0xF9	3.3000
0x3A	1.3250	0x7A	2.1250	0xBA	2.9250	0xFA	3.3000
0x3B	1.3375	0x7B	2.1375	0xBB	2.9375	0xFB	3.3000
0x3C	1.3500	0x7C	2.1500	0xBC	2.9500	0xFC	3.3000
0x3D	1.3625	0x7D	2.1625	0xBD	2.9625	0xFD	3.3000
0x3E	1.3750	0x7E	2.1750	0xBE	2.9750	0xFE	3.3000
0x3F	1.3875	0x7F	2.1875	0xBF	2.9875	0xFF	3.3000

Table 49. VPROGLDO3[5:0] REGISTER

Name: VPROGLDO3				**Address: 0x26**			
Type: RW				**Default: see register map**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
spare=0	spare=0	VPROGLDO3[5:0]					

Table 50. VPROGLDO4[5:0] REGISTER

Name: VPROGLDO4				**Address: 0x27**			
Type: RW				**Default: see register map**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
spare=0	spare=0	VPROGLDO4[5:0]					

Table 51. VPROGLDOx[5:0] BIT DESCRIPTION

VPROGLDOx [5:0]	V_{OUT}(V)	VPROGLDOx [5:0]	V_{OUT}(V)	VPROGLDOx [5:0]	V_{OUT}(V)	VPROGLDOx [5:0]	V_{OUT}(V)
0x00	1.00	0x10	1.80	0x20	2.60	0x30	3.30
0x01	1.05	0x11	1.85	0x21	2.65	0x31	3.30
0x02	1.10	0x12	1.90	0x22	2.70	0x32	3.30
0x03	1.15	0x13	1.95	0x23	2.75	0x33	3.30
0x04	1.20	0x14	2.00	0x24	2.80	0x34	3.30
0x05	1.25	0x15	2.05	0x25	2.85	0x35	3.30
0x06	1.30	0x16	2.10	0x26	2.90	0x36	3.30
0x07	1.35	0x17	2.15	0x27	2.95	0x37	3.30
0x08	1.40	0x18	2.20	0x28	3.00	0x38	3.30
0x09	1.45	0x19	2.25	0x29	3.05	0x39	3.30
0x0A	1.50	0x1A	2.30	0x2A	3.10	0x3A	3.30
0x0B	1.55	0x1B	2.35	0x2B	3.15	0x3B	3.30
0x0C	1.60	0x1C	2.40	0x2C	3.20	0x3C	3.30
0x0D	1.65	0x1D	2.45	0x2D	3.25	0x3D	3.30
0x0E	1.70	0x1E	2.50	0x2E	3.30	0x3E	3.30
0x0F	1.75	0x1F	2.55	0x2F	3.30	0x3F	3.30

APPLICATION INFORMATION

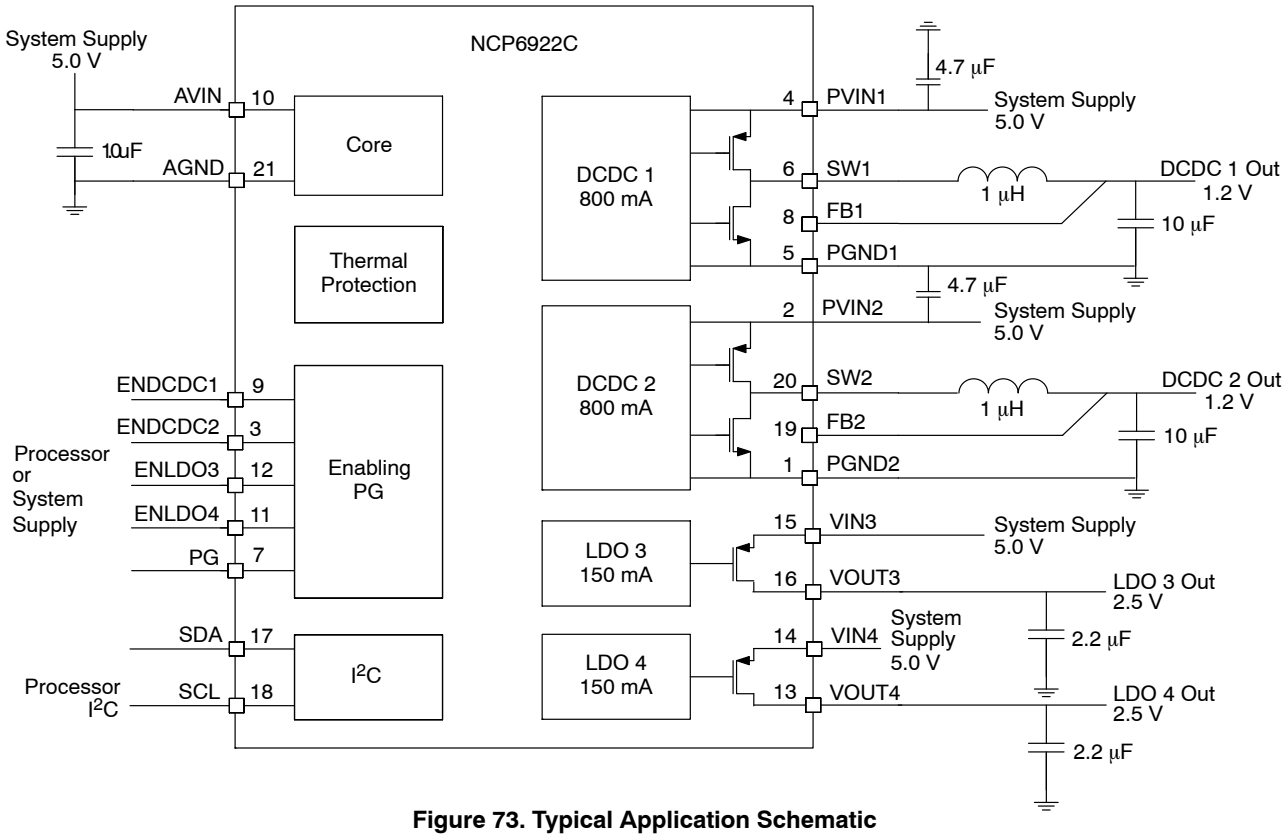


Figure 73. Typical Application Schematic

Inductor Selection

NCP6922C DC−to−DC converters typically use 1 μH inductor. Use of different values can be considered to optimize operation in specific conditions. The inductor parameters directly related to device performances are saturation current, DC resistance and inductance value. The inductor ripple current (ΔIL) decreases with higher inductance.

$$\Delta I_L = V_O \times \frac{1 - \frac{V_O}{V_{IN}}}{L \times F_{SW}} \quad \text{(eq. 1)}$$

$$I_{LMAX} = I_{OMAX} + \frac{\Delta I_L}{2} \quad \text{(eq. 2)}$$

With:

- Fsw = Switching Frequency (Typical 3 MHz)
- L = Inductor value
- ΔI_L = Peak−To−Peak inductor ripple current
- I_{LMAX} = Maximum Inductor Current

To achieve better efficiency, ultra low DC resistance inductor should be selected.

The saturation current of the inductor should be higher than the ILMAX calculated with the Equations 1 and 2.

Table 52. INDUCTOR L = 1.0 μH

Supplier	Part #	Size (mm) (L x l x T)	DC Rated Current (A)	DCR Max at 25°C (mΩ)
TDK	SPM3012T−1R0M	3.2 x 3.0 x 1.2	3.4	65
TDK	TFM252010A−1R0M	2.5 x 2.0 x 1.0	3.5	65
TDK	TFM201610A−1R0M	2.0 x 1.6 x 1.0	2.5	75
MURATA	LQH44PN−1R0NP0	4.0 x 3.5 x 1.8	2.5	36
MURATA	LQM2HPN−1R0MG0	2.5 x 2.0 x 1.0	1.6	69
TOKO	DFE252012C−1R0N	2.5 x 2.0 x 1.2	3.0	59

Table 53. INDUCTOR L = 2.2 μH

Supplier	Part #	Size (mm) (L x l x T)	DC Rated Current (A)	DCR Max at 25°C (mΩ)
TDK	SPM3012T−2R2M	3.2 x 3.0 x 1.2	2.5	115
TDK	TFM252010A−2R2M	2.5 x 2.0 x 1.0	2.3	115
TDK	TFM201610A−2R2M	2.0 x 1.6 x 1.0	1.7	200
MURATA	LQH44PN−1R0NP0	4.0 x 3.5 x 1.8	1.7	96
MURATA	LQM2HPN−2R2MG0	2.5 x 2.0 x 1.0	1.3	100
TOKO	DFE252012C−2R2N	2.5 x 2.0 x 1.2	2.0	108

Output Capacitor Selection for DC−to−DC Converters

Selecting the proper output capacitor is based on the desired output ripple voltage. Ceramic capacitors with low ESR values will have the lowest output ripple voltage and are strongly recommended. The output capacitor requires either an X7R or X5R dielectric.

The output ripple voltage in PWM mode can be estimated by:

$$\Delta V_O = V_O \times \frac{1 - \frac{V_O}{V_{IN}}}{L \times F_{SW}} \times \left(\frac{1}{2 \times \pi \times C_O \times F_{SW}} + ESR \right) \quad \text{(eq. 3)}$$

Table 54. RECOMMENDED OUTPUT CAPACITOR FOR DC−to−DC CONVERTERS

Manufacturer	Part Number	Case Size	HeightTyp. [mm]	C [μF]
MURATA	GRM188R60J106ME47	0603	0.8	10
MURATA	GRM219R60J106KE19	0805	1.25	10
MURATA	GRM21BR60J226ME39	0805	1.25	22
TDK	C1608X5R0C106K/M	0603	0.8	10
TDK	C2012X5R0C106K/M	0805	1.25	10
TDK	C2012X5R0C226K/M	0805	1.25	22

Input Capacitor Selection for DCDC Converters

In PWM operating mode, the input current is pulsating with large switching noise. Using an input bypass capacitor can reduce the peak current transients drawn from the input supply source, thereby reducing switching noise significantly.

The maximum RMS current occurs at 50% duty cycle with maximum output current, which is 1/2 of maximum output current. A low profile ceramic capacitor of 4.7 μF should be used for most of the cases. For effective bypass results, the input capacitor should be placed as close as possible to PVIN1 and PVIN2 pins.

Table 55. RECOMMENDED INPUT CAPACITOR FOR DC−to−DC CONVERTERS

Supplier	Part Number	CaseSize	Height Typ. [mm]	C [μF]
MURATA	GRM188R60J475KE	0603	0.8	4.7
MURATA	GRM188R60J106ME	0603	0.8	10
TDK	C1608X5R0C475K/M	0603	0.8	4.7
TDK	C1608X5R0C106K/M	0603	0.8	10

Output Capacitor for LDOs

For stability reason, a typical 2.2 μF ceramic output capacitor is suitable for LDOs. The LDO output capacitor should be placed as close as possible to the NCP6922C output pin.

Input Capacitor for LDOs

NCP6922C LDOs do not require specific input capacitor. However, a typical 1 μF ceramic capacitor placed close to LDOs' input is helpful for load transient.

Power input of LDO can be connected to main power supply. However, for optimum efficiency and lower NCP6922C thermal dissipation, lowest voltage available in the system is preferred. Input voltage of LDO, should always be higher than VOUT + VLDODROP (VDROP, LDO dropout voltage at maximum current).

Capacitor DC Bias Characteristics

Real capacitance of ceramic capacitor changes versus DC voltage. Special care should be taken to DC bias effect in order to make sure that the real capacitor value is always higher than the minimum allowable capacitor value specified.

PCB layout Recommendation

The high speed operation of the NCP6922C demands careful attention to board layout and component placement. To prevent electromagnetic interference (EMI) problems and reduce voltage ripple of the device, any high current copper trace which see high frequency switching should be optimized. Therefore, use short and wide traces for power current paths and for power ground tracks, power plane and ground plane are recommended if possible.

Both the inductor and input/output capacitor of DC−to−DC converters are in the high frequency switching path where current flow may be discontinuous. These components should be placed as close to NCP6922C as possible to reduce parasitic inductance connection. Also it is important to minimize the area of the switching nodes and use the ground plane under them to minimize cross−talk to sensitive signals and ICs. It's suggested to keep as complete ground plane under NCP6922C as possible.

PGND and AGND pin connection must be connected to the ground plane. Care should be taken to avoid noise interference between PGND and AGND.

It is always good practice to keep the sensitive tracks such as feedback connection (FB1 / FB2) away from switching signal connections (SW1 / SW2) by laying the tracks on the other side or inner layers of PCB.

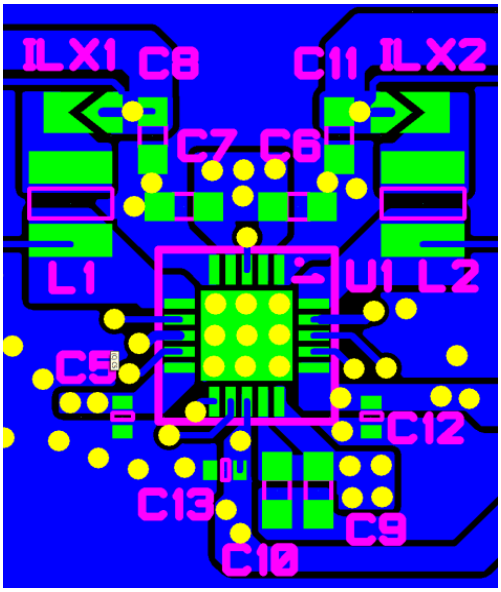


Figure 74. Recommended PCB Layout

Thermal Considerations

Careful attention must be paid to the power dissipation of the NCP6922C. The power dissipation is a function of efficiency and output power. Hence, increasing the output power requires better components selection. Care should be taken of LDO VDROP, the larger it is, the higher dissipation it will bring to NCP6922C. Keep large copper plane under and close to NCP6922C is helpful for thermal dissipation.

ORDERING INFORMATION

Device	Marking	Comment	Package	Shipping†
NCP6922CBMTTXG	6922CB	2 x 800 mA DCDC 2 x 150 mA LDO I²C address 0010 100x (See detailed description)	WQFN – 4 x 4mm (Pb – Free)	3000 / Tape & Reel
NCP6922CCMTTXG	6922CC	2 x 800 mA DCDC 2 x 150 mA LDO I²C address 0011 000x (See detailed description)	WQFN – 4 x 4mm (Pb – Free)	3000 / Tape & Reel
NCP6922CDMTTXG	6922CD	2 x 800 mA DCDC 2 x 150 mA LDO I²C address 0011 000x (See detailed description)	WQFN – 4 x 4mm (Pb – Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Demo board available:

- The NCP6922CGEVB/D evaluation board configures the device in typical application to supply constant voltage.

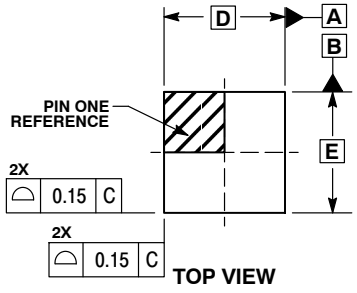
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

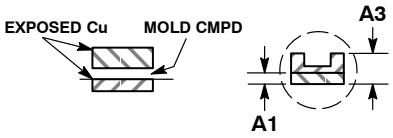
WQFN20, 4x4, 0.5P
CASE 510AV−01
ISSUE O

DATE 22 JUN 2011

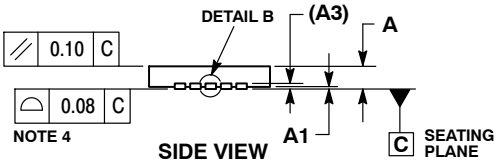
SCALE 2:1



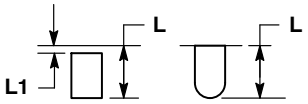
TOP VIEW



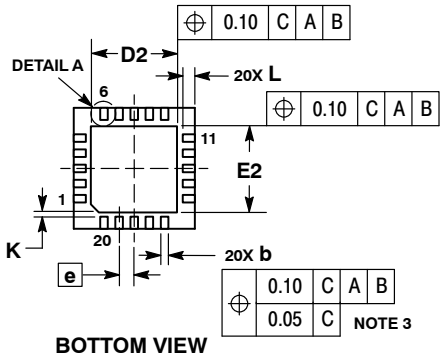
DETAIL B
ALTERNATE CONSTRUCTIONS



SIDE VIEW



DETAIL A
ALTERNATE CONSTRUCTIONS

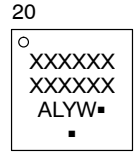


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	4.00 BSC	
D2	2.60	2.80
E	4.00 BSC	
E2	2.60	2.80
e	0.50 BSC	
K	0.20 REF	
L	0.30	0.50
L1	0.00	0.15

GENERIC MARKING DIAGRAM*

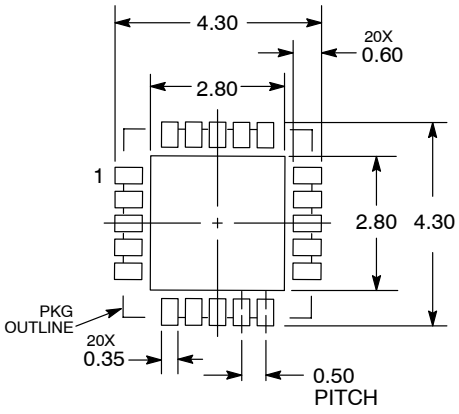


XXXXXX= Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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