# NCP5425

# Dual Synchronous Buck Controller

The NCP5425 is a highly flexible dual buck controller with internal gate drivers that can be used with two input power supplies and one or two outputs in multiple configurations. The part contains all the circuitry required for two independent synchronous dual NFET buck regulators utilizing a feed forward voltage mode control method. The NCP5425 can run from a single supply ranging from 4.6 to 12 V and support a single two phase or dual single phase outputs. When used as a dual output controller, the second output tracks voltage transients from the first. Power blanking for low noise applications is supported as well as independent cycle−by−cycle current limiting. The part is available in a 20 pin TSSOP package allowing the designer to minimize PCB area.

### Features

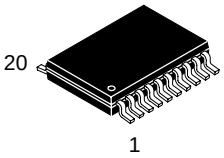
- Operation Over 4.6 to 13.2 V
- Dual Synchronous Buck Design
- Configurable as a Single Two Phase Output or Two Single Phase Outputs
- Programmable Power Sharing and Budgeting from Two Independent Supplies
- 0.8 V ±1% Reference for Low Voltage Outputs
- 1.5 A Peak Power Drive
- Switch Blanking for Noise Sensitive Applications through use of $R_{OSC}$ Pin
- Programmable Frequency, 150 kHz to 750 kHz Operation
- Programmable Soft−Start
- Cycle−by−Cycle Overcurrent Protection
- Independent Programmable Current Limits
- 100% Duty Cycle for Fast Transient Response
- Internal Slope Compensation
- Out−of−Phase Synchronization between the Controllers
- Input Undervoltage Lockout
- On/Off Enable through use of the COMP Pins
- Power Supply Sequencing
- These are Pb−Free Devices

### Applications

- DDR Memory Power
- Graphics Cards

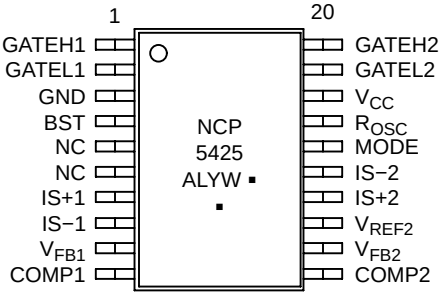
**ON Semiconductor®**

**http://onsemi.com**




**TSSOP−20**
**DB SUFFIX**
**CASE 948E**

**PIN CONNECTIONS AND MARKING DIAGRAM**




A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NCP5425DB | TSSOP−20* | 75 Units/Tube |
| NCP5425DBG | TSSOP−20* | 75 Units/Tube |
| NCP5425DBR2 | TSSOP−20* | 2500/Tape & Reel |
| NCP5425DBR2G | TSSOP−20* | 2500/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.
*This package is inherently Pb−Free.

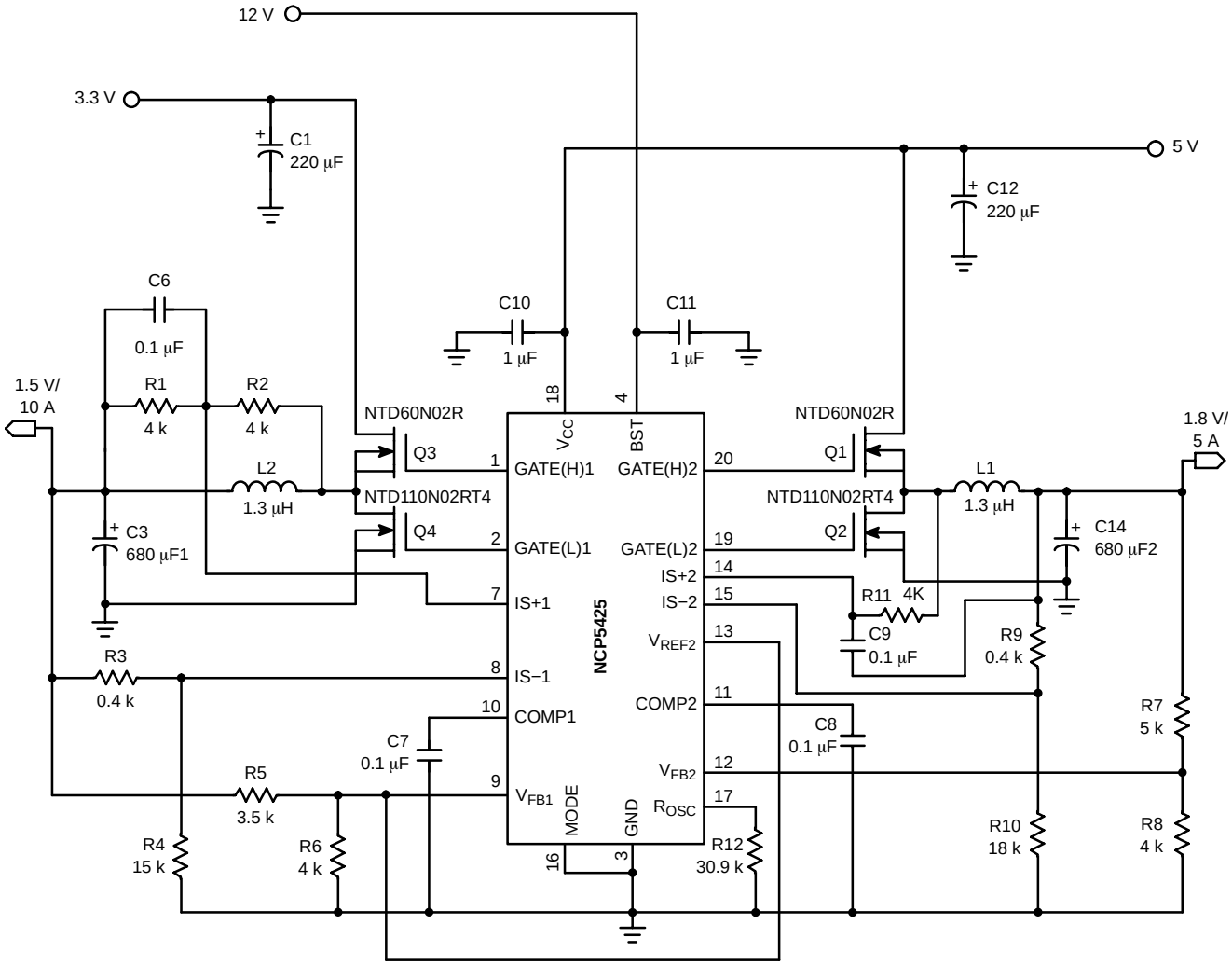



**Figure 1. Application Diagram, 3.3 V to 1.5 V/10 A and 1.8 V/5.0 A Converter**

**MAXIMUM RATINGS**

| Rating | Value | Unit |
|---|---|---|
| Operating Junction Temperature, $T_J$ | 150 | °C |
| Storage Temperature Range, $T_J$ | −65 to 150 | °C |
| ESD Susceptibility (Human Body Model) | 2.0 | kV |
| ESD Susceptibility (Machine Model) | 200 | V |
| Thermal Resistance, Junction−to−Air | 140 | °C/W |
| Moisture Sensitivity Level (MSL) | 1 | |
| Lead Temperature Soldering: Reflow: (Note 1) | 260 peak | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. 60 to 150 seconds maximum above 183°C, 260°C peak.

**MAXIMUM RATINGS**

| Pin Symbol | Pin Name | $V_{MAX}$ | $V_{MIN}$ | $I_{SOURCE}$ | $I_{SINK}$ |
|---|---|---|---|---|---|
| $V_{CC}$ | IC Power Input | 16 V | −0.3 V | N/A | 2.0 A Peak<br>200 mA DC |
| COMP1, COMP2 | Compensation Capacitor for Channel 1 or 2 | 4.0 V | −0.3 V | 1.0 mA | 1.0 mA |
| $V_{FB1}$, $V_{FB2}$, $V_{REF2}$ | Voltage Feedback Input for Channel 1 or 2 | 6.0 V | −0.3 V | 1.0 mA | 1.0 mA |
| $R_{OSC}$ | Oscillator Resistor | 5.0 V | −0.3 V | 1.0 mA | 1.0 mA |
| GATE(H)1, GATE(H)2 | High−Side FET Driver for Channel 1 or 2 | 20 V | −0.3 V | 2.0 A Peak<br>200 mA DC | 2.0 A Peak<br>200 mA DC |
| GATE(L)1, GATE(L)2 | Low−Side FET Driver for Channel 1 or 2 | 16 V | −0.3 V | 2.0 A Peak<br>200 mA DC | 2.0 A Peak<br>200 mA DC |
| IS+1, IS+2 | Positive Current Sense for Channel 1 or 2 | 6.0 V | −0.3 V | 1.0 mA | 1.0 mA |
| IS−1, IS−2 | Negative Current Sense for Channel 1 or 2 | 6.0 V | −0.3 V | 1.0 mA | 1.0 mA |
| GND | Ground | 100 mV | 0 V | 2.0 A Peak<br>200 mA DC | N/A |
| BST | Power Input for GATE(H)1 GATE(H)2 | 23 V | −0.3 V | N/A | 2.0 A Peak<br>200 mA DC |
| MODE | Dual or Single Output Select | 3.5 V | −0.3 V | N/A | N/A |

**ELECTRICAL CHARACTERISTICS** ($0°C < T_J < 125°C$; $R_{OSC}$ = 30.9 k, $C_{COMP1,2}$ = 0.1 μF, 4.75 V < $V_{CC}$ < 13.2 V; 10.8 V < BST < 20 V, $C_{GATE(H)1,2} = C_{GATE(L)1,2}$ = 1.0 nF; unless otherwise specified.)

| Characteristic | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **ERROR AMPLIFIER** | | | | | |
| $V_{FB1}$ Input Bias Current | $V_{FB1}$ = 0 V | – | 0.1 | 1.0 | μA |
| $V_{FB2}$, $V_{REF2}$ Input Bias Current | $V_{FB2}$, $V_{REF2}$ = 0.8 V | – | 0.1 | 1.0 | μA |
| Common Mode Input Voltage Range | – | 0.3 | – | 1.0 | V |
| COMP1(2) Source Current | COMP1(2) = 1.2 V to 2.5 V; $V_{FB1(2)}$ = 0.6 V | 15 | 30 | 60 | μA |
| COMP1(2) Sink Current | COMP1(2) = 1.2 V; $V_{FB1(2)}$ = 1.0 V | 15 | 30 | 60 | μA |
| Reference Voltage | COMP1 = $V_{FB1}$ | 0.792 | 0.800 | 0.808 | V |
| COMP1 Max Voltage<br>COMP2 Max Voltage, Mode Floating<br>COMP2 Max Voltage, Mode = 0 | $V_{FB1(2)}$ = 0.6 V<br>$V_{FB1(2)}$ = 0.6 V<br>$V_{FB1(2)}$ = 0.6 V | –<br>3.0<br>– | 2.0<br>3.1<br>2.0 | 2.1<br>–<br>2.1 | V |
| COMP1(2) Min Voltage | $V_{FB1(2)}$ = 1.2 V | – | 0.10 | 0.20 | V |
| Open Loop Gain | | – | 95 | – | dB |
| Unity Gain Bandwidth | | – | 40 | – | kHz |
| PSRR @ 1.0 kHz | | – | 70 | – | dB |
| Transconductance | – | – | 32 | – | mmho |
| Output Impedance | – | – | 2.5 | – | MΩ |
| **GATE(H) AND GATE(L)** | | | | | |
| High Voltage (AC) | $V_{CC}$ − GATE(L)1,2<br>BST − GATE(H)1,2 (Note 2) | – | 0 | 0.5 | V |
| Low Voltage (AC) | GATE(L)1,2 or GATE(H)1,2 (Note 2) | – | 0 | 0.5 | V |
| Rise Time | 1.0 V < GATE(L)1,2 < $V_{CC}$ − 1.0 V<br>1.0 V < GATE(H)1,2 < BST − 1.0 V | – | 25 | 80 | ns |
| Fall Time | $V_{CC}$ − 1.0 > GATE(L)1,2 > 1.0 V<br>BST − 1.0 > GATE(H)1,2 > 1.0 V | – | 25 | 80 | ns |
| GATE(H) to GATE(L) Delay | GATE(H)1,2 < 2.0 V<br>GATE(L)1,2 > 2.0 V | 20 | 40 | 80 | ns |
| GATE(L) to GATE(H) Delay | GATE(L)1,2 < 2.0 V<br>GATE(H)1,2 > 2.0 V | 20 | 40 | 80 | ns |
| GATE(H)1(2) and GATE(L)1(2) Pull−Down | Resistance to GND (Note 2) | 50 | 125 | 280 | kΩ |
| **PWM COMPARATOR** | | | | | |
| Propagation Delay | COMP1(2) = 1.0 V<br>$V_{FB1(2)}$ = 0 to 1.2 V (Note 2) | – | 200 | 300 | ns |
| PWM Comparator Offset | $V_{FB1(2)}$ = 0 V; Increase COMP1(2) until GATE(H)1(2) starts switching | 0.20 | 0.30 | 0.45 | V |
| Artificial Ramp | Duty Cycle = 50% | 55 | 95 | 150 | mV |
| Minimum Pulse Width | (Note 2) | – | 80 | 130 | ns |

2. Guaranteed by design, not 100% tested in production.

**ELECTRICAL CHARACTERISTICS (continued)** ($0°C < T_J < 125°C$; $R_{OSC}$ = 30.9 k, $C_{COMP1,2}$ = 0.1 μF, 4.75 V < $V_{CC}$ < 13.2 V; 10.8 V < BST < 20 V, $C_{GATE(H)1,2} = C_{GATE(L)1,2}$ = 1.0 nF; unless otherwise specified.)

| Characteristic | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OSCILLATOR** | | | | | |
| Switching Frequency | $R_{OSC}$ = 61.9 k; Measure GATE(H)1 | 112 | 150 | 188 | kHz |
| Switching Frequency | $R_{OSC}$ = 30.9 k; Measure GATE(H)1 | 224 | 300 | 376 | kHz |
| Switching Frequency | $R_{OSC}$ = 11.8 k; Measure GATE(H)1 | 562 | 750 | 938 | kHz |
| $R_{OSC}$ Voltage | $R_{OSC}$ = 30.9 k | 0.970 | 1.000 | 1.030 | V |
| Phase Difference | – | – | 180 | – | ° |
| Low Noise Disable | Guaranteed By Design | – | 3.1 | 3.5 | V |
| **OVERCURRENT PROTECTION** | | | | | |
| OVC Comparator Offset Voltage | 0 V < IS+1(2) < 5.5 V<br>0 V < IS−1(2) < 5.5 V | 55 | 70 | 85 | mV |
| IS+1(2) Bias Current<br>IS−1(2) Bias Current | 0 V < IS+1(2) < 5.5 V<br>0 V < IS−1(2) < 5.5 V | −1.0<br>−1.0 | 0.1<br>0.1 | 1.0<br>1.0 | μA<br>μA |
| OVC Common Mode Range | – | 0 | – | 5.5 | V |
| **SUPPLY CURRENTS** | | | | | |
| $V_{CC}$ Current | COMP = 0 V (No Switching) | – | 16 | 22 | mA |
| BST Current | COMP = 0 V (No Switching) | – | 3.5 | 6.0 | mA |
| **UNDERVOLTAGE LOCKOUT** | | | | | |
| Start Threshold | GATE(H) Switching; COMP1(2) Charging | 3.8 | 4.2 | 4.6 | V |
| Stop Threshold | GATE(H) Not Switching; COMP1(2) Discharging | 3.6 | 4.0 | 4.4 | V |
| Hysteresis | Start−Stop | 0.1 | 0.2 | 0.45 | V |

**PIN FUNCTION DESCRIPTION**

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | GATE(H)1 | High Side Switch FET driver pin for the channel 1 FET. |
| 2 | GATE(L)1 | Low Side Synchronous FET driver pin for the channel 1 FET. |
| 3 | GND | Ground. All circuits are referenced to this pin. IC substrate connection. |
| 4 | BST | Power input for GATE(H)1 and GATE(H)2 pins. |
| 5 | NC | No connection. |
| 6 | NC | No connection. |
| 7 | IS+1 | Positive input for channel 1 overcurrent comparator. |
| 8 | IS−1 | Negative input for channel 1 overcurrent comparator. |
| 9 | $V_{FB1}$ | Error amplifier inverting input for channel 1. |
| 10 | COMP1 | Channel 1 Error Amp output. PWM comparator reference input. A capacitor to GND provides Error Amp compensation. The same capacitor provides soft−start timing for channel 1. This pin also disables the channel 1 output when pulled below 0.2 V. |
| 11 | COMP2 | Channel 2 Error Amp output. PWM comparator reference input. A capacitor to GND provides Error Amp compensation and soft−start timing for channel 2. Channel 2 output is disabled when this pin is pulled below 0.2 V. |
| 12 | $V_{FB2}$ | Error amplifier inverting input for channel 2. |
| 13 | $V_{REF2}$ | Error amplifier noninverting input for channel 2. |
| 14 | IS+2 | Positive input for channel 2 overcurrent comparator. |
| 15 | IS−2 | Negative input for channel 2 overcurrent comparator. |
| 16 | MODE | Input pin used to inform internal circuitry of dual output or single output operation. Ground this pin for dual output operation, leave open for single output operation. |
| 17 | $R_{OSC}$ | A resistor from this pin to ground sets switching frequency. |
| 18 | $V_{CC}$ | Input Power supply pin. Power input for GATE(L)1 and GATE(L)2 pins. |
| 19 | GATE(L)2 | Low Side Synchronous FET driver pin for the channel 2 FET. |
| 20 | GATE(H)2 | High Side Switch FET driver pin for the channel 2 FET. |

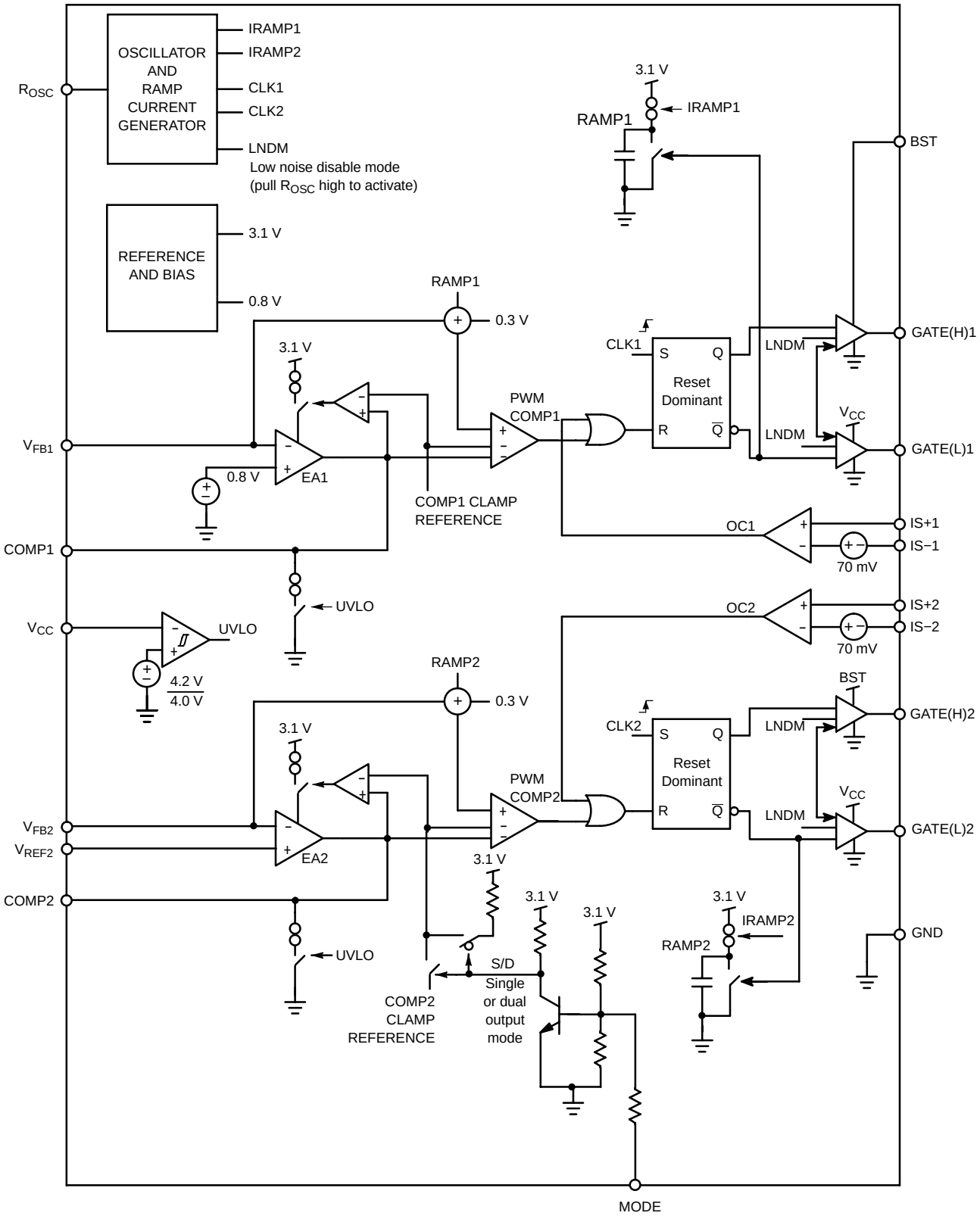



**Figure 2. Block Diagram**

## APPLICATIONS INFORMATION

### Theory of Operation

The NCP5425 is a very versatile buck controller using $V^{2\,™}$ control method. It can be configured as:

- Dual output Buck Controller.
- Two phase Buck Controller with current limit.
- Two phase Buck Controller with input power ratio and current limit.

The fixed−frequency architecture, driven from a common oscillator, ensures a 180° phase differential between channels.

#### $V^2$ Control Method

The $V^2$ method of control uses a ramp signal generated by the ESR (Effective Series Resistance) of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. The $V^2$ method differs from traditional techniques such as voltage mode control, which generates an artificial ramp, and current mode control, which generates a ramp using the inductor current.

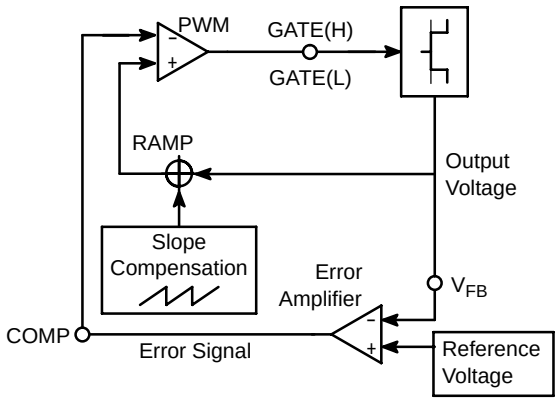



**Figure 3. $V^2$ Control with Slope Compensation**

The $V^2$ control method is illustrated in Figure 3. The output voltage generates both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output, regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, allowing the control circuit to drive the main switch to 0% or 100% duty cycle as required. A variation in line voltage changes the current ramp in the inductor, which causes the $V^2$ control scheme to compensate the duty cycle. Since any variation in inductor current modifies the ramp signal, as in current mode control, the $V^2$ control scheme offers the same advantages in line transient response. A variation in load current will affect the output voltage, modifying the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. The comparator response time and the transition speed of the main switch determine the load transient response. Unlike traditional control methods, the reaction time to the output load step is not related to the crossover frequency of the error signal loop. The error signal loop can have a low crossover frequency, since the transient response is handled by the ramp signal loop. The main purpose of this 'slow' feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered. Line and load regulation are drastically improved because there are two independent control loops. A voltage mode controller relies on the change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, the consequence of which is normally specified as line or load regulation. A current mode controller maintains a fixed error signal during line transients, since the slope of the ramp signal changes in this case. However, regulation of load transients still requires a change in the error signal. The $V^2$ method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.

The stringent load transient requirements of modern power supplies require the output capacitors to have very low ESR. The resulting shallow slope in the output ripple can lead to pulse width jitter and variation caused by both random and synchronous noise. A ramp waveform generated in the oscillator is added to the ramp signal from the output voltage to provide the proper voltage ramp at the beginning of each switching cycle. This slope compensation increases the noise immunity, particularly at higher duty cycle (above 50%).

#### Startup

The NCP5425 features a programmable soft−start function, which is implemented through the error amplifier and external compensation capacitor. This feature reduces stress to the power components and limits overshoot of the output voltage, during startup. As power is applied to the regulator, the NCP5425 Undervoltage Lockout circuit (UVLO) monitors the IC's supply voltage ($V_{CC}$). The UVLO circuit prevents the MOSFET gates from switching until $V_{CC}$ exceeds 4.2 V. Internal UVLO threshold hysteresis of 200 mV improves noise immunity. During startup, the external Compensation Capacitor connected to the COMP pin is charged by an internal 30 μA current source. When the capacitor voltage exceeds the 0.3 V offset of the PWM comparator, the PWM control loop will allow switching to occur. The upper gate driver GATE(H) is now activated, turning on the upper MOSFET. The output current then ramps up through the main inductor and linearly powers the output capacitors and load. When the regulator

output voltage exceeds the COMP pin voltage, minus the 0.3 V PWM comparator offset threshold and the artificial ramp, the PWM comparator terminates the initial pulse.

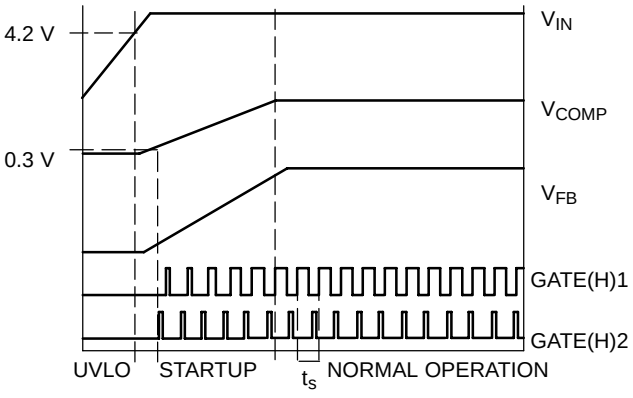



**Figure 4. Idealized Startup Waveforms**

### Normal Operation

During normal operation, the duty cycle remains approximately constant as the $V^2$ control loop maintains regulated output voltage under steady state conditions. Variations in supply line or output load conditions will result in changes in duty cycle to maintain regulation.

### Gate Charge Effect on Switching Times

When using the on board gate drivers, the gate charge has an important effect on the switching times of the FETs. A finite amount of time is required to charge the effective capacitor seen at the gate of the FET. Therefore, the rise and fall times rise linearly with increased capacitive loading, according to the following graphs.

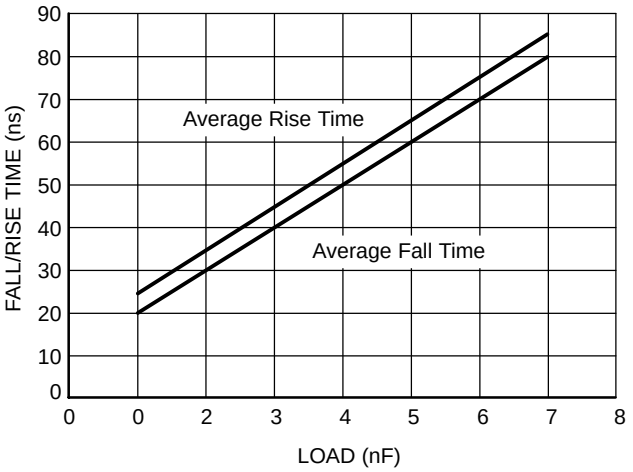



**Figure 5. Average Rise and Fall Times**

### Transient Response

The 200 ns reaction time of the control loop provides fast transient response to any variations in input voltage or output current. Pulse−by−pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed instantaneously, regulation is maintained by the output capacitors during the time required to slew the inductor current. For better transient response, a combination of several high frequency and bulk output capacitors are typically used.

### Out−of−Phase Synchronization

The turn−on of the second channel is delayed by half the switching cycle. This delay is supervised by the oscillator, which supplies a clock signal to the second channel that is 180° out of phase with the clock signal of the first channel. Advantages of out−of−phase synchronization are many. Since the input current pulses are interleaved with one another, the overlap time is reduced. Overlap reduction reduces the input filter requirement, allowing the use of smaller components. In addition, since peak current occurs during a shorter time period, emitted EMI is also reduced, potentially reducing shielding requirements. Interleaving the phases in a two phase application reduces ripple voltage and allows supplies with tighter tolerances to be built.

### Overvoltage Protection

Overvoltage Protection (OVP) is provided as a consequence of the normal operation of the $V^2$ control method, and requires no additional external components to implement. The control loop responds to an overvoltage condition within 200 ns, turning off the upper MOSFET and disconnecting the regulator from its input voltage. This results in a crowbar action to clamp the output voltage, preventing damage to the load. The regulator remains in this state until the overvoltage condition clears.

### Low Noise Disable Mode

A PWM converter operating at a constant frequency concentrates its noise output over a small frequency band. In noise−sensitive applications, this frequency can be chosen to prevent interference with other system functions. Some applications may have even more stringent requirements, where absolutely no noise may be emitted for a short period of time.

The user may disable the clock during noise sensitive periods to temporarily inhibit switching noise by disconnecting or pulling the $R_{OSC}$ pin to 3.3 V. This disables both gate drivers, leaving the switch node floating, and discharges the internal ramp.

The control circuitry remains enabled while the clock and drivers are disabled, so the COMP pins will charge up to a higher voltage. The COMP pins are clamped to prevent excessive overshoot when switching is resumed.

**Current Sharing**

When used in a two separate input to a single output mode, the NCP5425 dual controller can provide input power sharing in either of two ways:

- A preset ratio. For example, Channel 1 could provide 70% of the load current, and Channel 2, the remaining 30%. Practical ratios for Channel 1/Channel 2 contribution to total load current range from 50%−50% to 80%−20%.
- A preset ratio up to a specific current contribution from Channel 2. In excess of that limit, all of the additional load current would be supplied by Channel 1. Figure 7 depicts the actual performance of a NCP5425 configured in a 70%−30% share ratio, with Channel 2 output current limited to 5.0 Amps.

The availability both Channel 2 error amplifier inputs (signal and reference) at device pins is key to programmable current ratio sharing. Current sense information from Channel 1 is connected to the reference input of the Channel 2 error amplifier. Current information from Channel 2 is fed back to the error amplifier's inverting input. Channel 2 will therefore act to adjust its current to match the current information fed to its reference input from Channel 1. If this information is one−half the voltage developed across the Channel 1 output inductor, Channel 2 will run at half the current and supply a approximately 33% of the total load current. This application is illustrated in Figure 7.

In some applications the power supply designer may not only wish to draw a known percentage of power from one source, but also limit the power drawn from that source. The current limit amplifier on Channel 2 can be programmed to budget the maximum input power into Channel 2 and all power in excess of that limit will be supplied solely by Channel 1. This is accomplished by setting the Channel 2 cycle−by−cycle current limit in conjunction with programming the current ratio as described above.

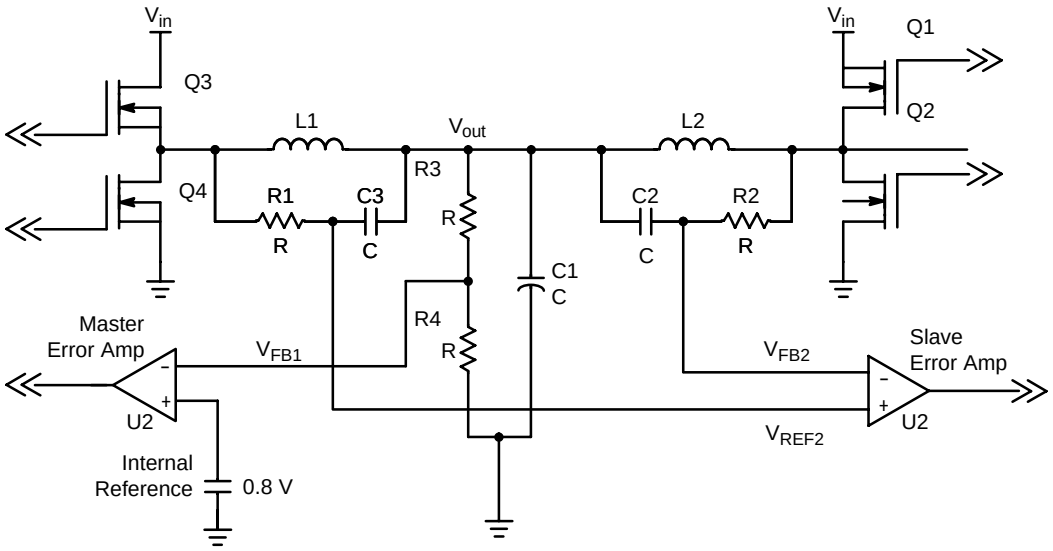



**Figure 6. Two Phase Current Sharing Circuit**

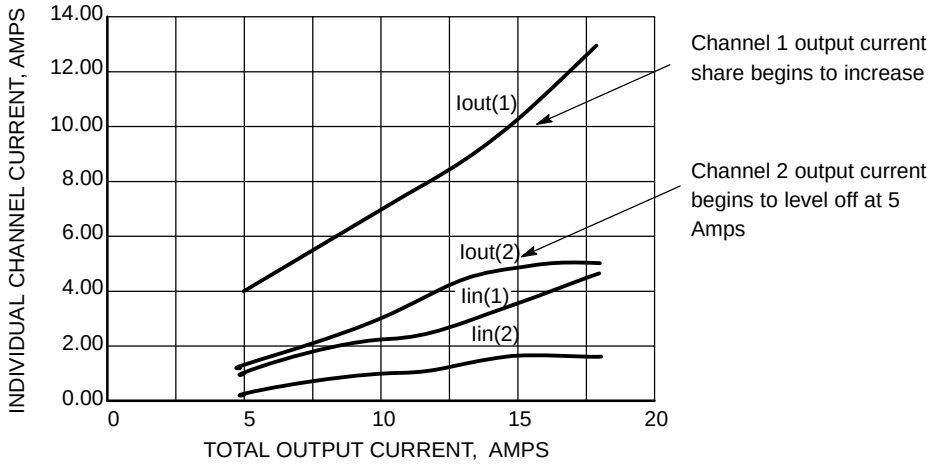



**Figure 7. 70%/30% Current Sharing with Channel 2 Current Limiting**

NOTE: Channel 1 input voltage = Channel 2 input voltage = 5.0 V
Output voltage = 1.5 V

**Inductor Current Sensing**

Examples of lossless current sensing across an output inductor are shown in Figure 8. Lx is the output inductance and Rx represents its equivalent series resistance. To compensate the current sense signal, the values of R1 and C1 are chosen so that Lx/Rx = R1 x C1. With these values, the current sense signal will have the same wave shape as the inductor current and the voltage signal on C1 will represent the instantaneous value of inductor current. The voltage across C1 can be used as though it were a sense resistor with the same value as the inductor's ESR, thus avoiding a sense resistor's power loss.

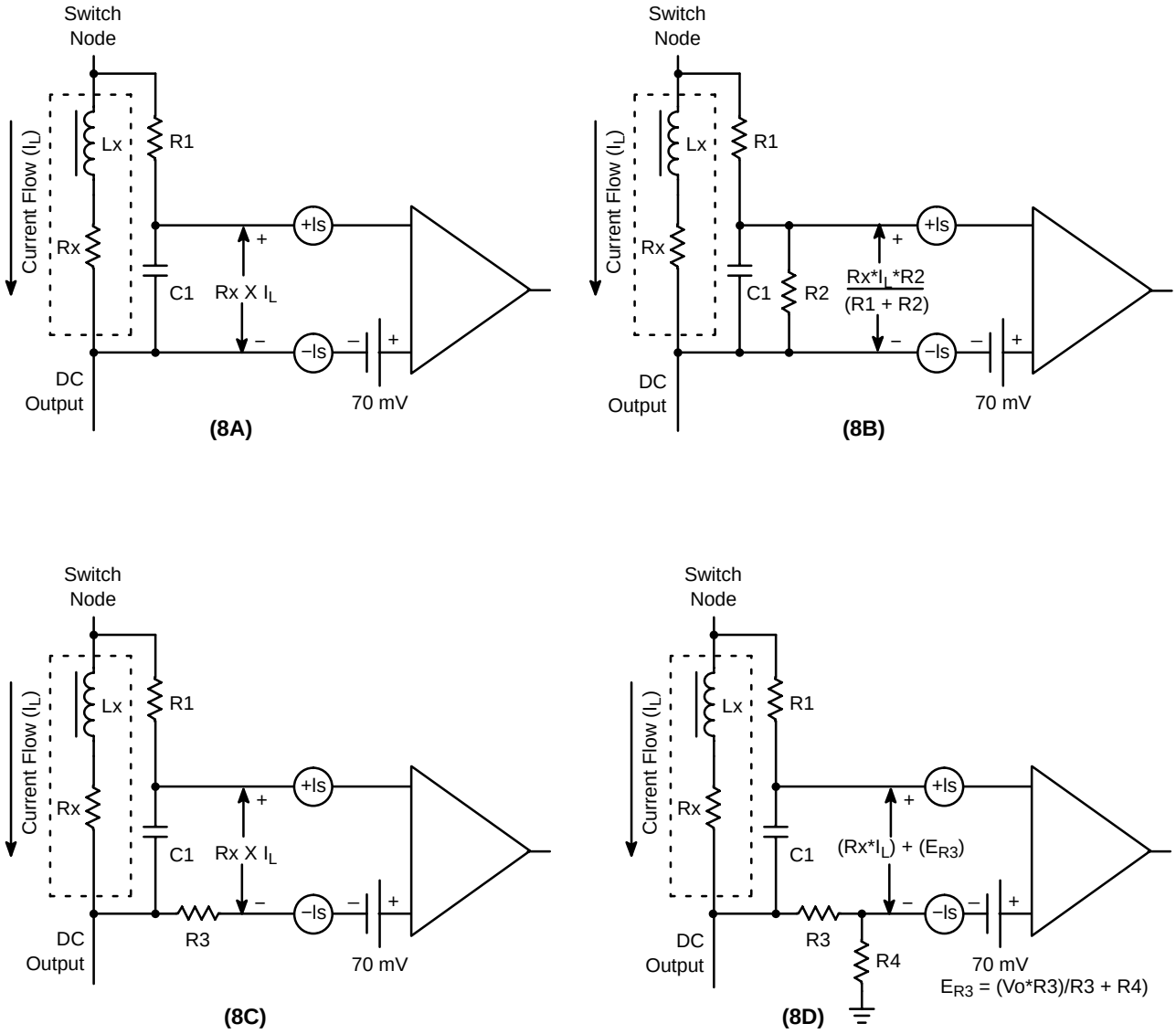



**Figure 8. Inductor Current Sensing − Circuit Configurations**

**Figure 8A − Basic Current Sensing**

Represents a basic inductor sensing configuration. When the voltage at pin +Is exceeds the voltage at pin –Is by 70 mV (nominal), the internal current sense comparator offset will be overcome. For this case, the current limit threshold is equal to (70 mV/Rx) amps. An obvious disadvantage of the basic configuration is the power supply designer has no control over the 70 mV offset, and limited control over the value of Rx. Therefore, he or she has little flexibility to set a specific current limit. Configurations (8B) and (8D) depict techniques to increase and decrease, respectively, the threshold current.

**Figure 8B – Increasing the Current Threshold**

Addition of resistor R2 forms a voltage divider such that only a portion of the voltage across Rx appears across C1. If, for example, R1 = R2, it will require a 140 mV drop across Rx to overcome the internal 70 mV current sense comparator offset. For optimum compensation with this configuration, R1 and R2 should be selected such that Rx is equal to their equivalent parallel resistance.

**Figure 8C – Bias Current Compensation**

Configurations 8A, 8B and 8D all introduce a potential error, since the bias currents of the current sense comparator inputs flow through unbalanced resistance paths. The addition of R3 in configuration 8C, where R3 = R1, restores a balanced input resistance, such that any voltage drops introduced by bias currents will cancel (assuming the +Is and –Is bias currents are equal). In the case of configuration 8B, R3 would be made equal to the equivalent resistance of R1 and R2 in parallel.

**Figure 8D – Decreasing the Current Threshold**

A voltage divider comprised of R3 and R4 is introduced to develop, by scaling the output voltage, a small voltage drop across R3 that opposes the internal current sense comparator offset. For example, if Vout = 1.2 V, R3 = 200 Ω, and R4 = 11.8 K, a DC voltage drop of 20 mV will be established across R3. The polarity of that voltage is such that it opposes the internal 70 mV offset, effectively reducing it to 50 mV. The current threshold is now given by (50 mV/Rx) instead of (70 mV/Rx).

### Current Limiting

Both channels of the NCP5425 employ identical Cycle−by−Cycle current limiting. Comparators with internal 70 mV offsets provide the references for setting current limit. Once a voltage greater than 70 mV is applied to the current limiting comparator, it resets that channel's output RS flip flop. This terminates the PWM pulse for the cycle and limits the energy delivered to the load. One advantage of this current limiting scheme is that the NCP5425 will limit large transient currents yet resume normal operation on the following cycle. A second benefit of limiting the PWM pulse width is, in an input power sharing application, one controller can be current limiting while the other supplies the remaining load current.

### Output Enable

On/Off control of the regulator outputs can be implemented by pulling the COMP pins low. Driving the COMP pins below the 0.20 V PWM comparator offset voltage disables switching of the GATE drivers.

## DESIGN GUIDELINES

### General

The output voltage tolerance can be affected by any or all of the following:

1. Buck regulator output voltage set point accuracy.
2. Output voltage change due to discharging or charging of the bulk decoupling capacitors during a load current transient.
3. Output voltage change due to the ESR and ESL of the bulk and high frequency decoupling capacitors, circuit traces, and vias.
4. Output voltage ripple and noise.

Budgeting the tolerance is left to the designer who must consider all of the above effects and provide an output voltage that will meet the specified tolerance at the load. The designer must also ensure that the regulator component temperatures are kept within the manufacturer's specified ratings at full load and maximum ambient temperature.

#### Selecting Feedback Divider Resistors

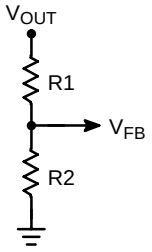



**Figure 9. Feedback Divider Resistors**

The feedback pins (VFB1(2)) are connected to external resistor dividers to set the output voltages. The error amplifier is referenced to 0.8 V and the output voltage is determined by selecting resistor divider values. Resistor R1 is selected based on a design trade−off between efficiency and output voltage accuracy. The output voltage error resulting from the bias current of the error amplifier can be estimated, neglecting resistor tolerance, from the following equation:

$$\%Error = (100)(1 \times 10^{-6})(R1)/0.8$$

$$\text{Rearranging, } R1 = (\%Error)(0.8)/(1 \times 10^{-4})$$

After R1 has been chosen, R2 can be calculated from:

$$R2 = (R1)/((V_{OUT}/0.8\ V) - 1)$$

Example:

Assume the desired $V_{OUT}$ = 1.2 V, and the tolerable error due to input bias current is 0.2%.

$$R1 = (0.2)(0.8)/(1 \times 10^{-4}) = 1.6\ K$$

$$R2 = 1.6\ K/((1.2/0.8) - 1) = 1.6\ K/0.5 = 3.2\ K$$

#### Calculating Duty Cycle

The duty cycle of a buck converter (including parasitic losses) is given by the formula:

$$\text{Duty Cycle} = D = \frac{V_{OUT} + (V_{HFET} + V_L)}{V_{IN} + V_{LFET} = V_{HFET} = V_L}$$

where:

$V_{OUT}$ = buck regulator output voltage;
$V_{HFET}$ = high side FET voltage drop due to RDS(ON);
$V_L$ = output inductor voltage drop due to inductor wire DC resistance;
$V_{IN}$ = buck regulator input voltage;
$V_{LFET}$ = low side FET voltage drop due to RDS(ON).

#### Switching Frequency Select and Set

Selecting the switching frequency is a trade−off between component size and power losses. Operation at higher switching frequencies allows the use of smaller inductor and capacitor values. Nevertheless, it is common to select lower frequency operation because a higher frequency also diminishes efficiency due to MOSFET gate charge losses. Additionally, low value inductors at higher frequencies result in higher ripple current, higher output voltage ripple, and lower efficiency at light load currents. The value of the oscillator resistor is designed to be linearly related to the switching period. If the designer prefers not to use Figure 10 to select the appropriate resistance, the following equation is a suitable alternative:

$$R_{OSC} = \frac{21700 - f_{SW}}{2.31\ f_{SW}}$$

where:

$R_{OSC}$ = oscillator resistor in kΩ;
$f_{SW}$ = switching frequency in kHz.

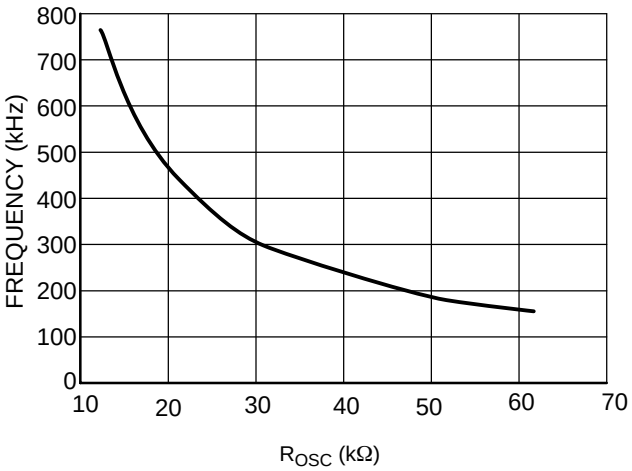



**Figure 10. Switching Frequency vs. $R_{OSC}$**

### Output Inductor Selection

The inductor should be selected based on the criteria of inductance, current capability, and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response. There are many factors to consider in selecting inductors including cost, efficiency, EMI and ease of manufacture. The inductor must be able to handle the peak current at the switching frequency without saturating, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss.

There are a variety of materials and types of magnetic cores that could be used, such as ferrites, molypermalloy cores (MPP), and amorphous and powdered iron cores. Powdered iron cores are particularly suitable due to high saturation flux density and low loss at high frequencies, a distributed gap, and they produce very low EMI. The minimum value of inductance to prevent inductor saturation, or exceeding the rated FET current, can be calculated as follows:

$$L_{MIN} = \frac{(V_{IN(MIN)} - V_{OUT})V_{OUT}}{f_{SW} \times V_{IN(MIN)} \times I_{SW(MAX)}}$$

where:

$L_{MIN}$ = minimum inductance value;
$V_{IN}$(MIN) = minimum design input voltage;
$V_{OUT}$ = output voltage;
$f_{SW}$ = switching frequency;
$I_{SW}$(MAX) = maximum design switch current.

The inductor ripple current can then be determined by:

$$\Delta I_L = \frac{V_{OUT} \times (1 - D)}{L \times f_{SW}}$$

where:

$\Delta_{IL}$ = inductor ripple current;
$V_{OUT}$ = output voltage;
L = inductor value;
D = duty cycle;
$f_{SW}$ = switching frequency.

After inductor selection, the designer can verify if the number of output capacitors will provide an acceptable output voltage ripple (1.0% of output voltage is common). The formula below is used;

$$\Delta I_L = \frac{\Delta V_{OUT}}{ESR_{MAX}}$$

where:

$ESR_{MAX}$ = maximum allowable ESR;
$\Delta V_{OUT}$ = 1.0% · VOUT = maximum allowable output voltage ripple (budgeted by the designer);
$\Delta I_L$ = inductor ripple current;
$V_{OUT}$ = output voltage.

Rearranging, we have:

$$ESR_{MAX} = \frac{\Delta V_{OUT}}{\Delta I_L}$$

The number of output capacitors is determined by:

$$\text{Number of capacitors} = \frac{ESR_{CAP}}{ESR_{MAX}}$$

where:

$ESR_{CAP}$ = maximum ESR per capacitor (specified in manufacturer's data sheet).

The designer must also verify that the inductor value yields reasonable inductor peak and valley currents (the inductor current is a triangular waveform):

$$I_{L(PEAK)} = I_{OUT} + \frac{\Delta I_L}{2} \qquad I_{L(VALLEY)} = I_{OUT} + \frac{\Delta I_L}{2}$$

where:

$I_{L(PEAK)}$ = inductor peak current;
$I_{L(VALLEY)}$ = inductor valley current;
$I_{OUT}$ = load current;
$\Delta I_L$ = inductor ripple current.

### Output Capacitor Selection

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the regulator output voltage. Key specifications for output capacitors are ESR (Equivalent Series Resistance) and ESL (Equivalent Series Inductance). For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required. To determine the number of output capacitors the maximum voltage transient allowed during load transitions has to be specified. The output capacitors must hold the output voltage within these limits since the inductor current can not change at the required slew rate. The output capacitors must therefore have a very low ESL and ESR.

The voltage change during the load current transient is given by:

$$\Delta V_{OUT} = \Delta I_{OUT} \times \left(\frac{ESL}{\Delta t} + ESR + \frac{t_{TR}}{C_{OUT}}\right)$$

where:

$\Delta I_{OUT}/D\Delta$ = load current slew rate;
$\Delta I_{OUT}$ = load transient;
$\Delta t$ = load transient duration time;
ESL = Maximum allowable ESL including capacitors, circuit traces, and vias;
ESR = Maximum allowable ESR including capacitors and circuit traces;
$t_{TR}$ = output voltage transient response time;
$C_{OUT}$ = output capacitance.

The designer must independently assign values for the change in output voltage due to ESR, ESL, and output capacitor discharging or charging. Empirical data indicates that most of the output voltage change (droop or spike, depending on the load current transition) results from the total output capacitor ESR.

Maximum allowable ESR can then be determined according to the formula:

$$ESR_{MAX} = \frac{\Delta V_{ESR}}{\Delta I_{OUT}}$$

where:

$\Delta V_{ESR}$ = change in output voltage due to ESR (assigned by the designer)

Once the maximum allowable ESR is determined, the number of output capacitors can be calculated:

$$\text{Number of capacitors} = \frac{ESR_{CAP}}{ESR_{MAX}}$$

where:

$ESR_{CAP}$ = maximum ESR per capacitor (specified in manufacturer's data sheet);

$ESR_{MAX}$ = maximum allowable ESR.

The actual output voltage deviation due to ESR can then be verified and compared to the value assigned by the designer:

$$\Delta V_{ESR} = \Delta I_{OUT} \times ESR_{MAX}$$

Similarly, the maximum allowable ESL is calculated from the following formula:

$$ESL_{MAX} = \frac{\Delta V_{ESL} \times \Delta t}{\Delta I}$$

### Input Inductor Selection

A common requirement is that the buck controller must not disturb the input voltage. One method of achieving this is by using an input inductor and a bypass capacitor. The input inductor isolates the supply from the noise generated in the switching portion of the buck regulator and also limits the inrush current into the input capacitors during power up. The inductor's limiting effect on the input current slew rate becomes increasingly beneficial during load transients. The worst case is when the load changes from no load to full load (load step), a condition under which the highest voltage change across the input capacitors is also seen by the input inductor. An input inductor successfully blocks the ripple current while placing the transient current requirements on the input bypass capacitor bank, which has to initially support the sudden load change. The minimum value for the input inductor is:

$$L_{IN} = \frac{\Delta V}{(dI/dt)_{MAX}}$$

where:

$L_{IN}$ = input inductor value;

$\Delta V$ = voltage seen by the input inductor during a full load swing;

$(dI/dt)_{MAX}$ = maximum allowable input current slew rate.

The designer must select the LC filter pole frequency such that a minimum of 40 dB attenuation is obtained at the regulator switching frequency. The LC filter is a double−pole network with a slope of −2.0, a roll−off rate of −40 dB/decade, and a corner frequency given by:

$$f_C = \frac{1}{2\pi \times \sqrt{LC}}$$

where:

L = input inductor;

C = input capacitor(s).

## POWER FET SELECTION

### FET Basics

The use of a MOSFET as a power switch is compelled by two reasons: 1) *high input impedance*; and 2) *fast switching times*. The electrical characteristics of a MOSFET are considered to be nearly those of a perfect switch. Control and drive circuitry power is therefore reduced. Because the input impedance is so high, it is voltage driven. The input of the MOSFET acts as if it were a small capacitor, which the driving circuit must charge at turn on. The lower the drive impedance, the higher the rate of rise of $V_{GS}$, and the faster the turn−on time. Power dissipation in the switching MOSFET consists of: (1) conduction losses, (2) leakage losses, (3) turn−on switching losses, (4) turn−off switching losses, and (5) gate−transitions losses. The latter three losses are all proportional to frequency. The most important aspect of FET performance is the Static Drain−to−Source On−Resistance ($R_{DS(ON)}$), which affects regulator efficiency and FET thermal management requirements. The On−Resistance determines the amount of current a FET can handle without excessive power dissipation that may cause overheating and potentially catastrophic failure. As the drain current rises, especially above the continuous rating, the On−Resistance also increases. Its positive temperature coefficient is between +0.6%/°C and +0.85%/°C. The higher the On−Resistance, the larger the conduction loss is. Additionally, the FET gate charge should be low in order to minimize switching losses and reduce power dissipation. Both logic level and standard FETs can be used. Voltage applied to the FET gates depends on the application circuit used. Both upper and lower gate driver outputs are specified to drive to within 1.5 V of ground when in the low state and to within 2.0 V of their respective bias supplies when in the high state. In practice, the FET gates will be driven rail−to−rail due to overshoot caused by the capacitive load they present to the controller IC.

### Switching (Upper) FET Selection

The designer must ensure that the total power dissipation in the FET switch does not cause the power component's junction temperature to exceed 150°C. The maximum RMS current through the switch can be determined by the following formula:

$$I_{RMS(H)} = \sqrt{\frac{I_{L(PEAK)}^2 + (I_{L(PEAK)} \times I_{L(VALLEY)}) + I_{L(VALLEY)}^2 \times D}{3}}$$

where:

$I_{RMS(H)}$ = maximum switching MOSFET RMS current;
$I_{L(PEAK)}$ = inductor peak current;
$I_{L(VALLEY)}$ = inductor valley current;
D = duty cycle.

Once the RMS current through the switch is known, the switching MOSFET conduction losses can be calculated by:

$$P_{RMS(H)} = I_{RMS(H)}^2 \times R_{DS(ON)}$$

where:

$P_{RMS(H)}$ = switching MOSFET conduction losses;
$I_{RMS(H)}$ = maximum switching MOSFET RMS current;
$R_{DS(ON)}$ = FET drain−to−source on−resistance.

Upper MOSFET switching losses occur during MOSFET switch−on and switch−off, and can be calculated by:

$$P_{SWH} = P_{SWH(ON)} + P_{SWH(OFF)} = \frac{V_{IN} \times I_{OUT} \times (t_{RISE} + t_{FALL})}{6T}$$

where:

$P_{SWH(ON)}$ = upper MOSFET switch−on losses;
$P_{SWH(OFF)}$ = upper MOSFET switch−off losses;
$V_{IN}$ = input voltage;
$I_{OUT}$ = load current;
$T_{RISE}$ =MOSFET rise time (from FET manufacturer's switching characteristics performance curve);
TFALL = MOSFET fall time (from FET manufacturer's switching characteristics performance curve);
$T = 1/f_{SW}$ = period.

The total power dissipation in the switching MOSFET can then be calculated as:

$$P_{HFET(TOTAL)} = P_{RMS(H)} + P_{SWH(ON)} + P_{SWH(OFF)}$$

where:

$P_{HFET(TOTAL)}$ = total switching (upper) MOSFET losses;
$P_{RMS(H)}$ = upper MOSFET switch conduction Losses;
$P_{SWH(ON)}$ = upper MOSFET switch−on losses;
$P_{SWH(OFF)}$ = upper MOSFET switch−off losses.

Once the total power dissipation in the switching FET is known, the maximum FET switch junction temperature can be calculated:

$$T_J = T_A + [P_{HFET(TOTAL)} \times R_{\theta JA}]$$

where:

$T_J$ = FET junction temperature;
$T_A$ = ambient temperature;
$P_{HFET(TOTAL)}$ = total switching (upper) FET losses;
$R_{\theta JA}$ = upper FET junction−to−ambient thermal resistance.

**Synchronous (Lower) FET Selection**

The switch conduction losses for the lower FET are calculated as follows:

$$P_{RMS(L)} = I_{RMS}^2 \times R_{DS(ON)} = \left[I_{OUT} \times \sqrt{(1 - D)}\right]^2 \times R_{DS(ON)}$$

where:

$P_{RMS(L)}$ = lower MOSFET conduction losses;
$I_{OUT}$ = load current;
D = Duty Cycle;
$R_{DS(ON)}$ = lower FET drain−to−source on−resistance.

The synchronous MOSFET has no switching losses, except for losses in the internal body diode, because it turns on into near zero voltage conditions. The MOSFET body diode will conduct during the non−overlap time and the resulting power dissipation (neglecting reverse recovery losses) can be calculated as follows:

$$P_{SWL} = V_{SD} \times I_{LOAD} \times \text{non−overlap time} \times f_{SW}$$

where:

$P_{SWL}$ = lower FET switching losses;
$V_{SD}$ = lower FET source−to−drain voltage;
$I_{LOAD}$ = load current;
Non−overlap time = GATE(L)−to−GATE(H) or GATE(H)−to−GATE(L) delay (from NCP5425 data sheet Electrical Characteristics section);
$f_{SW}$ = switching frequency.

The total power dissipation in the synchronous (lower) MOSFET can then be calculated as:

$$P_{LFET(TOTAL)} = P_{RMS(L)} + P_{SWL}$$

where:

$P_{LFET(TOTAL)}$ = Synchronous (lower) FET total losses;
$P_{RMS(L)}$ = Switch Conduction Losses;
$P_{SWL}$ = Switching losses.

Once the total power dissipation in the synchronous FET is known the maximum FET switch junction temperature can be calculated:

$$T_J = T_A + [P_{LFET(TOTAL)} \times R_{\theta JA}]$$

where:

$T_J$ = MOSFET junction temperature;
$T_A$ = ambient temperature;
$P_{LFET(TOTAL)}$ = total synchronous (lower) FET losses;
$R_{\theta JA}$ = lower FET junction−to−ambient thermal resistance.

### Control IC Power Dissipation

The power dissipation of the IC varies with the MOSFETs used, VCC, and the NCP5425 operating frequency. The average MOSFET gate charge current typically dominates the control IC power dissipation, and is given by:

$$P_{CONTROL(IC)} = I_{CC1}V_{CC1} + I_{BST}V_{BST} + P_{GATE(H)1} + P_{GATE(L)1} + P_{GATE(H)2} + P_{GATE(L)2}$$

where:

$P_{CONTROL(IC)}$ = control IC power dissipation;
$I_{CC1}$ = IC quiescent supply current;
$V_{CC1}$ = IC supply voltage;
$P_{GATE(H)}$ = upper MOSFET gate driver (IC) losses;
$P_{GATE(L)}$ = lower MOSFET gate driver (IC) losses.

The upper (switching) MOSFET gate driver (IC) losses are given by:

$$P_{GATE(H)} = Q_{GATE(H)} \times f_{SW} \times V_{BST}$$

where:

$P_{GATE(H)}$ = upper MOSFET gate driver (IC) losses;
$Q_{GATE(H)}$ = total upper MOSFET gate charge at VCC;
$f_{SW}$ = switching frequency.

The lower (synchronous) MOSFET gate driver (IC) losses are:

$$P_{GATE(L)} = Q_{GATE(L)} \times f_{SW} \times V_{CC}$$

where:

$P_{GATE(L)}$ = lower MOSFET gate driver (IC) losses;
$Q_{GATE(L)}$ = total lower MOSFET gate charge at VCC;
$f_{SW}$ = switching frequency.

The junction temperature of the control IC is primarily a function of the PCB layout, since most of the heat is removed through the traces connected to the pins of the IC.

## CURRENT SENSING AND CURRENT SHARING

### Current Sharing Errors

The three main errors in current are from board layout imbalances, inductor mismatch, and input offsets in the error amplifiers. The first two sources of error can be controlled through careful component selection and good layout practice. With a 4.0 mΩ (parasitic winding resistance) inductor, for example, one mV of input offset error will represent 0.25 A of measurement error. One way to diminish this effect is to use higher resistance inductors, but the penalty is higher power losses in the inductors.

### Current Limiting Options

The current supplied to the load can be sensed using the IS+ and IS− pins. These pins sense a voltage, proportional to the output current, and compare it to a fixed internal voltage threshold. When the differential voltage exceeds 70 mV, the internal overcurrent protection system goes into a cycle−by−cycle limiting mode. Two methods for sensing the current are available.

### Sense Resistor

A sense resistor can be added in series with the inductor. When the voltage drop across the sense resistor exceeds the internal voltage threshold of 70 mV, a limit condition is set. The sense resistor value is calculated by:

$$R_{SENSE} = \frac{0.070\ V}{I_{LIMIT}}$$

In a high current supply, the sense resistor will be a very low value, typically less than 10 mΩ. Such a resistor can be either a discrete component or a PCB trace. The resistance of a discrete component can be more precise than a PCB trace, but the cost is also greater. Setting the current limit using an external sense resistor is very precise because all the values can be designed to specific tolerances. However, the disadvantage of using a sense resistor is its additional constant power loss and heat generation. Trace resistance can vary as much as ± 10% due to copper plating variations.

### Inductor ESR

Another means of sensing current is to use the intrinsic resistance of the inductor. A model of an inductor reveals that the windings have an effective series resistance (ESR). The voltage drop across the inductor ESR can be measured with a simple parallel circuit: an RC integrator. If the value of RS1 and C are chosen such that:

$$\frac{L}{ESR} = R_{S1}C$$

then the voltage measured across the capacitor C will be:

$$V_C = ESR \times I_{LIM}$$

### Inductor Sensing Component Selection

Select the capacitor C first. A value of 0.1 μF is recommended. The value of RS1 can be calculated by:

$$R_{S1} = \frac{L}{ESR \times C}$$

Typical values for inductor ESR range in the low milliohms; consult manufacturer's data sheets for specific values. Selection of components at these values will result in a current limit of:

$$I_{LIM} = \frac{0.070\ V}{ESR}$$

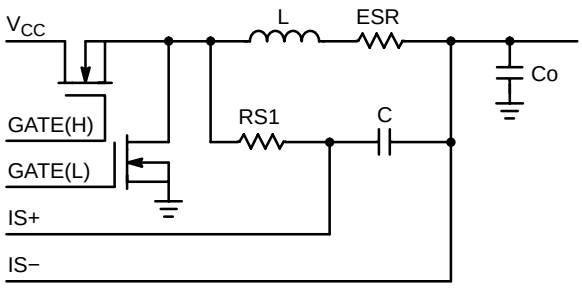



**Figure 11. Inductor ESR Current Sensing**

Given an ESR value of 3.5 mΩ, the current limit becomes 20 A. If an increased current limit is required, a resistor divider can be added (see Figure 8). Advantages of setting the current limit by using the winding resistance of the inductor (relative to a sense resistor) are higher efficiency and lower heat generation. The tolerance of the inductor ESR must be factored into the design of the current limit. Finally, one or two more components are required for this approach than with resistor sensing.

### Selecting and Configuring Current Sharing for a 2 Phase Single Output Application

When the two controllers are connected as a single output two phase Buck Converter, they are in a Master−Slave configuration. The Slave controller on the right side of Figure 6 tries to follow information provided by the Master controller, on the left. This circuit uses inductor current sensing, in which the parasitic resistances (LSR) of the controllers' output chokes are used as current sensing elements. On the Slave side (Controller Two), both Error Amplifier inputs are brought to external pins so the reference is available. The RC network in parallel with the output inductor on the Master side (Controller One) generates the reference for the Slave. Current information from the Slave is fed back to the error amplifier's inverting input. In this configuration, the Slave tries to adjust its current to match the current information fed to its reference input from the Master Controller. If 50−50 current sharing is needed, then Figure 8a is used for both sides to generate the reference and the inverting signals. The values for both sides should be calculated with the following equation:

$$R1 = \frac{Lx}{C1 \cdot Rx}, \text{ where,}$$

$L_x$ = Inductor value, both controllers should use the same inductor.

$R_x$ = Internal resistance of L, from the inductor data sheet.

C1 = Select a value such that R1 is less than 15 KΩ.

With the RC time constant selected to equal the $L_x/R_x$ time constant, the voltage across the capacitor will be equal to the voltage drop across the internal resistance of the inductor. For proper sharing, the inductors on both Master and Slave side should be the identical.

If a current share ratio other than 50−50 is desired, inductor sense resistor network selection is a three step process:

1. Decide how the total load current will be budgeted between the two controllers.
2. Calculate the value of R1 for the controller with the lesser current share.
3. Calculate the current sense resistor network (2 resistors) for the controller with the greater current share.

In the two examples that follow, the inductor sense resistors are designated R1, R2, and R3, as depicted in Figures 12 and 13.

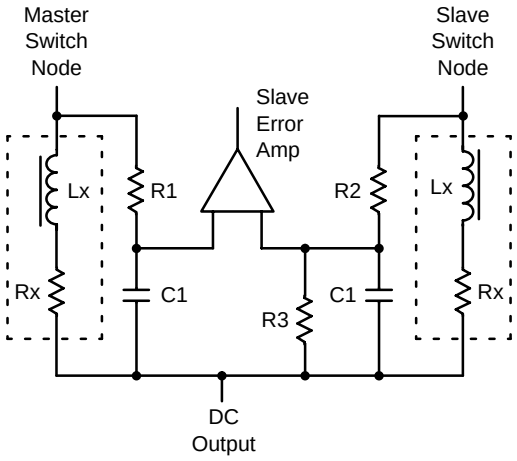



**Figure 12. 40%/60% Current Sharing**

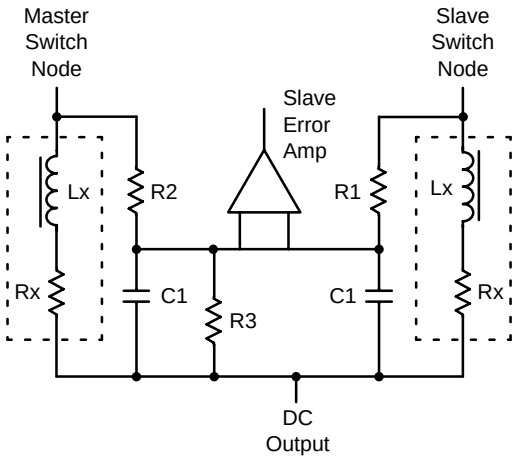



**Figure 13. 66.7%/33.3% Current Sharing**

### Example 1

Assume we have elected to source 40% of the output current from the master controller, and 60% from the Slave. Figure 12 shows the configuration of the inductor sense networks and Slave error amplifier. The ratio of Slave−to−Master load current is 60%/40%, or 1.5:1. R2 and R3 must be chosen to satisfy two conditions:

A parallel equivalent resistance equal to R1, and,

A ratio such that the drop across the parasitic resistance of the Slave inductor is 1.5 times the drop across the parasitic resistance of the Master inductor when the inputs to the Slave error amplifier are equal (assumes the inductors are identical). The optimum value of R1 is described by the equation:

$$R1 = Lx/(C1 * Rx)$$

The values of R2 and R3 can be found by solving two simultaneous equations:

$$R2 = R3/2$$

$$R1 = (R2 * R3)/(R2 + R3)$$

Solving for R2 and R3 yields:

$$R2 = 1.5R1$$

$$R3 = 3R1$$

**Example 2**

Assume we have elected to source 66.7% output current from the Master controller, and 33.3% from the Slave. Figure 13 shows the configuration of the inductor sense networks and Slave error amplifier for this case. The ratio of Master−to−Slave load current is equal to 66.7%/33.3%, or 2:1. Therefore R2 and R3 must be chosen to satisfy two conditions:

A parallel equivalent resistance equal to R1, and,

A ratio such that the drop across the parasitic resistance of the Master inductor is 2 times the drop across the parasitic resistance of the Slave inductor when the inputs to the Slave error amplifier are equal (assumes the inductors are identical). The optimum value of R1 is described by the equation:

$$R1 = Lx/(C1 * Rx)$$

The values of R2 and R3 can be found by solving two simultaneous equations:

$$R2 = R3$$

$$R1 = (R2 * R3)/(R2 + R3)$$

Solving for R2 and R3 yields:

$$R2 = 2R1$$

$$R3 = 2R1$$

Note that the Mode pin must be floating for a two−phase, single output design. This disables the internal Error Amplifier Reference clamp, and increases its common mode range.

**No Load Zero Balance**

To improve current matching, a low pass filter can be inserted between the Master controller inductor sensing RC network and the Slave controller Vref2 input pin (see Figure 14). This will attenuate the amplitude of the out−of−phase ripple current signal superimposed on the DC current signal, providing a smoother Slave Error Amplifier reference input.

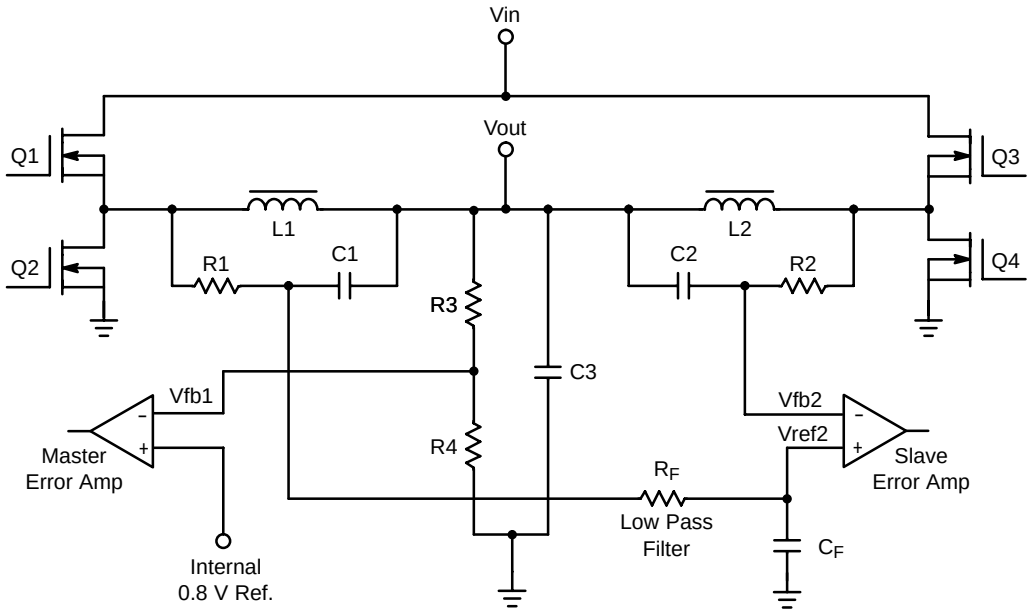



**Figure 14. Addition of a Low Pass Filter to the Current Sense Reference Input**

With the value of $R_F$ set to approximately two times the value of R1, Cf can be calculated as follows:

$$Cf = 1/(2\pi \cdot f \cdot R_F), \text{ where :}$$

f = operating frequency of the controller

When a filter is added, the response delay introduced by the RC time constant must be considered.

**Configuring a Dual Output Application**

To configure the NCP5425 for a dual output application:

- The Mode pin must be grounded
- An external voltage reference must be provided for Controller 2, via the Vref2 pin

Grounding the Mode pin enables an internal clamp to limit the Comp 2 voltage excursions during overcurrent faults. Without this clamp, the output voltage (Vout1 and Vout2) can overshoot the regulated output voltages when the fault is removed. For a single output two−phase application the Mode pin must be floating, which disables the clamp and permits a larger current−sharing reference voltage range. The Comp1 pin is always clamped, because it is regulated to a fixed internal voltage (0.8 V).

The simplest way to provide a Controller 2 reference is by using the Controller 1 feedback voltage. This will provide a 0.8 V reference for regulation, and also causes the Controller 2 output to track the Controller 1 output during transients. With a voltage reference established and the Mode pin floating, Controller 2 can function as an independent Buck regulator.

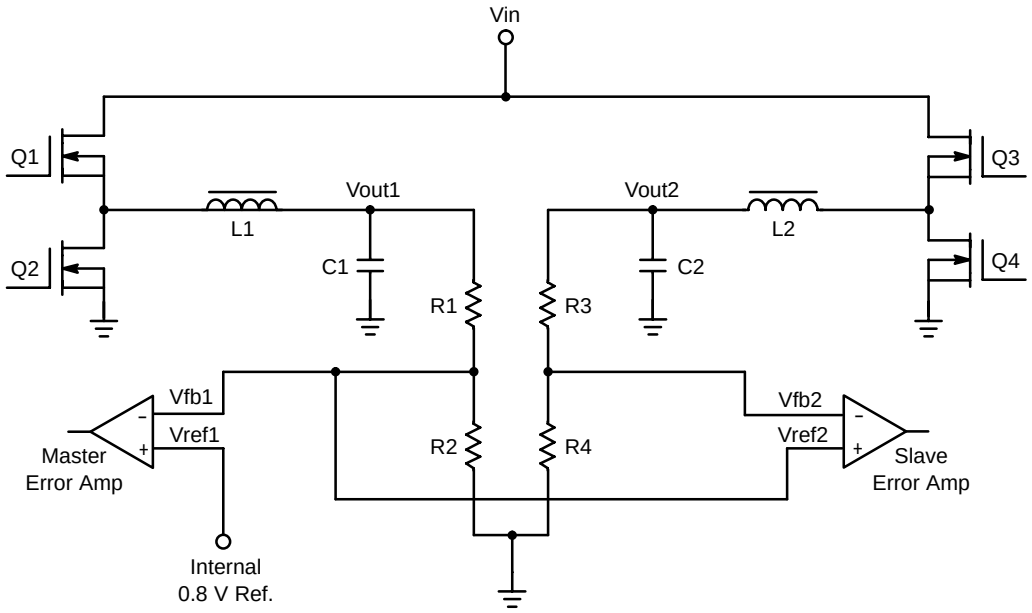



**Figure 15. Dual Output Configuration**

### Adding External Slope Compensation

Today's voltage regulators are expected to meet very stringent load transient requirements. One of the key factors in achieving tight dynamic voltage regulation is low ESR. Low ESR at the regulator output results in low output voltage ripple. The consequence is, however, that very little voltage ramp exists at the control IC feedback pin (VFB), resulting in increased regulator sensitivity to noise and the potential for loop instability. In applications where the internal slope compensation is insufficient, the performance of the NCP5425−based regulator can be improved through the addition of a fixed amount of external slope compensation at the output of the PWM Error Amplifier (the COMP pin) during the regulator off−time. Referring to Figure 8, the amount of voltage ramp at the COMP pin is dependent on the gate voltage of the lower (synchronous) FET and the value of resistor divider formed by R1and R2.

$$V_{SLOPECOMP} = V_{GATE(L)} \times \left(\frac{R2}{R1 + R2}\right) \times (1 - e^{\frac{-1}{\tau}})$$

where:

$V_{SLOPECOMP}$ = amount of slope added;
$V_{GATE(L)}$ = lower MOSFET gate voltage;
R1, R2 = voltage divider resistors;
t = $t_{ON}$ or $t_{OFF}$ (switch off−time);
$\tau$ = RC constant determined by C1 and the parallel combination of R1, R2 neglecting the low driver output impedance.

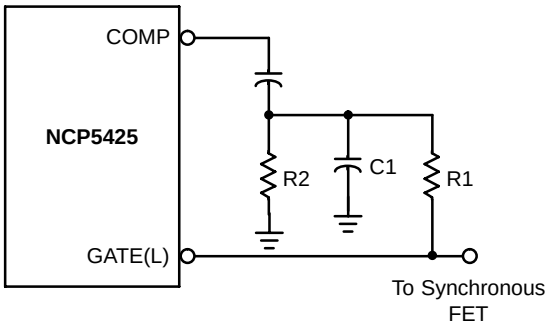



**Figure 16. RC Filter Provides the Proper Voltage Ramp at the Beginning of each On−Time Cycle**

The artificial voltage ramp created by the slope compensation scheme results in improved control loop stability provided that the RC filter time constant is smaller than the off−time cycle duration (time during which the lower MOSFET is conducting). It is important that the series combination of R1 and R2 is high enough in resistance to avoid loading the GATE(L) pin. Also, C1 should be very small (less than a few nF) to avoid heating the part.

## EMI MANAGEMENT

As a consequence of large currents being turned on and off at high frequency, switching regulators generate noise during normal operation. When designing for compliance with EMI/EMC regulations, additional components may be necessary to reduce noise emissions. These components are not required for regulator operation and experimental results may allow them to be eliminated. The input filter inductor may not be required because bulk filter and bypass capacitors, as well as other loads located on the board will tend to reduce regulator di/dt effects on the circuit board and input power supply. Placement of the power components to minimize routing distance will also help to reduce emissions.

## LAYOUT GUIDELINES

When laying out a buck regulator on a printed circuit board, the following checklist should be used to ensure proper operation of the NCP5425.

1. Rapid changes in voltage across parasitic capacitors and abrupt changes in current in parasitic inductors are major concerns.
2. Keep high currents out of sensitive ground connections.
3. Avoid ground loops as they pick up noise. Use star or single point grounding.
4. For high power buck regulators on double−sided PCB's a single ground plane (usually the bottom) is recommended.
5. Even though double sided PCB's are usually sufficient for a good layout, four−layer PCB's are the optimum approach to reducing susceptibility to noise. Use the two internal layers as the power and GND planes, the top layer for power connections and component vias, and the bottom layers for the noise sensitive traces.
6. Keep the inductor switching node small by placing the output inductor, switching and synchronous FETs close together.
7. The MOSFET gate traces to the IC must be short, straight, and wide as possible.
8. Use fewer, but larger output capacitors, keep the capacitors clustered, and use multiple layer traces with wide, thick copper to keep the parasitic resistance low.
9. Place the switching MOSFET as close to the input capacitors as possible.
10. Place the output capacitors as close to the load as possible.
11. Place the COMP capacitor as close as possible to the COMP pin.
12. Connect the filter components of pins $R_{OSC}$, $V_{FB}$, $V_{OUT}$, and COMP, to the GND pin with a single trace, and connect this local GND trace to the output capacitor GND.
13. Place the $V_{CC}$ bypass capacitors as close as possible to the IC.
14. Place the $R_{OSC}$ resistor as close as possible to the $R_{OSC}$ pin.
15. Assign the output with lower duty cycle to channel 2, which has inherently better noise immunity.

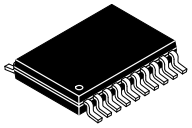
$V^2$ is a trademark of Switch Power, Inc.

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

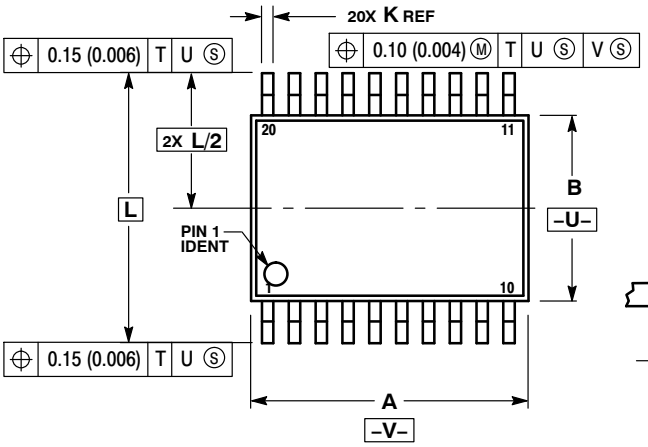
ON Semiconductor®

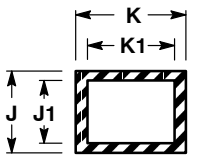
**TSSOP−20 WB**
CASE 948E
ISSUE D

DATE 17 FEB 2016

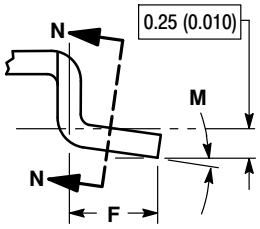


SCALE 2:1

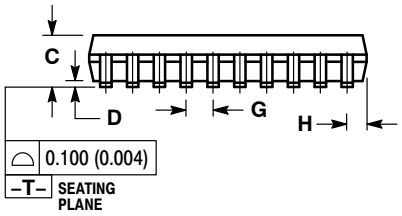


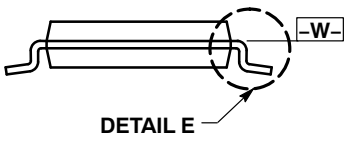




SECTION N−N




DETAIL E

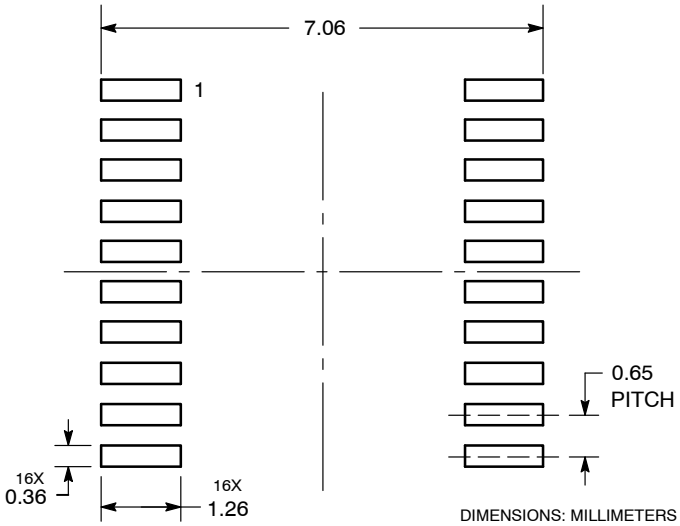



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

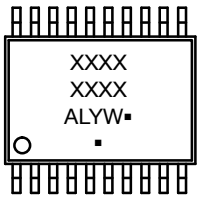
| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

### SOLDERING FOOTPRINT




DIMENSIONS: MILLIMETERS

### GENERIC MARKING DIAGRAM*




A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

| DOCUMENT NUMBER: | 98ASH70169A | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
|---|---|---|
| DESCRIPTION: | TSSOP−20 WB | PAGE 1 OF 1 |

## PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT**:
**Email Requests to:** orderlit@onsemi.com

**onsemi Website:** www.onsemi.com

**TECHNICAL SUPPORT**
**North American Technical Support:**
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

**Europe, Middle East and Africa Technical Support:**
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊