NCP1652, NCP1652A

Controller, PFC, High Efficiency, Single Stage

The NCP1652 is a highly integrated controller for implementing power factor correction (PFC) and isolated step down ac–dc power conversion in a single stage, resulting in a lower cost and reduced part count solution. This controller is ideal for notebook adapters, battery chargers and other off–line applications with power requirements between 75 W and 150 W. The single stage is based on the flyback converter and it is designed to operate in continuous conduction (CCM) or discontinuous conduction (DCM) modes.

The NCP1652 increases the system efficiency by incorporating a secondary driver with adjustable nonoverlap delay for controlling a synchronous rectifier switch in the secondary side, an active clamp switch in the primary or both. In addition, the controller features a proprietary Soft–Skip™ to reduce acoustic noise at light loads. Other features found in the NCP1652 include a high voltage startup circuit, voltage feedforward, brown out detector, internal overload timer, latch input and a high accuracy multiplier.

Features
- Dual Control Outputs with Adjustable Non Overlap Delay for Driving a Synchronous Rectifier Switch, an Active Clamp Switch or Both
- Voltage Feedforward Improves Loop Response
- Frequency Jittering Reduces EMI Signature
- Proprietary Soft–Skip™ at Light Loads Reduces Acoustic Noise
- Brown Out Detector
- Internal 150 ms Fault Timer
- Independent Latch–Off Input Facilitates Implementation of Overvoltage and Overtemperature Fault Detectors
- Single Stage PFC and Isolated Step Down Converter
- Continuous or Discontinuous Conduction Mode Operation
- Average Current Mode Control (ACMC), Fixed Frequency Operation
- High Accuracy Multiplier Reduces Input Line Harmonics
- Adjustable Operating Frequency from 20 kHz to 250 kHz
- These are Pb–Free Devices

Typical Applications
- Notebook Adapter
- High Current Battery Chargers
- Front Ends for Distributed Power Systems
- High Power Solid State Lighting

See detailed ordering and shipping information in the package dimensions section on page 32 of this data sheet.
Figure 1. Pin Connections
Figure 2. Detailed Block Diagram
## PIN FUNCTION DESCRIPTION

<table>
<thead>
<tr>
<th>Pin</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>16 Pin</td>
<td>20 Pin</td>
<td>Symbol</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>CT</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>RAMP COMP</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>AC IN</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td>FB</td>
</tr>
<tr>
<td>5</td>
<td>5</td>
<td>VFF</td>
</tr>
<tr>
<td>6</td>
<td>6</td>
<td>CM</td>
</tr>
<tr>
<td>7</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>9</td>
<td>AC COMP</td>
</tr>
<tr>
<td>8</td>
<td>10</td>
<td>Latch</td>
</tr>
<tr>
<td>9</td>
<td>11</td>
<td>Rdelay</td>
</tr>
<tr>
<td>10</td>
<td>12</td>
<td>$I_{AVG}$</td>
</tr>
<tr>
<td>11</td>
<td>13</td>
<td>$I_{Spos}$</td>
</tr>
<tr>
<td>12</td>
<td>14</td>
<td>$V_{CC}$</td>
</tr>
<tr>
<td>13</td>
<td>15</td>
<td>OUTA</td>
</tr>
<tr>
<td>14</td>
<td>16</td>
<td>OUTB</td>
</tr>
<tr>
<td>15</td>
<td>17</td>
<td>GND</td>
</tr>
<tr>
<td>18</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>20</td>
<td>HV</td>
</tr>
</tbody>
</table>
MAXIMUM RATINGS (Notes 1 and 2)

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Start_up Input Voltage</td>
<td>$V_{HV}$</td>
<td>-0.3 to 500</td>
<td>V</td>
</tr>
<tr>
<td>Start_up Input Current</td>
<td>$I_{HV}$</td>
<td>± 100</td>
<td>mA</td>
</tr>
<tr>
<td>Power Supply Input Voltage</td>
<td>$V_{CC}$</td>
<td>-0.3 to 20</td>
<td>V</td>
</tr>
<tr>
<td>Power Supply Input Current</td>
<td>$I_{CC}$</td>
<td>± 100</td>
<td>mA</td>
</tr>
<tr>
<td>Latch Input Voltage</td>
<td>$V_{Latch}$</td>
<td>-0.3 to 10</td>
<td>V</td>
</tr>
<tr>
<td>Latch Input Current</td>
<td>$I_{Latch}$</td>
<td>± 100</td>
<td>mA</td>
</tr>
<tr>
<td>OUTA Pin Voltage</td>
<td>$V_{outA}$</td>
<td>-0.3 to 20</td>
<td>V</td>
</tr>
<tr>
<td>OUTA Pin Current</td>
<td>$I_{outA}$</td>
<td>± 100</td>
<td>mA</td>
</tr>
<tr>
<td>OUTB Pin Voltage</td>
<td>$V_{outB}$</td>
<td>-0.3 to 20</td>
<td>V</td>
</tr>
<tr>
<td>OUTB Pin Current</td>
<td>$I_{outB}$</td>
<td>± 600</td>
<td>mA</td>
</tr>
<tr>
<td>All Other Pins Voltage</td>
<td></td>
<td>-0.3 to 6.5</td>
<td>V</td>
</tr>
<tr>
<td>All Other Pins Current</td>
<td></td>
<td>± 100</td>
<td>mA</td>
</tr>
<tr>
<td>Thermal Resistance, Junction—to–Air</td>
<td>$\theta_{JA}$</td>
<td>130</td>
<td>°C/W</td>
</tr>
<tr>
<td>0.1 in” Copper</td>
<td></td>
<td>110</td>
<td>°C/W</td>
</tr>
<tr>
<td>Thermal Resistance, Junction—to–Lead</td>
<td>$R_{JUL}$</td>
<td>50</td>
<td>°C/W</td>
</tr>
<tr>
<td>Maximum Power Dissipation @ $T_A = 25^\circ$C</td>
<td>$P_{MAX}$</td>
<td>0.77</td>
<td>W</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>$T_J$</td>
<td>-40 to 125</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$T_{STG}$</td>
<td>-55 to 150</td>
<td>°C</td>
</tr>
</tbody>
</table>

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and exceeds the following tests:
   - Machine Model 200 V per JEDEC standard JESD22, Method A115.
   - Pin 16 is the high voltage startup of the device and is rated to the maximum rating of the part, 500 V.

2. This device contains Latchup protection and exceeds ±100 mA per JEDEC Standard JESD78.
Figure 3. Typical Application Schematic
### ELECTRICAL CHARACTERISTICS

(VCC = 15 V, VAC IN = 3.8 V, VFF = 2.0 V, VLatch = open, VISPOS = −100 mV, COUTA = 1 nF, CT = 470 pF, CAVG = 0.27 nF, CLatch = 0.1 nF, CM = 10 nF, RAVG = 76.8 kΩ, Rdelay = 49.9 kΩ, COUTB = 330 pF, RRC = 43 kΩ. For typical Value TJ = 25°C, for min/max values TJ = −40°C to 125°C, unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Condition</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>OSCILLATOR</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequency</td>
<td></td>
<td>fosc</td>
<td>90</td>
<td>100</td>
<td>110</td>
<td>kHz</td>
</tr>
<tr>
<td>Frequency Modulation in Percentage of fosc</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ramp Peak Voltage</td>
<td></td>
<td>VCT(peak)</td>
<td>4.0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Ramp Valley Voltage</td>
<td></td>
<td>VCT(valley)</td>
<td>0.10</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Maximum Duty Ratio</td>
<td>Rdelay = open</td>
<td>D</td>
<td>94</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Ramp Compensation Peak Voltage</td>
<td></td>
<td>VRCOMP(peak)</td>
<td>4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td><strong>AC ERROR AMPLIFIER</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Offset Voltage (Note 3)</td>
<td>Ramp IAVG, VFB = 0 V</td>
<td>ACVIO</td>
<td>40</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Error Amplifier Transconductance</td>
<td></td>
<td>gm</td>
<td>100</td>
<td></td>
<td></td>
<td>μS</td>
</tr>
<tr>
<td>Source Current</td>
<td>VAC COMP = 2.0 V, VAC IN = 2.0 V, VFF = 1.0 V</td>
<td>IEA(source)</td>
<td>25</td>
<td>70</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>Sink Current</td>
<td>VAC COMP = 2.0 V, VAC IN = 2.0 V, VFF = 5.0 V</td>
<td>IEA(sink)</td>
<td>−25</td>
<td>−70</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td><strong>CURRENT AMPLIFIER</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>VISPOS = 0 V</td>
<td>CAbias</td>
<td>40</td>
<td>53</td>
<td>80</td>
<td>μA</td>
</tr>
<tr>
<td>Input Offset Voltage</td>
<td>VAC COMP = 5.0 V, VISpos = 0 V</td>
<td>CAVIO</td>
<td>−20</td>
<td>0</td>
<td>20</td>
<td>mV</td>
</tr>
<tr>
<td>Current Limit Threshold</td>
<td>force OUTA high, VAC COMP = 3.0 V, ramp VISPOS, VRamp_Comp = open</td>
<td>VILIM</td>
<td>0.695</td>
<td>0.74</td>
<td>0.77</td>
<td>V</td>
</tr>
<tr>
<td>Leading Edge Blanking Duration</td>
<td></td>
<td>ILEB</td>
<td>−200</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Bandwidth</td>
<td></td>
<td></td>
<td>1.5</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>PWM Output Voltage Gain</td>
<td>PWMk = 4(VILIM − CAVIO)</td>
<td>PWMk</td>
<td>4.0</td>
<td>5.3</td>
<td>6.0</td>
<td>V/V</td>
</tr>
<tr>
<td>Current Limit Voltage Gain (See Current Sense Section)</td>
<td>ISVK =</td>
<td>VAVG/(VSPOS)</td>
<td>ISVk</td>
<td>15.4</td>
<td>18.5</td>
<td>23</td>
</tr>
<tr>
<td><strong>REFERENCE GENERATOR</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reference Generator Gain</td>
<td></td>
<td>k</td>
<td>−0.55</td>
<td>−0.55</td>
<td>−0.55</td>
<td>V</td>
</tr>
<tr>
<td>Reference Generator output voltage (low input ac line and full load)</td>
<td>VAC IN = 1.2 V, VFF = 0.765 V, VFB = 4 V</td>
<td>RGout1</td>
<td>3.61</td>
<td>4.36</td>
<td>4.94</td>
<td>Vpk</td>
</tr>
<tr>
<td>Reference Generator output voltage (high input ac line and full load)</td>
<td>VAC IN = 3.75 V, VFF = 2.39 V, VFB = 4.0 V</td>
<td>RGout2</td>
<td>1.16</td>
<td>1.35</td>
<td>1.61</td>
<td>Vpk</td>
</tr>
<tr>
<td>Reference Generator output Voltage (low input as line and minimum load)</td>
<td>VAC IN = 1.2 V, VFF = 0.765 V, VFB = 2.0 V</td>
<td>RGout3</td>
<td>1.85</td>
<td>2.18</td>
<td>2.58</td>
<td>Vpk</td>
</tr>
<tr>
<td>Reference Generator output voltage (high input ac line and minimum load)</td>
<td>VAC IN = 3.75 V, VFF = 2.39 V, VFB = 2.0 V</td>
<td>RGout4</td>
<td>0.55</td>
<td>0.65</td>
<td>0.78</td>
<td>Vpk</td>
</tr>
<tr>
<td>Reference Generator output offset voltage</td>
<td></td>
<td>RGoffset</td>
<td>−100</td>
<td>−100</td>
<td>−100</td>
<td>mV</td>
</tr>
</tbody>
</table>

3. Guaranteed by Design
ELECTRICAL CHARACTERISTICS (VCC = 15 V, VAC IN = 3.8 V, VFB = 2.0 V, VFF = 2.4 V, VLatch = open, VISPOS = −100 mV, COUTA = 1 nF, CT = 470 pF, CIAVG = 0.27 nF, CLatch = 0.1 nF, CM = 10 nF, RI AVG = 76.8 kΩ, R delay = 49.9 kΩ, COUTB = 330 pF, FRRC = 43 kΩ. For typical Value Tj = 25°C, for min/max values Tj = −40°C to 125°C, unless otherwise noted)

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<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>AC INPUT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Bias Current Into Reference Multiplier &amp; Current Compensation Amplifier</td>
<td></td>
<td>IAC IN(IB)</td>
<td>–</td>
<td>0.01</td>
<td>–</td>
<td>μA</td>
</tr>
<tr>
<td><strong>DRIVE OUTPUTS A and B</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Drive Resistance (Thermally Limited)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OUTA Sink</td>
<td>VOUTA = 1 V</td>
<td>RSNK1</td>
<td>–</td>
<td>8</td>
<td>18</td>
<td>Ω</td>
</tr>
<tr>
<td>OUTA Source</td>
<td>IOUTA = 100 mA</td>
<td>RSRC1</td>
<td>–</td>
<td>10.8</td>
<td>24</td>
<td></td>
</tr>
<tr>
<td>OUTB Sink</td>
<td>VOUTB = 1 V</td>
<td>RSNK2</td>
<td>–</td>
<td>10</td>
<td>22</td>
<td></td>
</tr>
<tr>
<td>OUTB Source</td>
<td>IOUTB = 100 mA</td>
<td>RSRC2</td>
<td>–</td>
<td>21</td>
<td>44</td>
<td></td>
</tr>
<tr>
<td>Rise Time (10% to 90%)</td>
<td></td>
<td>t1</td>
<td>–</td>
<td>40</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>t2</td>
<td>–</td>
<td>25</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>Fall Time (90% to 10%)</td>
<td></td>
<td>t1</td>
<td>–</td>
<td>20</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>t2</td>
<td>–</td>
<td>10</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>DRV Low Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OUTA</td>
<td>IOUTA = 100 μA</td>
<td>VOUTA(low)</td>
<td>–</td>
<td>1.0</td>
<td>100</td>
<td>mV</td>
</tr>
<tr>
<td>OUTB</td>
<td>IOUTB = 100 μA</td>
<td>VOUTB(low)</td>
<td>–</td>
<td>1.0</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>Non–Overlap Adjustable Delay Range (Note 3)</td>
<td></td>
<td>t_delay(range)</td>
<td>0.08</td>
<td>–</td>
<td>2.8</td>
<td>μs</td>
</tr>
<tr>
<td>Non–Overlap Adjustable Delay</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Leading</td>
<td></td>
<td>t_delay(lead)</td>
<td>250</td>
<td>250</td>
<td>550</td>
<td>ns</td>
</tr>
<tr>
<td>Trailing</td>
<td></td>
<td>t_delay(trail)</td>
<td>250</td>
<td>450</td>
<td>550</td>
<td></td>
</tr>
<tr>
<td>Non–Overlap Adjustable Delay Matching</td>
<td></td>
<td>t_delay(match)</td>
<td>–</td>
<td>–</td>
<td>55</td>
<td>%</td>
</tr>
<tr>
<td><strong>Soft–Skip™</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Skip Synchronization to ac Line Voltage Threshold</td>
<td>VACIN Increasing, VFB = 1.5 V</td>
<td>VSSKIP(SYNC)</td>
<td>210</td>
<td>267</td>
<td>325</td>
<td>mV</td>
</tr>
<tr>
<td>Skip Synchronization to ac Line Voltage Threshold Hysteresis</td>
<td>VACIN Decreasing</td>
<td>VSSKIP(SYNCHYS)</td>
<td>–</td>
<td>40</td>
<td>–</td>
<td>mV</td>
</tr>
<tr>
<td>Skip Ramp Period (Note 3)</td>
<td></td>
<td>ISKIP</td>
<td>–</td>
<td>2.5</td>
<td>–</td>
<td>ms</td>
</tr>
<tr>
<td>Skip Voltage Threshold NCP1652</td>
<td></td>
<td>VSSKIP</td>
<td>1.04</td>
<td>1.24</td>
<td>1.56</td>
<td>V</td>
</tr>
<tr>
<td>NCP1652A</td>
<td>0.36</td>
<td>0.41</td>
<td>0.46</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Skip Voltage Hysteresis</td>
<td></td>
<td>VSSKIP(HYS)</td>
<td>45</td>
<td>90</td>
<td>140</td>
<td>mV</td>
</tr>
<tr>
<td>Skip Transient Load Detect Threshold (Note 3)</td>
<td></td>
<td>VSSKIP(TLD) = VSSKIP +0.55 V</td>
<td>VSSKIP(TLD)</td>
<td>–</td>
<td>1.75</td>
<td>–</td>
</tr>
<tr>
<td><strong>FEEDBACK INPUT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pull–Up Current Source</td>
<td>VFB = 0.5 V</td>
<td>IFB</td>
<td>600</td>
<td>750</td>
<td>920</td>
<td>μA</td>
</tr>
<tr>
<td>Pull–Up Resistor</td>
<td></td>
<td>RFB</td>
<td>–</td>
<td>6.7</td>
<td>–</td>
<td>kΩ</td>
</tr>
<tr>
<td>Open Circuit Voltage</td>
<td></td>
<td>VFB(open)</td>
<td>5.3</td>
<td>5.7</td>
<td>6.3</td>
<td>V</td>
</tr>
<tr>
<td><strong>STARTUP AND SUPPLY CIRCUITS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Startup Threshold</td>
<td>VCC Increasing</td>
<td>VCC(on)</td>
<td>14.3</td>
<td>15.4</td>
<td>16.3</td>
<td>V</td>
</tr>
<tr>
<td>Minimum Operating Voltage</td>
<td>VCC Decreasing</td>
<td>VCC(off)</td>
<td>9.3</td>
<td>10.2</td>
<td>11.3</td>
<td></td>
</tr>
<tr>
<td>Logic Reset Voltage</td>
<td>VCC Decreasing</td>
<td>VCC(reset)</td>
<td>–</td>
<td>7.0</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>Inhibit Threshold Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>VHV = 40 V, Iinhibit = 500 μA</td>
<td>VINHIBIT</td>
<td>–</td>
<td>0.83</td>
<td>1.15</td>
<td></td>
</tr>
</tbody>
</table>
**ELECTRICAL CHARACTERISTICS**  
(V<sub>CC</sub> = 15 V, V<sub>AC IN</sub> = 3.8 V, V<sub>FF</sub> = 2.0 V, V<sub>Latch</sub> = 2.4 V, V<sub>Latch</sub> = open, V<sub>ISPOS</sub> = -100 mV,  
C<sub>OUTA</sub> = 1 nF, C<sub>T</sub> = 470 pF, C<sub>AVG</sub> = 0.27 nF, C<sub>Latch</sub> = 0.1 nF, C<sub>M</sub> = 10 nF, R<sub>AVG</sub> = 76.8 kΩ, R<sub>delay</sub> = 49.9 kΩ,  
C<sub>OUTB</sub> = 330 pF, R<sub>RC</sub> = 43 kΩ. For typical Value T<sub>J</sub> = 25°C, for min/max values T<sub>J</sub> = −40°C to 125°C, unless otherwise noted.

### STARTUP AND SUPPLY CIRCUITS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Condition</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inhibit Bias Current</td>
<td>( V_{HV} = 40 \text{ V}, V_{CC} = 0.8 \times V_{inhibit} )</td>
<td>( I_{inhibit} )</td>
<td>40</td>
<td>-</td>
<td>500</td>
<td>µA</td>
</tr>
<tr>
<td>Minimum Startup Voltage</td>
<td>( I_{start} = 0.5 \text{ mA}, V_{CC} = V_{CC(on)} - 0.5 \text{ V} )</td>
<td>( V_{start(min)} )</td>
<td>-</td>
<td>-</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td>Startup Current</td>
<td>( V_{CC} = V_{CC(on)} - 0.5 \text{ V}, V_{FB} = \text{Open} )</td>
<td>( I_{start} )</td>
<td>3.0</td>
<td>5.62</td>
<td>8.0</td>
<td>mA</td>
</tr>
</tbody>
</table>
| Off–State Leakage Current        | \( V_{HV} = 400 \text{ V}, T_J = 25°C \)  
\( T_J = -40°C \) to 125°C  
\( I_{HV(off)} \) | -    | 17   | 40   | 80   | µA   |
| Supply Current                    |                                                     |         |      |      |      | mA   |
| Device Disabled (Overload)        |                                                     |         |      |      |      | mA   |
| Device Switching                  | \( V_{FB} = \text{Open} \)  
\( f_{OSC} = 100 \text{ kHz} \)  
\( I_{CC1} \) | -    | 6.72 | 1.2  |      | mA   |
| Device Switching                  |                                                     |         |      |      |      | mA   |

### FAULT PROTECTION

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Condition</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overload Timer</td>
<td></td>
<td>( I_{OVLVD} )</td>
<td>120</td>
<td>162</td>
<td>360</td>
<td>ms</td>
</tr>
<tr>
<td>Overload Detect Threshold</td>
<td></td>
<td>( V_{OVLVD} )</td>
<td>4.7</td>
<td>4.9</td>
<td>5.2</td>
<td>V</td>
</tr>
</tbody>
</table>
| Brown–Out Detect Threshold        | \( V_{FF} \) Decreasing, \( V_{FB} = 2.5 \text{ V}, \)  
\( V_{AC IN} = 2.0 \text{ V} \)  
\( V_{BO(low)} \) | 0.41  | 0.45 | 0.49 | V    |
| Brown–Out Exit Threshold          | \( V_{FF} \) Increasing, \( V_{FB} = 2.5 \text{ V}, \)  
\( V_{AC IN} = 2.0 \text{ V} \)  
\( V_{BO(high)} \) | 0.57  | 0.63 | 0.69 | V    |
| Brown–Out Hysteresis              |                                                     | \( V_{BO(HYS)} \) | -    | 174  | -    | mV   |

### LATCH INPUT

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Condition</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
</table>
| Pull–Down Latch Voltage Threshold | \( V_{Latch} \) Decreasing  
\( V_{Latch(low)} \) | 0.9    | 0.98 | 1.1  | V    |
| Pull–Up Latch Voltage Threshold   | \( V_{Latch} \) Increasing  
\( V_{latch(high)} \) | 5.6    | 7.0  | 8.4  | V    |
| Latch Propagation Delay           | \( V_{Latch} = V_{latch(high)} \)  
\( I_{latch(delay)} \) | 30    | 56   | 90   | µs   |
| Latch Clamp Current (Going Out)   | \( V_{Latch} = 1.5 \text{ V} \)  
\( I_{latch(clamp)} \) | 42    | 51   | 58   | µA   |
| Latch Clamp Voltage (ILatch Going In) | \( I_{Latch} = 50 \text{ µA} \)  
\( V_{latch(clamp)} \) | 2.5   | 3.27 | 4.5  | V    |
| Latch–Off Current Shutdown (Going In) | \( V_{Latch} \) Increasing  
\( I_{latch(shdn)} \) | -     | 95   | -    | µA   |

3. Guaranteed by Design
Figure 4. Oscillator Frequency ($f_{OSC}$) vs. Junction Temperature

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Figure 22. OUTB Low Voltage vs. Junction Temperature

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Figure 39. Overload Timer vs. Junction Temperature

Figure 40. Overload Detect Threshold vs. Junction Temperature

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Figure 43. Brown-Out Hysteresis vs. Junction Temperature
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**Figure 46.** Latch Pull–Up Voltage Threshold vs. Junction Temperature

**Figure 47.** Latch Propagation Delay vs. Junction Temperature

**Figure 48.** Latch Clamp Current vs. Junction Temperature
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Figure 50. Latch–Off Current Shutdown vs. Junction Temperature
**Introduction**

The NCP1652 is a highly integrated controller combining PFC and an isolated step down ac–dc power conversion in a single stage, resulting in a lower cost and reduced part count solution. This controller is ideal for notebook adapters, battery chargers and other off–line applications with power requirements between 75 W and 150 W with an output voltage greater than 12 V. The single stage is based on the flyback converter and it is designed to operate in CCM or DCM modes.

**Power Factor Correction (PFC) Introduction**

Power factor correction shapes the input current of off–line power supplies to maximize the real power available from the mains. Ideally, the electrical appliance should present a load that emulates a pure resistor, in which case the reactive power drawn by the device is zero. Inherent in this scenario is the freedom from input current harmonics. The current is a perfect replica of the input voltage (usually a sine wave) and is exactly in phase with it. In this case the current drawn from the mains is at a minimum for the real power required to perform the needed work, and this minimizes losses and costs associated not only with the distribution of the power, but also with the generation of the power and the capital equipment involved in the process. The freedom from harmonics also minimizes interference with other devices being powered from the same source.

Another reason to employ PFC in many of today’s power supplies is to comply with regulatory requirements. Today, electrical equipment in Europe must comply with the European Norm EN61000–3–2. This requirement applies to most electrical appliances with input power of 75 W or greater, and it specifies the maximum amplitude of line–frequency harmonics up to and including the 39th harmonic. While this requirement is not yet in place in the US, power supply manufacturers attempting to sell products worldwide are designing for compliance with this requirement.

**Typical Power Supply with PFC**

A typical power supply consists of a boost PFC preregulator creating an intermediate ~400 V bus and an isolated dc–dc converter producing the desired output voltage as shown in Figure 51. This architecture has two power stages.

![Figure 51. Typical Two Stage Power Converter](http://onsemi.com)

A two stage architecture allows optimization of each individual power stage. It is commonly used because of designer familiarity and a vast range of available components. But, because it processes the power twice, the search is always on for a more compact and power efficient solution.

The NCP1652 controller offers the convenience of shrinking the front–end converter (PFC preregulator) and the dc–dc converter into a single power processing stage as shown in Figure 52.

![Figure 52. Single Stage Power Converter](http://onsemi.com)

This approach significantly reduces the component count. The NCP1652 based solution requires only one each of MOSFET, magnetic element, output rectifier (low voltage) and output capacitor (low voltage). In contrast, the 2–stage solution requires two or more of the above–listed components. Elimination of certain high–voltage components (e.g. high voltage capacitor and high voltage PFC diode) has significant impact on the system design. The resultant cost savings and reliability improvement are often worth the effort of designing a new converter.

**Single PFC Stage**

While the single stage offers certain benefits, it is important to recognize that it is not a recommended solution for all requirements. The following three limitations apply to the single stage approach:

- The output voltage ripple will have a 2x line frequency component (120 Hz for North American applications) that can not be eliminated easily. The cause of this ripple is the elimination of the energy storage element that is typically the boost output capacitor in the 2–stage solution. The only way to reduce the ripple is to increase the output filter capacitance. The required value of capacitance is inversely proportional to the output voltage – hence this approach is not recommended for low voltage outputs such as 3.3 V or 5 V. However, if there is a follow–on dc–dc converter stage or a battery after the single stage converter, the low frequency ripple should not cause any concerns.

- The hold–up time will not be as good as the 2–stage approach – again due to the lack of an intermediate energy storage element.

- In a single stage converter, one FET processes all the power – that is both a benefit and a limitation as the stress on that main MOSFET is relatively higher. Similarly, the magnetic component (flyback transformer/inductor) can not be optimized as well as in
the 2–stage solution. As a result, potentially higher leakage inductance induces higher voltage spikes (like the one shown in Figure 53) on the MOSFET drain. This may require a MOSFET with a higher voltage rating compared to similar dc–input flyback applications.

![Figure 53. Typical Drain Voltage Waveform of a Flyback Main Switch](image)

There are a few methods to clamp the voltage spike on the main switch, a resistor–capacitor–diode (RCD) clamp, a transient voltage suppressor (TVS) or an active clamp using a MOSFET and capacitor can be used as shown in Figures 54 to 56.

![Figure 54. RCD Clamp](image)

![Figure 55. TVS Clamp](image)

![Figure 56. Active Clamp](image)

The first two methods result in dissipation of the leakage energy in the clamping circuits – the dissipation is proportional to $L I^2$ where $L$ is the leakage inductance of the transformer and $I$ is the peak of the switch current at turn–off. An RDC snubber is simple and has the lowest cost, but constantly dissipates power. A TVS provides good voltage clamping at a slightly higher cost and dissipates power only when the drain voltage exceeds the voltage rating of the TVS.

The active clamp circuit provides an intriguing alternative to the other methods. It requires addition of a MOSFET and a high voltage capacitor as part of the active clamp circuit, thus adding complexity, but it results in a complete reuse of the leakage inductance energy. As a result, the transformer construction is no longer critical and one can use cheaper cost solution. Also, the active clamp circuit reduces the voltage stress on the primary switch and that can lead to usage of lower cost or lower on resistance ($R_{DS(on)}$) MOSFET. Finally, the turn–on switching losses are eliminated because the active clamp circuit allows the discharge of the MOSFET $C_{oss}$ capacitance prior to the turn–on. The energy stored in the leakage inductance is utilized for this transition.

In many applications, the added complexity of the active clamp circuit may not be justified. However, the OUTB of the NCP1652 is also usable for another purpose, synchronous rectification control. Synchronous rectification for flyback converters is an emerging requirement for flyback converters. The OUTB signal from NCP1652 is ideal for interfacing with a secondary side synchronous rectifier controller such as NCP4303 as shown in Figure 57. As shown in Figure 57, using the OUTB (coupled through pulse transformer or Y–capacitor) as a trigger for the NCP4303 allows guaranteed turn–off of the secondary side synchronous MOSFET prior to turn–on of the primary switch. In any CCM flyback converter, this is a critical requirement to prevent cross–conduction and NCP1652 and NCP4303 combination is the first such chipset that guarantees the operation without cross–conduction.

http://onsemi.com

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The NCP1652 incorporates a secondary driver, OUTB, with adjustable non overlap delay for controlling a synchronous rectifier switch in the secondary side, an active clamp switch in the primary or both. In addition, the controller features a proprietary Soft-Skip™ to reduce acoustic noise at light loads. Other features found in the NCP1652 include a high voltage startup circuit, voltage feedforward, brown out detector, internal overload timer, latch input and a high accuracy multiplier.

**NCP1652 PFC Loop**

The NCP1652 incorporates a modified version of average current mode control used for achieving the unity power factor. The PFC section includes a variable reference generator, a low frequency voltage regulation error amplifier (AC error AMP), ramp compensation (Ramp Comp) and current shaping network. These blocks are shown in the lower portion of the block diagram (Figure 51).

The inputs to the reference generator include feedback signal (FB), scaled AC input signal (AC_IN) and feedforward input (V_FF). The output of the reference generator is a rectified version of the input sine-wave scaled by the FB and V_FF values. The reference amplitude is proportional to the FB and inversely proportional to the square of the V_FF. This, for higher load levels and/or lower input voltage, the signal would be higher.

The function of the AC error amp is to force the average current output of the current sense amplifier to match the reference generator output. The output of the AC error amplifier is compensated to prevent response to fast events. This output (V_error) is fed into the PWM comparator through a reference buffer. The PWM comparator sums the V_error and the instantaneous current and compares it to a 4.0 V threshold to provide the desired duty cycle control. Ramp compensation is also added to the input signal to allow CCM operation above 50% duty cycle.

**High Voltage Startup Circuit**

The NCP1652 internal high voltage startup circuit eliminates the need for external startup components and provides a faster startup time compared to an external startup resistor. The startup circuit consists of a constant current source that supplies current from the HV pin to the supply capacitor on the V_CC pin (C_CC). The startup current (I_{start}) is typically 5.5 mA.

The OUTA and OUTB drivers are enabled and the startup current source is disabled once the V_CC voltage reaches V_CC(on), typically 15.3 V. The controller is then biased by the V_CC capacitor. The drivers are disabled if V_CC decays to its minimum operating threshold (V_CC(off)) typically 10.3 V. Upon reaching V_CC(off) the gate drivers are disabled. The V_CC capacitor should be sized such V_CC is kept above V_CC(off) while the auxiliary voltage is building up. Otherwise, the system will not start.

The controller operates in double hiccup mode while in overload or V_CC(off). A double hiccup fault disables the drivers, sets the controller in a low current mode and allows V_CC to discharge to V_CC(off). This cycle is repeated twice to minimize power dissipation in external components during a fault event. Figure 58 shows double hiccup mode operation. A soft-start sequence is initiated the second time V_CC reaches V_CC(on). If the controller is latched upon reaching V_CC(on), the controller stays in hiccup mode. During this mode, V_CC never drops below V_CC(reset), the controller logic reset level. This prevents latched faults to be cleared unless power to the controller is completely removed (i.e. unplugging the supply from the AC line).
An internal supervisory circuit monitors the $V_{CC}$ voltage to prevent the controller from dissipating excessive power if the $V_{CC}$ pin is accidentally grounded. A lower level current source ($I_{inhibit}$) charges $C_{CC}$ from 0 V to $V_{inhibit}$ typically 0.85 V. Once $V_{CC}$ exceeds $V_{inhibit}$, the startup current source is enabled. This behavior is illustrated in Figure 59. This slightly increases the total time to charge $V_{CC}$, but it is generally not noticeable.

The rectified ac line voltage is provided to the power stage to achieve accurate PFC. Filtering the rectified ac line voltage with a large bulk capacitor distorts the PFC in a single stage PFC converter. A peak charger is needed to bias the HV pin as shown in Figure 60. Otherwise, the HV pin follows the ac line and the startup circuit is disabled every time the ac line voltage approaches 0 V. The $V_{CC}$ capacitor is sized to bias the controller during power up.
The startup circuit is rated at a maximum voltage of 500 V. Power dissipation should be controlled to avoid exceeding the maximum power dissipation of the controller. If dissipation on the controller is excessive, a resistor can be placed in series with the HV pin. This will reduce power dissipation on the controller and transfer it to the series resistor.

**Drive Outputs**

The NCP1652 has out of phase output drivers with an adjustable non-overlap delay ($t_d$). The main output, OUTA, drives the primary MOSFET. The secondary output, OUTB, is designed to provide a logic signal used to control a synchronous rectification switch in the secondary side, an active clamp switch in the primary or both. The outputs are biased directly from $V_{CC}$ and their high state voltage is approximately $V_{CC}$.

OUTA has a source resistance of 13 $\Omega$ (typical) and a sink resistance of 8.0 $\Omega$ (typical) OUTB has a source resistance 22 $\Omega$ (typical) and a sink resistance of 10 $\Omega$ (typical). OUTB is a purposely sized smaller than OUTA because the gate charge of an active switch or logic used with synchronous rectification is usually less than that of the primary MOSFET. If a higher drive capability is required, an external discrete driver can be used.

The drivers are enabled once $V_{CC}$ reaches $V_{CC(on)}$ and there are no faults present. They are disabled once $V_{CC}$ discharges to $V_{CC(off)}$. OUTB is always the last pulse generated when the outputs are disabled due to a fault (latch-off, $V_{CC(off)}$, overload, or brown-out). The last pulse terminates at the end of the clock cycle. This ensures the active clamp capacitor is reset.

The high current drive capability of OUTA and OUTB may generate voltage spikes during switch transitions due to parasitic board inductance. Shortening the connection length between the drivers and their loads and using wider connections will reduce inductance–induce spikes.

**Adjustable Dead Time**

OUTA and OUTB have an adjustable dead time between transitions to prevent simultaneous conduction of the main and synchronous rectifier or active clamp MOSFETs. The delay is also used to optimize the turn–off transition of the active clamp switch to achieve zero–volt switching of the main switch in an active clamp topology. Figure 61 shows the timing relationship between OUTA and OUTB.

$$t_{delay}(\text{in ns}) = 8.0 \times R_{delay}(\text{in k}\Omega)$$

$R_{delay}$ varying between 10 $k\Omega$ and 230 $k\Omega$

**AC Error Amplifier and Buffer**

The AC error amplifier (EA) shapes the input current into a high quality sine wave by forcing the filtered input current to follow the output of the reference generator. The output of the reference generator is a full wave rectified ac signal and it is applied to the non inverting input of the EA. The filtered input current, $I_{in}$, is the current sense signal at the
ISpos pin multiplied by the current sense amplifier gain. It is applied to the inverting input of the AC EA. The AC EA is a transconductance amplifier. A transconductance amplifier generates an output current proportional to its differential input voltage. This amplifier has a nominal gain of 100 \( \mu \)S (or 0.0001 A/V). That is, an input voltage difference of 10 mV causes the output current to change by 1.0 \( \mu \)A. The AC EA has typical source and sink currents of 70 \( \mu \)A.

The filtered input current is a high frequency signal. A low frequency pole forces the average input current to follow the reference generator output. A pole-zero pair is created by placing a \( (R_{COMP}) \) and capacitor \( (C_{COMP}) \) series combination at the output of the AC EA. The AC COMP pin provides access to the AC EA output.

The output of the AC EA is inverted and converted into a current using a second transconductance amplifier. The output of the inverting transconductance amplifier is \( V_{ACEA(buffer)} \). Figure 62 shows the circuit schematic of the AC EA buffer. The AC EA buffer output current, \( I_{ACEA(out)} \), is given by Equation 1.

\[
I_{ACEA(out)} = \left( \frac{2.8 - V_{ACEA}}{37.33k} \right) \cdot 4 \quad (eq. 1)
\]

The voltage at the PWN non-inverting input is determined by \( I_{ACEA(out)} \), the instantaneous switch current along and the ramp compensation current. OUTA is terminated once the voltage at the PWM non-inverting input reaches 4 V.

**Current Sense Amplifier**

A voltage proportional to the main switch current is applied to the current sense input, ISPOS. The current sense amplifier is a wide bandwidth amplifier with a differential input. The current sense amplifier has two outputs, PWM Output and \( I_{AVG} \) Output. The PWM Output is the instantaneous switch current which is filtered by the internal leading edge blanking (LEB) circuitry prior to applying it to the PWM Comparator non-inverting input. The second output is a filtered current signal resembling the average value of the input current. Figure 63 shows the internal architecture of the current sense amplifier.
Caution should be exercised when designing a filter between the current sense resistor and the ISPOS input, due to the low impedance of this amplifier. Any series resistance due to a filter creates a voltage offset (VOS) due to its input bias current, CAbias. The input bias current is typically 60 μA. The voltage offset is given by Equation 2.

\[ V_{OS} = C_{A bias} \times R_{external} \]  
\[ \text{eq. 2} \]

The offset adds a positive offset to the current sense signal. The ac error amplifier will then try to compensate for the average output current which appears never to go to zero and cause additional zero crossing distortion.

A voltage proportional to the main switch current is applied to the ISPOS pin. The ISPOS pin voltage is converted into a current, \( i_1 \), and internally mirrored. Two internal currents are generated, \( I_{CS} \) and \( I_{AVG} \). \( I_{CS} \) is a high frequency signal which is a replica of the instantaneous switch current. \( I_{AVG} \) is a low frequency signal. The relationship between \( V_{ISPOS} \) and \( I_{CS} \) and \( I_{AVG} \) is given by Equation 3.

\[ I_{CS} = I_{IN} = \frac{V_{ISPOS}}{4k} \]  
\[ \text{eq. 3} \]

The PWM Output delivers current to the positive input of the PWM input where it is added to the AC EA and ramp compensation signal.

The \( I_{AVG} \) output generates a voltage signal to a buffer amplifier. This voltage signal is the product of \( I_{AVG} \) and an external \( R_{AVG} \) resistor filtered by the capacitor on the \( I_{AVG} \) pin, \( C_{AVG} \). The pole frequency, \( f_p \) set by \( C_{AVG} \) should be significantly below the switching frequency to remove the high frequency content. But, high enough to not to cause significant distortion to the input full wave rectified sinewave waveform. A properly filtered average current signal has twice the line frequency. Equation 4 shows the relationship between \( C_{AVG} \) (in nF) and \( f_p \) (in kHz).

\[ C_{AVG} = \frac{1}{2 \times \pi \times R_{AVG} \times f_p} \]  
\[ \text{eq. 4} \]
The gain of the low frequency current buffer is set by the resistor at the IAVG pin, RIAVG. RIAVG sets the scaling factor between the primary peak and primary average currents. The gain of the current sense amplifier, ACA, is given by Equation 5.

\[ A_{CA} = \frac{RI_{AVG}}{4k} \]  
(eq. 5)

The current sense signal is prone to leading edge spikes during the main switch turn on due to parasitic capacitance and inductance. This spike may cause incorrect operation of the PWM Comparator. Filtering the current sense signal will inevitably change the shape of the current pulse. The NCP1652 incorporates LEB circuitry to block the first 200 ns (typical) of each current pulse. This removes the leading edge spikes without altering the current signal waveform.

**Oscillator**

The oscillator controls the switching frequency, \( f \), the jitter frequency and the gain of the multiplier. The oscillator ramp is generated by charging the timing capacitor on the CT Pin, \( C_T \), with a 200 \( \mu \)A current source. This current source is tightly controlled during manufacturing to achieve a controlled and repeatable oscillator frequency. The current source turns off and \( C_T \) is immediately discharged with a pull down transistor once the oscillator ramp reaches its peak voltage, \( V_{CT(peak)} \), typically 4.0 V. The pull down transistor turns off and the charging current source turns on once the oscillator ramp reaches its valley voltage, \( V_{CT(valley)} \).

Figure 64 shows the resulting oscillator ramp and control circuitry.

The relationship between the oscillator frequency in kHz and timing capacitor in pF is given by Equation 6.

\[ C_T = \frac{47000}{f} \]  
(eq. 6)

A low frequency oscillator modulates the switching frequency, reducing the controller EMI signature and allowing the use of a smaller EMI filter. The frequency modulation or jitter is typically \( \pm 5\% \) of the oscillator frequency.
Output Overload

The Feedback Voltage, V_{FB}, is directly proportional to the output power of the converter. An internal 6.7 kΩ resistor pulls up the FB voltage to the internal 6.5 V reference. An external optocoupler pulls down the FB voltage to regulate the output voltage of the system. The optocoupler is off during power up and output overload conditions allowing the FB voltage to reach its maximum level.

The NCP1652 monitors the FB voltage to detect an overload condition. A typical startup time of a single PFC stage converter is around 100 ms. If the converter is out of regulation (FB voltage exceeds 5.0 V) for more than 150 ms (typical) the drivers are disabled and the controller enters the double hiccup mode to reduce the average power dissipation. A new startup sequence is initiated after the double hiccup is complete. This protection feature is critical to reduce power during an output short condition.

Soft–Skip™ Cycle Mode

The FB voltage reduces as the output power demand of the converter reduces. Once V_{FB} drops below the skip threshold, V_{SSKIP}, 1.30 V (typical) the drivers are disabled. The skip comparator hysteresis is typically 180 mV.

The converter output voltage starts to decay because no additional output power is delivered. As the output voltage decreases the feedback voltage increases to maintain the output voltage in regulation. This mode of operation is known as skip mode. The skip mode frequency is dependent of load loop gain and output capacitance and can create audible noise due to mechanical resonance in the transformer and snubber capacitor. A proprietary Soft–Skip™ mode reduces audible noise by slowly increasing the primary peak current until it reaches its maximum value. The minimum skip ramp period, t_{SSKIP}, is 2.5 ms. Figure 65 shows the relationship between V_{FB}, V_{SSKIP} and the primary current.

![Figure 65. Soft–Skip™ operation.](image)

Skip mode operation is synchronous of the ac line voltage. The NCP1652 disables Soft–Skip™ when the rectified ac line voltage drops to its valley level. This ensures the primary current always ramp up reducing audible noise. A skip event occurring as the ac line voltage is decreasing, causes the primary peak current to ramp down instead of ramp up. Once the skip period is over the primary current is only determined by the ac line voltage. A Soft–Skip™ event terminates once the AC–IN pin voltage decreases below 260 mV. A new Soft–Skip™ period starts once the voltage on the AC–IN pin increases to 260 mV.

An increase in output load current terminates a Soft–Skip™ event. A transient load detector terminates a Soft–Skip™ period once V_{FB} voltage exceeds V_{SSKIP} by more than 550 mV. This ensures the required output power is delivered during a load transient and the output voltage does not fall out of regulation. Figure 66 shows the relationship between Soft–Skip™ and the transient load detector.

![Figure 66. Load transient during Soft–Skip™](image)

The output of the Soft–Skip™ Comparator is or–ed with the PWM Comparator output to control the duty ratio. The Soft–Skip™ Comparator controls the duty ratio in skip mode and the PWM Comparator controls the duty cycle during normal operation. In skip mode, the non–inverting input of the Soft–Skip™ Comparator exceeds 4 V, disabling the drivers. As the FB voltage increases, the voltage at the non–inverting input is ramp down from 4 V to 0.2 V to enable the drivers.

Multiplier and Reference Generator

The NCP1652 uses a multiplier to regulate the average output power of the converter. This controller uses a proprietary concept for the multiplier used within the reference generator. This innovative design allows greatly improved accuracy compared to a conventional linear analog multiplier. The multiplier uses a PWM switching circuit to create a scalable output signal, with a very well defined gain.

The output of the multiplier is the ac-reference signal. The ac-reference signal is used to shape the input current. The multiplier has three inputs, the error signal from an external error amplifier (V_{FB}), the full wave rectified ac input (AC–IN) and the feedforward input (V_{FF}).

The FB signal from an external error amplifier circuit is applied to the V_{FB} pin via an optocoupler or other isolation circuit. The FB voltage is converted to a current with a V–I
The third input to the reference generator is the V_FF signal. The V_FF signal is a dc voltage proportional to the ac line voltage. A resistive voltage divider attenuates the full wave rectified line voltage between 0.7 and 5.0 V. The full wave rectified line is then averaged with a capacitor. The ac average voltage must be constant over each half cycle of the line. Line voltage ripple (120 Hz or 100 Hz) ripple on the V_FF signal adds ripple to the output of the multiplier. This will distort the ac reference signal and reduce the power factor and increase the line current distortion. Excessive filtering delays the feedforward signal reducing the line transient response. A good starting point is to set the filter time constant to one cycle of the line voltage. The user can then optimize the filter for line transient response versus power factor. The average voltage on the V_FF pin is:

\[ V_{\text{FF}} = \frac{2}{\pi} \frac{V_{\text{AC}, \text{peak}}}{2 \alpha} \]  

(eq. 7)

Where, \( \alpha \) is the voltage divider ratio, normally 0.01.

\[ V_{\text{AC}_\text{REF}} = k \frac{V_{\text{FB}} \cdot V_{\text{AC}_\text{IN}}}{V_{\text{FF}}^2} \]  

(eq. 8)

The multiplier transfer function is given by Equation 8. The output of the multiplier is the \( V_{\text{AC}_\text{REF}} \). It connects to the AC Error Amplifier.

where, \( k \) is the reference generator gain, typically 0.55. The output of the reference generator is clamped at 4.5 V to limit the maximum output power.

Feedforward maintains a constant input power independent of the line voltage. That is, for a given FB voltage, if the line voltage doubles (\( V_{\text{AC}_\text{IN}} \)), the feedforward term quadruples and reduces the output of the error amplifier in half to maintain the same input power.

**AC Error Amplifier Compensation**

A pole-zero pair is created by placing a series combination of \( R_{\text{COMP}} \) and \( C_{\text{COMP}} \) at the output of the AC error amplifier (EA). The value of the compensation components is...
dependent of the average input current and the instantaneous switch current. The gain of the average input current or slow loop is given by Equation 9.

\[ A_{LF} = \left( \frac{R_{RAC\_COMP}}{4k} \right) \cdot (gm \cdot R_{AC\_COMP}) \cdot (2.286) \]  
(eq. 9)

The low frequency gain is the product of the current sense averaging circuit, the transconductance amplifier and the gain of the AC error amplifier.

A current proportional to the instantaneous current is generated using a 4 kΩ resistor in the current sense amplifier input. This proportional current is applied to a 21.33 kΩ at the PWM comparator input to generate a current sense voltage signal. The high frequency or fast loop gain, \( A_{HF} \), is calculated using Equation 10.

\[ A_{HF} = \frac{21.33k}{4k} = 5.333 \]  
(eq. 10)

Equation 11 shows system stability requirements. That is, the high frequency gain has to be less than one half of the high frequency gain.

\[ \left( \frac{R_{I\_AVG}}{4k} \right) \cdot (gm \cdot R_{AC\_COMP}) \cdot (2.286) < \frac{5.333}{2} \]  
(eq. 11)

Equation 12 is obtained by re-arranging Equation 11 for \( R_{AC\_COMP} \). This equation provides the maximum value for \( R_{AC\_COMP} \).

\[ R_{AC\_COMP} < \frac{4666}{R_{I\_AVG} \cdot gm} \]  
(eq. 12)

The control loop zero, \( f_z \), is calculated using Equation 13. The control loop zero should be set at approximately at 1/10\(^{th}\) of the oscillator frequency, \( f_{OSC} \). The compensation capacitor is calculated using Equation 14.

\[ f_z = \frac{1}{2\pi \cdot C_{AC\_COMP} \cdot R_{AC\_COMP}} \]  
(eq. 13)

\[ C_{AC\_COMP} = \frac{1}{2\pi \cdot f_{OSC} \cdot 10 \cdot R_{AC\_COMP}} \]  
(eq. 14)

**Current Sense Resistor**

The PFC stage has two control loops. The first loop controls the average input current and the second loop controls the instantaneous current across the main switch. The current sense signal affects both loops. The current sense signal is fed into the positive input of the error amplifier to control the average input current. In addition, the current sense information together with the ramp compensation and error amplifier signal control the instantaneous primary peak current.

The primary peak current, \( I_{PK} \), is calculated using Equation 15.

\[ I_{PK} = \frac{\sqrt{2} \cdot P_{out}}{\eta \cdot V_{in(LL)} \cdot D} + \frac{V_{in(LL)} \cdot t_{on}}{0.88 \cdot 2 \cdot L_p} \]  
(eq. 15)

where, \( V_{in(LL)} \) is the low line ac input voltage, \( D \) is the duty ratio, \( P_{out} \) is the output power, \( P_{in} \) is the input power, \( \eta \) is the efficiency, \( L_p \) is the primary inductance and \( t_{on} \) is the on time. Typical efficiency for this topology is around 88%.

The current sense resistor is selected to achieve maximum signal resolution at the input of the ac reference amplifier. The maximum voltage input of the ac reference amplifier to prevent saturation is 4.5 V. This together with the instantaneous peak current is used to calculate the current sense resistor, \( R_{CS} \), using Equation 16.

\[ R_{CS} = 4.5 \cdot \frac{4k \cdot (V_{in(LL)} \cdot D)}{R_{I\_AVG} \cdot P_{in} \cdot \sqrt{2}} \]  
(eq. 16)

**Ramp Compensation**

Subharmonic oscillations are observed in peak current-mode controllers operating in continuous conduction mode with a duty ratio greater than 50%. Injecting a compensation ramp on the current sense signal eliminates the subharmonic oscillations. The amount of compensation is system dependent and it is determined by the inductor falling \( di/dt \).

The NCP1652 has built in ramp compensation to facilitate system design. The amount of ramp compensation is set by the user with a resistor, \( R_{R\_COMP} \), between the Ramp Comp pin and ground. The Ramp Comp pin buffers the oscillator ramp generated on the CT pin. The current across \( R_{R\_COMP} \) is internally mirrored with a 1:1.2 ratio. The inverted ac error amplifier and the instantaneous switch current signals are added to the ramp compensation mirrored current. The resulting current signal is applied to an internal 21.33 kΩ between the PWM Comparator non inverting input and ground as shown in Figure 64.

The maximum voltage contribution of the ramp compensation signal to the error signal, \( V_{R\_COMP} \), is given by Equation 17.

\[ V_{R\_COMP} = \frac{(1.2) \cdot (V_{CT\_peak}) \cdot (21.33k)}{R_{R\_COMP}} = \frac{102.38k}{R_{R\_COMP}} \]  
(eq. 17)

where, \( V_{CT\_peak} \) is the oscillator ramp peak voltage, typically 4.0 V.

For proper ramp compensation, the ramp signal should match the falling \( di/dt \) (which has been converted to a dv/dt) of the inductor at 50% duty cycle. Both the falling \( di/dt \) and output voltage need to be reflected by the transformer turns ratio to the primary side. Equations 18 through 23 assist in the derivation of equations for \( R_{CS} \) and \( R_{R\_COMP} \).

\[ \frac{di}{dt_{secondary}} = \frac{V_{out}}{L_S} = \frac{V_{out}}{L_p} \cdot \left( \frac{N_p}{N_s} \right)^2 \]  
(eq. 18)

\[ \frac{di}{dt_{primary}} = \frac{di}{dt_{secondary}} \cdot \frac{N_s}{N_p} = \frac{V_{out} \cdot N_p}{L_p \cdot N_s} \]  
(eq. 19)
\[ V_{\text{RCOMP}} = \frac{\text{di}}{\text{dt}_{\text{primary}}} \cdot T \cdot R_{\text{CS}} \cdot A_{\text{HF}} \quad \text{(eq. 20)} \]

\[ R_{\text{CS}} = \frac{N_S}{N_P} \cdot \frac{L_p \cdot 102.38k}{T \cdot A_{\text{HF}} \cdot V_{\text{out}} \cdot R_{\text{RCOMP}}} \quad \text{(eq. 21)} \]

At low line and full load, the output of the ac error amplifier output is nearly saturated in a low state. While the ac error amplifier output is saturated, \( I_{\text{ACEA}} \) is zero and does not contribute to the voltage across the internal 21.33 kΩ resistor on the PWM comparator non-inverting input. In this operation mode, the voltage across the 21.33 kΩ resistor is determined solely by the ramp compensation and the instantaneous switch current as given by Equation 22.

\[ V_{\text{ref(PWM)}} = \left( V_{\text{RCOMP}} \cdot \frac{t_{\text{on}}}{T} \right) + V_{\text{INST}} \quad \text{(eq. 22)} \]

The voltage reference of the PWM Comparator, \( V_{\text{REF(PWM)}} \), is 4 V. For these calculations, 3.8 V is used to provide some margin. The maximum instantaneous switch current voltage contribution, \( V_{\text{INST}} \), is given by Equation 23.

\[ V_{\text{INST}} = I_{\text{PK}} \cdot R_{\text{CS}} \cdot A_{\text{HF}} \quad \text{(eq. 23)} \]

Substituting Equation 23 in Equation 22, setting \( V_{\text{REF(PWM)}} \) at 3.8 V (provides margin) and solving for \( R_{\text{RCOMP}} \), Equation 24 is obtained.

\[ R_{\text{RCOMP}} = \frac{102.38k}{(3.8 - 5.333 \cdot I_{\text{PK}})} \cdot \frac{t_{\text{on}}}{T} \quad \text{(eq. 24)} \]

Replacing Equation 24 in Equation 21 we obtain:

\[ R_{\text{CS}} = \frac{3.8}{\left( \frac{N_P}{N_S} \cdot A_{\text{HF}} \cdot t_{\text{on}} \cdot I_{\text{PK}} \frac{t_{\text{on}}}{t_P} \right)} + 5.333 I_{\text{PK}} \quad \text{(eq. 25)} \]

**PWM Logic**

The PWM and logic circuits are comprised of a PWM comparator, an RS flip-flop (latch) and an OR gate. The latch is Set dominant which means that if both R and S are high the S signal will dominate and Q will be high, which will hold the power switch off.

The NCP1652 uses a pulse width modulation scheme based on a fixed frequency oscillator. The oscillator generates a voltage ramp as well as a pulse in sync with the falling edge of the ramp. The pulse is an input to the PWM Logic and Driver block. While the oscillator pulse is present, the latch is reset, and the output drive is in its low state. On the falling edge of the pulse, the OUTA goes high and the power switch begins conduction.

The instantaneous inductor current is summed with a current proportional to the ac error amplifier output voltage. This complex waveform is compared to the 4 V reference signal on the PWM comparator inverting input. When the signal at the non-inverting input to the PWM comparator exceeds 4 V, the output of the PWM comparator toggles to a high state which drives the Set input of the latch and turns the power switch off until the next clock cycle.

**Brown–Out**

The NCP1652 incorporates a brown–out detection circuit to prevent the controller operate at low ac line voltages and reduce stress in power components. A scaled version of the rectified line voltage is applied to the VFF Pin by means of a resistor divider. This voltage is used by the brown out detector.

A brown–out condition exists if the feedforward voltage is below the brown–out exit threshold, \( V_{\text{BO(high)}} \) typically 0.45 V. The brown–out detector has 180 mV hysteresis. The controller is enabled once \( V_{\text{FF}} \) is above 0.63 V and \( V_{\text{CC}} \) reaches \( V_{\text{CC(on)}} \). OUTB is the last drive pulse. Figure 68 shows the relationship between the brown–out, \( V_{\text{CC}} \), OUTA and OUTB signals.
Latch Input

The NCP1652 has a dedicated latch input to easily latch the controller during overtemperature and overvoltage faults (See Figure 69). The controller is latched if the Latch–Off pin voltage is pulled below 1 V or above 6.5 V. Once the controller is latched, OUTA is disabled and OUTB generates a final pulse that ends with the oscillator period. No more pulses are generated after OUTB is terminated. Figure 70 shows the relationship between the Latch–Off, VCC, OUTA and OUTB signals.
Figure 70. Relationship Between the Latch–Off, V_CC, OUTA and OUTB

The Latch–Off pin is clamped at 3.5 V. A 50 μA (typical) pull–up current source is always on and a 100 μA (typical) pull–down current source is enabled once the Latch–Off pin voltage reaches 3.5 V (typical). This effectively clamps the Latch–Off pin voltage at 3.5 V. A minimum pull–up or pull–down current of 50 μA is required to overcome the internal current sources and latch the controller. The Latch–Off input features a 50 μs (typical) filter to prevent latching the controller due to noise or a line surge event.

The startup circuit continues to cycle V_CC between V_CC(on) and V_CC(off) while the controller is in latch mode. The controller exits the latch mode once power to the system is removed and V_CC drops below V_CC(reset).

APPLICATION INFORMATION

ON Semiconductor provides an electronic design tool, facilitate design of the NCP1652 and reduce development cycle time. The design tool can be downloaded at www.onsemi.com. The electronic design tool allows the user to easily determine most of the system parameters of a single PFC stage. The tool evaluates the power stage as well as the frequency response of the system.

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package</th>
<th>Shipping†</th>
</tr>
</thead>
<tbody>
<tr>
<td>NCP1652DWR2G</td>
<td>SO–20 WB (Pb–Free)</td>
<td>1000 / Tape &amp; Reel</td>
</tr>
<tr>
<td>NCP1652DR2G</td>
<td>SO–16 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td>NCP1652ADR2G</td>
<td>SO–16 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
</tbody>
</table>

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

The products described herein (NCP1652), may be covered by one or more of the following U.S. patents; 6,373,734. There may be other patents pending.
NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

STYLE 1:
1. COLLECTOR
2. BASE
3. Emitter
4. NO CONNECTION
5. Emitter
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. Emitter
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

STYLE 4:
1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. CATHODE
15. CATHODE
16. CATHODE

STYLE 6:
1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. GATE, #4
11. ANODE
12. Source, #3
13. GATE, #2
14. Source, #2
15. GATE, #1
16. Source, #1

SOLDERING FOOTPRINT

DIMENSIONS: MILLIMETERS

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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

DATE 22 APR 2015

SOIC−20 WB
CASE 751D−05
ISSUE H

SCALE 1:1

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
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<table>
<thead>
<tr>
<th>DIM</th>
<th>MIN</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>0.18</td>
<td>0.25</td>
</tr>
<tr>
<td>b</td>
<td>0.35</td>
<td>0.39</td>
</tr>
<tr>
<td>c</td>
<td>0.23</td>
<td>0.27</td>
</tr>
<tr>
<td>D</td>
<td>12.65</td>
<td>12.95</td>
</tr>
<tr>
<td>E</td>
<td>7.40</td>
<td>7.60</td>
</tr>
<tr>
<td>e</td>
<td>1.275</td>
<td></td>
</tr>
<tr>
<td>h</td>
<td>10.05</td>
<td>10.35</td>
</tr>
<tr>
<td>L</td>
<td>0.25</td>
<td>0.30</td>
</tr>
<tr>
<td>φ</td>
<td>1.75</td>
<td></td>
</tr>
</tbody>
</table>

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " *", may or may not be present.

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