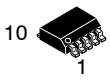
High-Voltage, Multimode Power Factor Controller

NCP1618



SOIC−9 NB
CASE 751BP

The NCP1618 is an innovative multimode power factor controller. The circuit naturally transitions from one operation mode to another depending the switching period duration so that the efficiency is optimized over the line/load range. In very−light−load conditions, the circuit can enter the soft−SKIP mode for minimized losses.

Housed in a SO−9 package, the circuit further incorporates the features necessary for robust and compact PFC stages, with few external components.

Multimode Operation

- Multimode Operation for Optimized Operation over the Line/Load Range:
  - Continuous Conduction Mode (CCM) in Heavy−Load Conditions
  - Frequency−Clamped Critical Conduction Mode (FCCrM) in Medium− and Light−Load Conditions
  - FCCrM: Critical Conduction Mode (CrM) when the CrM Switching Frequency is Lower than 130 kHz, Discontinuous Conduction Mode (DCM) at 130 kHz Otherwise
  - DCM Frequency Reduction in Light Load Conditions
  - Minimum DCM Frequency Forced above 25 kHz
  - Valley Turn−On in FCCrM
  - Soft−SKIP Mode in Very Light Load Conditions
- Near−Unity Power Factor in All Modes (Except Soft−SKIP Mode)
- Firm Control of the Switching Frequency between 25 kHz and 130 kHz

General Features

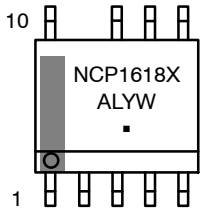
- High−Voltage Start−Up Current Source for V_{CC} Capacitor Charge at Startup
- Internal Compensation of the Regulation Loop
- X2 Cap Discharge Function
- Fast Line / Load Transient Compensation (Dynamic Response Enhancer)
- Large V_{CC} Operating Range (9.5 V to 35 V)
- Line Range Detection
- pfcOK Signal For Enabling/Disabling the Downstream Converter
- Jittering for Easing EMI Filtering

Protection Features

- Soft− and Fast−Overvoltage Protection
- Line−Sag and Brown−Out Detection
- 2−Level Over Current Detection
- Bulk Under−Voltage Detection
- OVP2: Redundant Over−Voltage Protection Using the ZCD Pin
- Thermal Shutdown

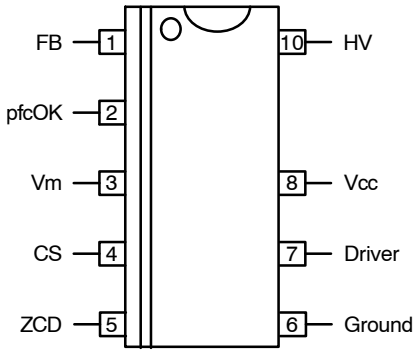
This document contains information on some products that are still under development. **onsemi** reserves the right to change or discontinue these products without notice.

MARKING DIAGRAM



NCP1618X	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 29 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 29.

Typical Applications

- PC Power Supplies
- All Off−Line Appliances Requiring Power Factor Correction

Table 1. SELECTION TABLE

	NCP1618A	NCP1618B	NCP1618C	NCP1618D	NCP1618F	NCP1618H	NCP1618J	NCP1618K	NCP1618L
f_{CCM}	65 kHz	65 kHz	65 kHz	65 kHz	65 kHz	65 kHz	65 kHz	125 kHz	44 kHz
f_{clamp}	130 kHz	130 kHz	130 kHz	130 kHz	NONE	NONE	NONE	250 kHz	88 kHz
OVP2	YES	NO	NO	NO	NO	NO	NO	NO	NO
$V_{CC(on)}$	17.0 V	10.5 V	17.0 V	17.0 V	17.0 V	17.0 V	17.0 V	17.0 V	17.0 V
$V_{BO(start)}$ / $V_{BO(stop)}$	111 V / 100 V	95 V / 87 V	111 V / 100 V	111 V / 100 V	95 V / 87 V	95 V / 87 V	111 V / 100 V	111 V / 100 V	95 V / 87 V
$\left(P_{FF,\,th}\right)_{LL}$	$\frac{12\% \cdot V_{in,\,rms}^{2}}{L \cdot f_{CCM}}$	$\frac{6\% \cdot V_{in,\,rms}^{2}}{L \cdot f_{CCM}}$	$\frac{12\% \cdot V_{in,\,rms}^{2}}{L \cdot f_{CCM}}$	$\frac{12\% \cdot V_{in,\,rms}^{2}}{L \cdot f_{CCM}}$	NONE	NONE	NONE	$\frac{12\% \cdot V_{in,\,rms}^{2}}{L \cdot f_{CCM}}$	$\frac{12\% \cdot V_{in,\,rms}^{2}}{L \cdot f_{CCM}}$
Current criterion for CCM detection and confirmation at high line	YES	NO	YES	NO	NONE	NONE	NONE	NO	NO
Operation mode	Multi Mode	Multi Mode	Multi Mode	Multi Mode	CCM only	CCM only	CCM only	Multi Mode	DCM/CrM only
X2 cap discharger	NO	NO	YES	NO	NO	NO	NO	YES	NO

NOTES:

- f_{CCM} is the switching frequency when the circuit operates in continuous conduction mode (CCM)
- f_{clamp} is the maximum level to which the switching frequency is clamped when the circuit operates in FCCrM (frequency−clamped critical conduction mode). Practically, considering all modes, the circuit maintains the switching frequency above 25 kHz and below f_{clamp}.
- $V_{BO(start)}$ and $V_{BO(stop)}$ respectively are the upper and the lower thresholds of the brown−out protection (Table 1 provides their typical value)
- $V_{CC(on)}$ is the V_{CC} startup threshold, that is, the V_{CC} voltage at which the circuit starts to operate (Table 1 provides the typical value)
- OVP2: if an image of the output voltage is provided to the ZCD pin during the off−time, the circuit can detect an overvoltage of the output voltage and provide a redundant protection
- $(P_{FF,th})_{LL}$ is the expression of the power below which the circuit enters the frequency foldback operation at low line. This threshold varies as a function of the line rms voltage square and depends on the selected inductor value (L). In high line conditions, the power threshold are obtained by dividing the power expression by two (see the frequency foldback section).
- See the CCM detection section for more information regarding the current criterion for CCM detection and confirmation at high line

TYPICAL APPLICATION SCHEMATIC DIAGRAMS

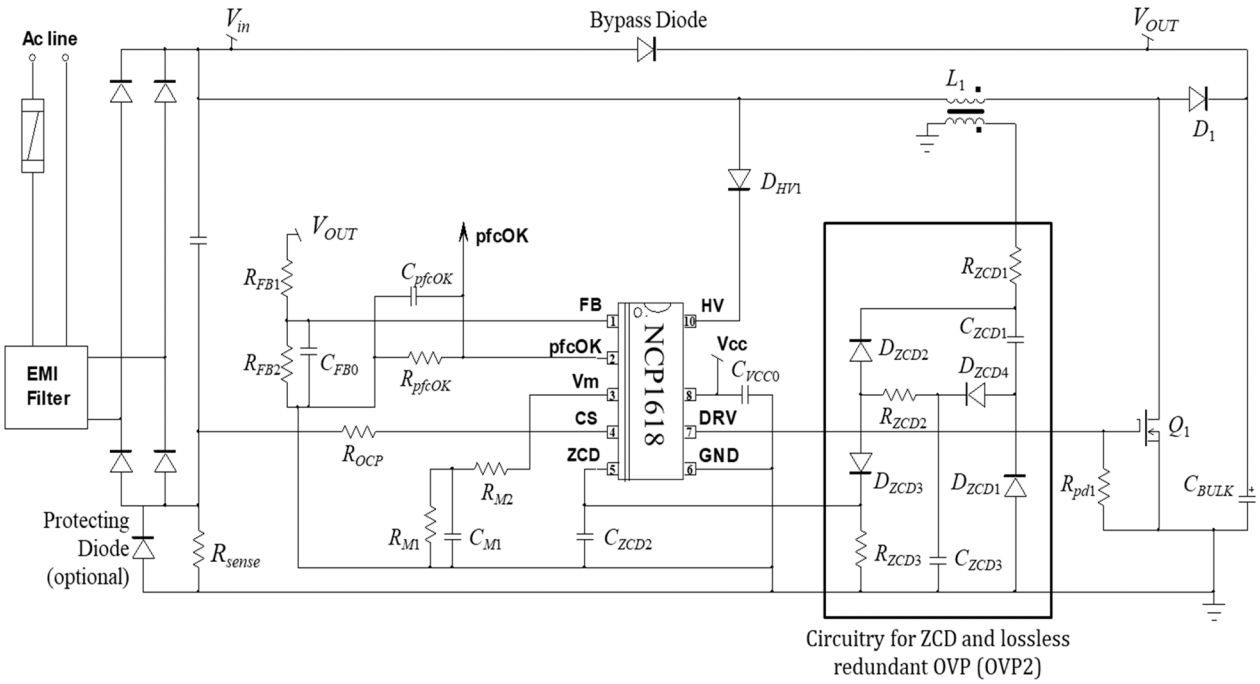


Figure 1. NCP1618 with ZCD_OVP2 Typical Application Schematic Diagram

Note that several circuitries exist for lossless redundant OVP2 as discussed in application note AND90011.

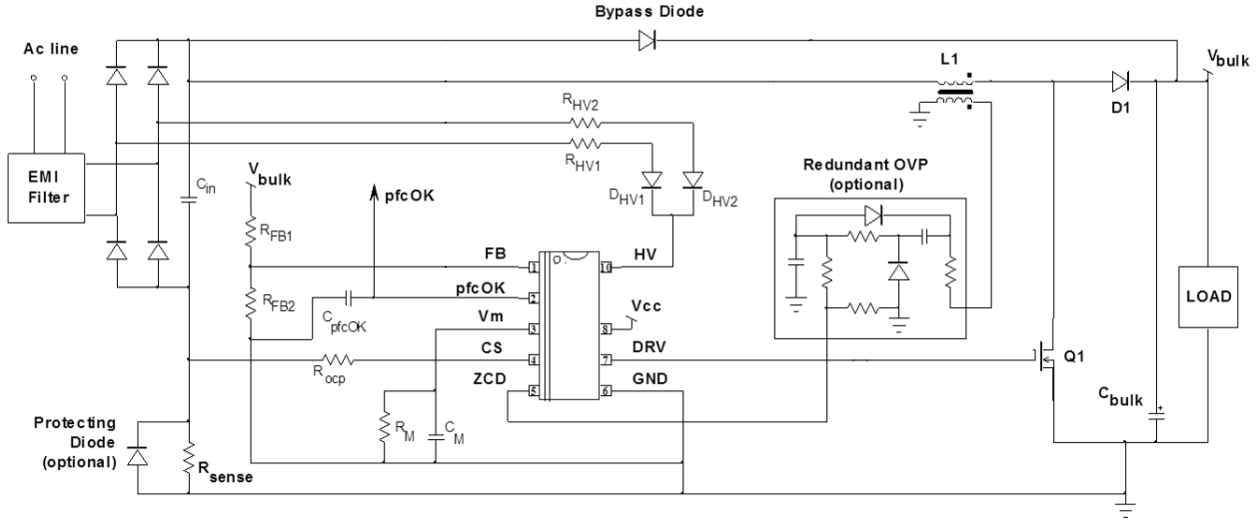


Figure 2. NCP1618 AC Start−up Typical Application Schematic Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Function	Description
1	*FB*	Feedback Pin	This pin receives a portion of the PFC output voltage for regulation and the Dynamic Response Enhancer (DRE) function which drastically speeds−up the loop response when the output voltage drops below 95.5% of the desired output level. V_{FB} is also the input signal for the soft− and fast−overvoltage (OVP) and under−voltage (UVP) comparators. A 250 nA sink current is built−in to trigger the UVP protection and disable the part if the feedback pin is accidently open.
2	*pfcOK*	PFC OK Pin	This pin is grounded until the PFC output has reached its nominal level. It is also grounded if the NCP1618 detects a major fault like a brown−out situation. A resistor is to be placed between the *pfcOK* pin and ground to form a voltage representative of the output voltage which can be used to enable the downstream converter and provide it with a feedforward signal.
3	V_M	Multiplier Output	This pin provides a voltage V_M for duty cycle modulation when the circuit operates in continuous conduction mode. The external resistor R_M applied to the V_M pin, adjusts the maximum power which can be delivered by the PFC stage. The device operates in average−current mode if an external capacitor C_M is further connected to the pin. Otherwise, it operates in peak−current mode
4	*CS*	Current Sense Pin	This pin sources a current I_{CS} which is proportional to the inductor current. The NCP1618 uses I_{CS} to adjust the PFC duty ratio in CCM operation. I_{CS} is also used for protection: inrush current detection, abnormal current detection and overcurrent protection (OCP).
5	*ZCD*	Zero Current Detection	This pin is designed to monitor a signal from an auxiliary winding and to detect the core reset when this voltage drops to zero. This function ensures valley turn on in discontinuous and critical conduction modes (DCM and CrM). The NCP1618 can further use the ZCD voltage to detect an over−voltage condition of the bulk voltage, reduce the power delivery and if the FB pin voltage is low, latch off the part in such an event.
6	*GND*	Ground Pin	Connect this pin to the PFC stage ground.
7	*DRV*	Driver Output	The high−current capability of the totem pole gate drive (−0.5/+0.8 A) makes it suitable to effectively drive high gate charge power MOSFETs.
8	V_{CC}	IC Supply Pin	This pin is the positive supply of the IC.
9	−	−	Removed for creepage distance.
10	*HV*	High Voltage Pin	The circuit senses the HV pin voltage for line range detection and line−sag and brownout protections. This pin is also the input for the high voltage start−up circuit.

INTERNAL CIRCUIT ARCHITECTURE

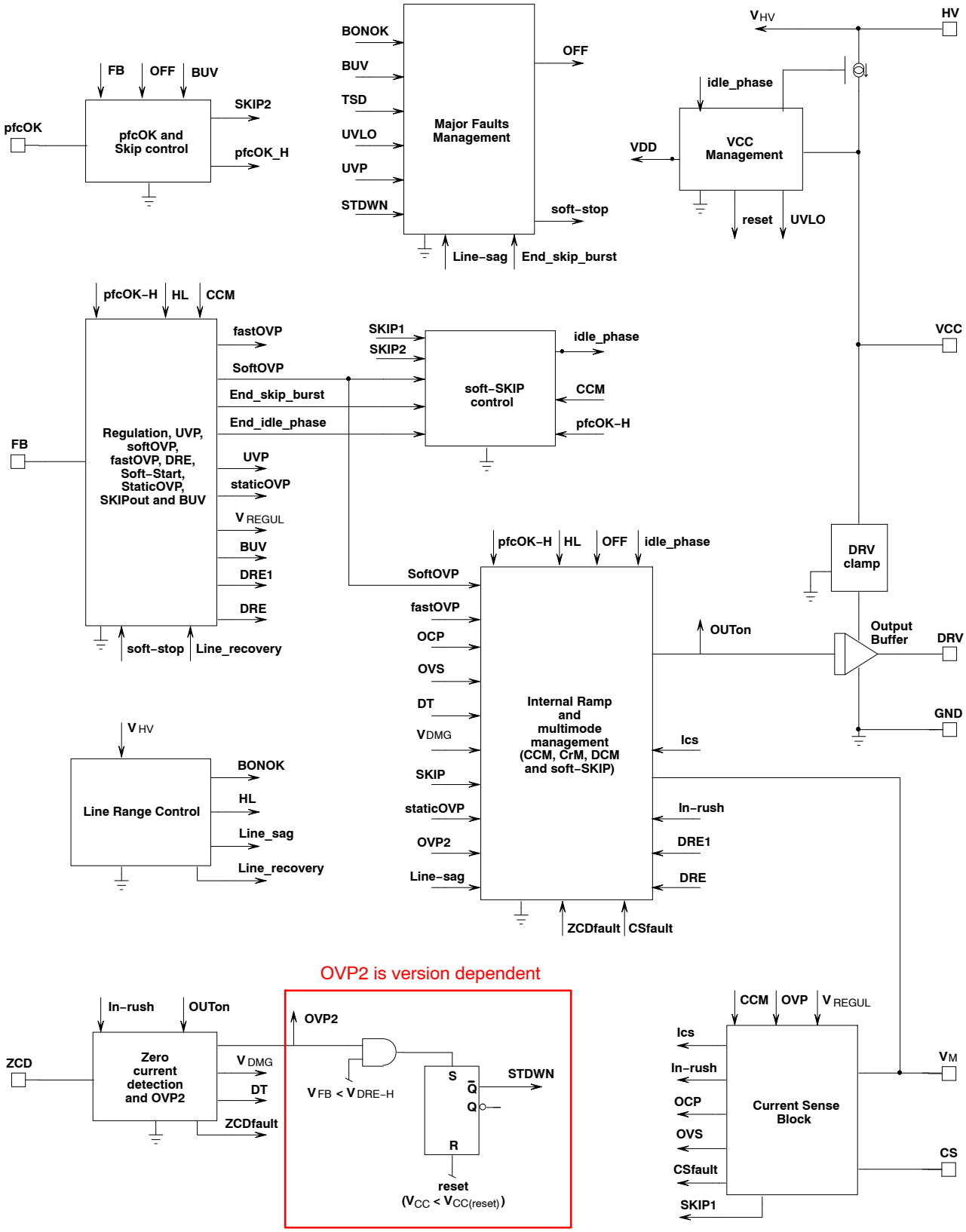


Figure 3. Internal Circuit Architecture

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
$V_{HV(MAX)}$	High Voltage Start – Up Circuit Input Voltage	– 0.3 to 700	V
$V_{CC(MAX)}$ $I_{CC(MAX)}$	Maximum Power Supply voltage, V_{CC} pin, continuous voltage Maximum current for V_{CC} pin	–0.3 to 35 Internally limited	V mA
$V_{DRV(MAX)}$ $I_{DRV(MAX)}$	Maximum driver pin voltage, DRV pin, continuous voltage Maximum current for DRV pin	–0.3, V_{DRV} (Note 1) –500, +800	V mA
V_{MAX} I_{MAX}	Maximum voltage on low voltage pins (except DRV and V_{CC} pins) Current range for low voltage pins (except DRV and V_{CC} pins)	–0.3, 5.5 (Note 2) –2, +5	V mA
$R_{\theta J-A}$	Thermal Resistance Junction–to–Air	180	°C/W
$T_{J(MAX)}$	Maximum Junction Temperature	150	°C
T_J	Operating Temperature Range	–40 to +125	°C
T_S	Storage Temperature Range	–60 to +150	°C
MSL	Moisture Sensitivity Level	1	–
	ESD Capability, HBM model (Notes 3 and 4)	3.5	kV
	ESD Capability, CDM model (Note 4)	1	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. V_{DRV} is the DRV clamp voltage $V_{DRV(high)}$ when V_{CC} is higher than $V_{DRV(high)}$. V_{DRV} is V_{CC} otherwise.
2. This level is low enough to guarantee not to exceed the internal ESD diode and 5.5 V ZENER diode. More positive and negative voltages can be applied if the pin current stays within the –2 mA / 5 mA range.
3. Except HV pin
4. This device contains ESD protection and exceeds the following tests: Human Body Model 3500 V per JEDEC Standard JESD22–A114F, Charged Device Model 1000 V per JEDEC Standard JESD22–C101F
5. This device contains latch–up protection and exceeds 100 mA per JEDEC Standard JESD78E.

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, V_{CC} = 12 V, V_{HV} = 130 V unless otherwise noted. For min/max values T_J = –40°C to +125°C, V_{CC} = 12 V, V_{HV} = 130 V unless otherwise noted)

Symbol	Description	Test Condition	Min	Typ	Max	Unit
STARTUP AND SUPPLY CIRCUITS						
$V_{CC(on)}$	Startup Threshold NCP1618A, C, D, F, H, J, K, L NCP1618B	V_{CC} rising	15.8 9.75	17.0 10.5	18.2 11.25	V
$V_{CC(off)}$	Minimum Operating Voltage	V_{CC} decreasing	8.5	9.0	9.5	
$V_{CC(HYS)}$	Hysteresis $V_{CC(on)} - V_{CC(off)}$ NCP1618A, C, D, F, H, J, K, L NCP1618B	V_{CC} decreasing	6.0 0.5	8.0 1.5	– –	
$V_{CC(reset)}$	V_{CC} level below which the circuit resets	V_{CC} decreasing	3.5	5.0	6.0	
	Start–Up Current when the V_{CC} Pin is Grounded, NCP1618A	V_{CC} = 0 V, V_{HV} = 130 V				mA
I_{start1}	Sourced by the V_{CC} Pin		0.7	1.0	1.3	
I_{HV1}	Sunk by the HV pin		–	–	1.3	
	Start–Up Current when the V_{CC} Pin is Grounded (Except NCP1618A)	V_{CC} = 0 V, V_{HV} = 130 V				mA
I_{start1}	Sourced by the V_{CC} Pin		1.0	1.6	2.2	
I_{HV1}	Sunk by the HV pin		–	–	2.2	
	Start – Up Current	$V_{CC} = V_{CC(on)} - 0.5$ V,				mA
I_{start2}	Sourced by the V_{CC} Pin	V_{HV} = 130 V	6.5	12.0	16.5	
I_{HV2}	Sunk by the HV pin		–	–	18.0	
$V_{CC(inhibit)}$	V_{CC} Threshold for I_{start1} to I_{start2} transition	V_{CC} increasing, I_{HV} > 6.5 mA	0.4	0.8	1.2	V
$HV_{(MIN)}$	Minimum Voltage for Start–Up Circuit ensuring I_{start2} = 6.5 mA	$V_{CC} = V_{CC(on)} - 0.5$ V	–	–	38	V
	Supply Current	V_{CC} = 9.6 V, F_{sw} = 65 kHz				mA
I_{CC1}	Device Disabled / Fault (no switching)		0.80	1.20	1.40	
I_{CC2}	Device Enabled (switching) / No output load on pin 5		–	2.20	4.00	
I_{CC3}	Soft–SKIP Idle Phase		–	0.25	0.50	

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, V_{CC} = 12 V, V_{HV} = 130 V unless otherwise noted. For min/max values T_J = −40°C to +125°C, V_{CC} = 12 V, V_{HV} = 130 V unless otherwise noted) (continued)

Symbol	Description	Test Condition	Min	Typ	Max	Unit
GATE DRIVE						
t_R	Output voltage rise−time	C_L = 1 nF 10 − 90% of output signal	−	45	−	ns
t_F	Output voltage fall−time	C_L = 1 nF 10 − 90% of output signal	−	30	−	ns
R_{OH}	Source resistance		−	11	−	Ω
R_{OL}	Sink resistance		−	7	−	Ω
I_{SOURCE}	Peak source current (Note 6)	V_{DRV} = 0 V	−	500	−	mA
I_{SINK}	Peak sink current (Note 6)	V_{DRV} = 12 V	−	800	−	mA
V_{DRVlow}	DRV pin level at V_{CC} close to $V_{CC(off)}$	V_{CC} = $V_{CC(off)}$ + 200 mV 10 kΩ resistor to GND	8	−	−	V
$V_{DRVhigh}$	DRV pin level at V_{CC} = 35 V	R_L = 33 kΩ, C_L = 220 pF	10	12	14	V
RAMP						
f_{CCM}	CCM switching frequency NCP1618K NCP1618L		60 115.4 40.3	65 125 44	70 134.6 47.7	kHz
R_{CCM}	Ratio f_{CCM} over Switching Frequency for CCM detection		−	112	−	%
t_{CCMend}	Blanking Time for CCM mode end detection		315	360	415	ms
f_{clamp}	Clamp Frequency (DCM Frequency) NCP1618K NCP1618L	No frequency foldback	− − −	130 250 88	− − −	kHz
f_{clamp_ratio}	f_{clamp} over f_{CCM} ratio	No frequency foldback	1.90	2.00	2.05	−
$(t_{on,FF})_{LL}$ $(t_{on,FF})_{HL}$	On−Time below which Frequency Foldback is Engaged NCP1618A, C, D NCP1618B NCP1618K NCP1618L	 Low line High line Low line High line Low line High line Low line High line	 − − − − − − − −	 3.75 1.87 1.87 0.94 2 1 5.68 2.84	 − − − − − − − −	µs
f_{min}	Minimum DCM Frequency		25.0	30.5	36.0	kHz
$t_{on,max}$	Maximum On−Time (CCM) NCP1618K NCP1618L	f_{CCM} = 65 kHz f_{CCM} = 125 kHz f_{CCM} = 44 kHz	− − −	15 7.8 22.7	− − −	µs
R_{jit}	Ramp Frequency Jittering		−	10	−	%
f_{jit}	Jittering Frequency		−	119	−	Hz
REGULATION BLOCK						
V_{REF}	Feedback Voltage Reference	T_J = 25°C T_J = −40°C to +125°C	2.46 2.44	2.50 2.50	2.54 2.56	V
$V_{DRE}L$ / V_{REF}	Ratio (V_{OUT} Low Detect Lower Threshold / V_{REF})		95.0	95.5	96.0	%
$V_{DRE}H$ / V_{REF}	Ratio (V_{OUT} Low Detect Higher Threshold / V_{REF})		97.5	98.0	98.5	%
H_{DRE} / V_{REF}	Ratio (V_{OUT} Low Detect Hysteresis / V_{REF})		2	−	−	%
K_{DRE1} K_{DRE0}	Loop Gain Increase due to Dynamic Response Enhancer	pfcOK high pfcOK low	− −	10 5	− −	−
$t_{SSTOP,max}$	Soft−Stop Duration for Gradual Discharge of the Control Voltage from Max to Min		−	140	−	ms

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, V_{CC} = 12 V, V_{HV} = 130 V unless otherwise noted. For min/max values T_J = −40°C to +125°C, V_{CC} = 12 V, V_{HV} = 130 V unless otherwise noted) (continued)

Symbol	Description	Test Condition	Min	Typ	Max	Unit
StaticOVP						
D_{MIN}	Duty Ratio	V_{FB} = 3 V	–	–	0	%
SOFT SKIP CYCLE MODE BLOCK						
I_{VM}	CrM/DCM V_M pin Current Capability		400	–	–	μA
$V_{SKIP(th)}$	V_M Pin SKIP Threshold		1.2	1.5	1.8	V
V_{SKIP2}	pfcOK SKIP Threshold		0.4	0.5	0.6	V
t_{SKIP2}	pfcOK Minimum Negative Pulse Duration for SKIP Detection		24	29	33	μs
V_{REFX}/V_{REF}	V_{FB} Upper Value (V_{REFX}) During a Soft−SKIP Burst Cycle (defined as a V_{REF} percentage)		102.5	103.0	103.5	%
$(R_{FB})_{recover}$	V_{FB} Lower Value During a Soft Skip Cycle Burst (defined as a percentage of V_{REF}) for NCP1618C, D, H, J		96.5 98.5	98.0 100	99.5 101.5	%
CURRENT SENSE BLOCK						
$V_{CSoff100}$	Current Sense Voltage Offset	I_{CS} = −100 μA	−10	–	15	mV
$V_{CSoff10}$	Current Sense Voltage Offset	I_{CS} = −10 μA	−10	–	10	mV
I_{CCM-H}	Minimum I_{CS} current for CCM detection		44	50	56	μA
I_{CCM-L}	Minimum I_{CS} current for CCM confirmation		26	30	35	μA
$I_{ILIMIT1(LL)}$	Low−Line Over−Current Protection Threshold	V_{HV} = 130 V	185	200	215	μA
$I_{ILIMIT1(HL)}$	High−Line Over−Current Protection Threshold	V_{HV} = 290 V	185	200	215	μA
$t_{OCP1(LL)}$	Low−Line Over−current Protection Delay from (I_{CS} > $I_{ILIMIT1(LL)}$) to DRV low	V_{HV} = 130 V	–	40	100	ns
$t_{OCP1(HL)}$	High−Line Over−current Protection Delay from (I_{CS} > $I_{ILIMIT1(HL)}$) to DRV low	V_{HV} = 290 V	–	40	100	ns
$I_{ILIMIT2(LL)}$	Low−Line Threshold for Abnormal Current Protection	V_{HV} = 130 V	270	300	330	μA
$I_{ILIMIT2(HL)}$	High−Line Threshold for Abnormal Current Protection	V_{HV} = 290 V	270	300	330	μA
$t_{LEB,CS}$	Leading Edge Blanking Time for the Over−Current and Abnormal Current Detection Comparators (Note 6)		150	260	350	ns
$I_{in-rush}$	Threshold for In−rush Current Detection		7.5	10.0	12.5	μA
$V_{CS(fault)}$	CS Fault Threshold		180	250	320	mV
$t_{CS(fault)}$	CS Fault Blanking Time		1	2	3	μs
$I_{CS(test)}$	Source Current for CS pin testing		–	235	–	μA
$R_{OCP,min}$	Minimum Impedance to apply to the CS pin not to Trig the CS Short−to−Ground Protection (Note 6)		–	–	1.5	kΩ
ZERO VOLTAGE DETECTION CIRCUIT						
$t_{LEB,ZCD}$	ZCD Leading Edge Blanking Time		70	100	130	ns
$V_{ZCD(th)H}$	Zero Current Detection, V_{ZCD} rising		0.90	1.00	1.10	V
$V_{ZCD(th)L}$	Zero Current Detection, V_{ZCD} falling		0.40	0.50	0.60	V
$V_{ZCD(hyst)}$	Hysteresis of the Zero Current Detection Comparator		0.35	0.50	–	V
$I_{ZCD(bias)H}$	ZCD Pin Bias Current, V_{ZCD} = $V_{ZCD(th)H}$		0.5	–	2.0	μA
$I_{ZCD(bias)L}$	ZCD Pin Bias Current, V_{ZCD} = $V_{ZCD(th)L}$		0.5	–	2.0	μA
t_{ZCD}	(V_{ZCD} < $V_{ZCD(th)L}$) to (DRV high)		–	50	85	ns
t_{SYNC}	Minimum ZCD Pulse Width		–	50	–	ns
$t_{WDG(OS)}$	Watch Dog Timer in “Overstress” Situation		710	815	950	μs

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, V_{CC} = 12 V, V_{HV} = 130 V unless otherwise noted. For min/max values T_J = −40°C to +125°C, V_{CC} = 12 V, V_{HV} = 130 V unless otherwise noted) (continued)

Symbol	Description	Test Condition	Min	Typ	Max	Unit
ZERO VOLTAGE DETECTION CIRCUIT						
$I_{ZCD(test)}$	Source Current for ZCD pin testing		–	230	–	μA
$R_{ZCD,min}$	Minimum Impedance to apply to the ZCD pin not to Trig the ZCD Short−to−Ground Protection (Note 6)		–	–	7.5	kΩ
UNDER− AND OVER−VOLTAGE PROTECTION						
V_{UVP}	UVP Threshold	V_{FB} falling	–	0.3	–	V
R_{UVP}	Ratio (UVP Threshold) over V_{REF} (V_{UVP} / V_{REF})	V_{FB} falling	8	12	16	%
$R_{UVP(HYST)}$	Ratio (UVP Hysteresis) over V_{REF}	V_{FB} rising	2	3	4	%
$V_{softOVP}$	Soft OVP Threshold	V_{FB} rising	–	2.625	–	V
$R_{softOVP}$	Ratio (Soft OVP Threshold) over V_{REF} ($V_{softOVP}$ / V_{REF})	V_{FB} rising	104	105	106	%
$R_{softOVP(H)}$	Ratio (Soft OVP Hysteresis) over V_{REF}	V_{FB} falling	1.5	2.0	2.5	%
$V_{fastOVP}$	Fast OVP Threshold	V_{FB} rising	–	2.7	–	V
$R_{fastOVP1}$	Ratio (Fast OVP Threshold) over (Soft OVP Upper Threshold) ($V_{fastOVP}$ / $V_{softOVP}$)	V_{FB} rising	102	103	104	%
$R_{fastOVP2}$	Ratio (Fast OVP Threshold) over V_{REF} ($V_{fastOVP}$ / V_{REF})	V_{FB} rising	107.0	108.3	109.5	%
$V_{OVPrecover}$	FB Threshold for Recovery from a Soft or Fast OVP	V_{FB} falling	–	2.575	–	V
$(I_B)_{FB1}$	FB bias Current @ V_{FB} = $V_{softOVP}$		50	210	450	nA
$(I_B)_{FB2}$	FB bias Current @ V_{FB} = V_{UVP}		50	210	450	nA
V_{OVP2}	ZCD OVP2 Threshold (NCP1618A only)	V_{ZCD} rising	3.9	4.0	4.1	V
t_{OVP2}	OVP2 Blanking Time (NCP1618A only)		70	100	130	ns
V_M PIN						
$V_{M,FCCrM}$	V_M Pin Voltage in FCCrM (CrM or DCM)		2.0	2.5	3.0	V
$(V_{ramp})_{pk}$	PWM Comparator Reference Voltage for CCM Operation	V_M rising	3.50	3.75	4.00	V
$I_{M1(LL)}$	V_M Pin Source Current	V_{FB} = 2 V, I_{CS} = −100 μA low line	31	39	46	μA
$I_{M1(LL)}$ / $(V_{ramp})_{pk}$	$I_{M1(LL)}$ over $(V_{ramp})_{pk}$ ratio	V_{FB} = 2 V, I_{CS} = −100 μA low line	8.4	10.4	12.4	μS
$I_{M2(LL)}$	V_M Pin Source Current	V_{FB} = 2 V, I_{CS} = −200 μA low line	66	82	96	μA
$I_{M2(LL)}$ / $(V_{ramp})_{pk}$	$I_{M2(LL)}$ over $(V_{ramp})_{pk}$ ratio	V_{FB} = 2 V, I_{CS} = −200 μA low line	17	22	26	μS
$I_{M1(HL)}$	V_M Pin Source Current	V_{FB} = 2 V, I_{CS} = −100 μA high line	131	163	194	μA
$I_{M1(HL)}$ / $(V_{ramp})_{pk}$	$I_{M1(HL)}$ over $(V_{ramp})_{pk}$ ratio	V_{FB} = 2 V, I_{CS} = −100 μA high line	35	43	52	μS
BROWN−OUT, LINE SAG AND LINE RANGE DETECTION						
$V_{BO(start)}$	Upper Threshold for Line Sag and Brown−Out Detection NCP1618A, C, D, J, K NCP1618B, F, H, L	V_{HV} increasing	 103 88	 111 95	 119 102	V
$V_{BO(stop)}$	Lower Threshold for Line Sag and Brown−Out Detection NCP1618A, C, D, J, K NCP1618B, F, H, L	V_{HV} decreasing	 92 80	 100 87	 108 94	V
$V_{BO(HYS)}$	Hysteresis NCP1618A, C, D, J, K NCP1618B, F, H, L	V_{HV} increasing	7 3.5	11 7.5	– –	V

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, V_{CC} = 12 V, V_{HV} = 130 V unless otherwise noted. For min/max values T_J = −40°C to +125°C, V_{CC} = 12 V, V_{HV} = 130 V unless otherwise noted) (continued)

Symbol	Description	Test Condition	Min	Typ	Max	Unit
BROWN−OUT, LINE SAG AND LINE RANGE DETECTION						
$t_{BO(blank)}$	Brown−out Detection Blanking Time	V_{HV} decreasing	550	650	750	ms
$t_{Sag(blank)}$	Line Sag Detection Blanking Time	V_{HV} decreasing	22.8	26.0	30.2	ms
V_{HL}	High−Line Level Detection Threshold	V_{HV} increasing	220	236	252	V
V_{LL}	Low−Line Level Detection Threshold	V_{HV} decreasing	207	222	237	V
$V_{LR(HYST)}$	Line Range Select Hysteresis	V_{HV} increasing	9	–	–	V
$t_{blank(LL)}$	High− to Low−Line Mode Selector Timer	V_{HV} decreasing	22.8	26.0	30.2	ms
$t_{filter(HV)}$	Low− to High−Line Mode Selector Timer Filter		300	360	420	μs
$t_{line(lockout)}$	Lockout Timer for Low− to High−Line Mode Transition	V_{HV} increasing	450	515	600	ms
X2 DISCHARGE						
$t_{line(removal)}$	Line Voltage Removal Detection Timer		83	100	100	ms
$t_{HV(up)}$	Upslope Detection Reset Timer (Note 6)	HV increasing	–	1	27	V/ms
$t_{HV(down)}$	Downslope Detection Reset Timer (Note 6)	HV decreasing	–	14.0	1.89	V/ms
$I_{HV(discharge)}$	HV Discharge Current		2.5	4.5	6.5	mA
$V_{HV(discharge)}$	HV Discharge Stop Level		–	–	34	V
pfcOK AND BUV PROTECTION						
$V_{pfcOK−L}$	pfcOK Voltage in OFF Mode	1 mA being sunk by the pfcOK pin	–	–	100	mV
I_{pfcOK}	pfcOK Current	V_{FB} = 2.5 V, V_{pfcOK} = 1 V	23	25	27	μA
V_{BUV}	Bulk Under−Voltage Protection (BUV) Threshold NCP1618H NCP1618K	V_{FB} falling	1.71 1.52 0.95	1.80 1.6 1	1.89 1.68 1.05	V
t_{BUV}	BUV Delay Before Operation Recovery		450	515	600	ms
THERMAL SHUTDOWN						
T_{LIMIT}	Thermal Shutdown Threshold		–	150	–	°C
H_{TEMP}	Thermal Shutdown Hysteresis		–	50	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Guaranteed by Design

STARTUP SEQUENCE / V_{CC} MANAGEMENT

An internal high−voltage startup current source is enabled whenever V_{CC} drops below $V_{CC(off)}$ (9 V, typically), to charge the V_{CC} capacitor, in particular when the PFC stage is plugged to the mains outlet. When V_{CC} exceeds the $V_{CC(on)}$ level, the current source turns off and the circuit starts operating. The energy stored by the V_{CC} capacitor must be large enough to feed the controller and maintain V_{CC} above $V_{CC(off)}$ (that is, the level below which the circuit turns off) until an auxiliary power supply takes over. The large 8−V UVLO typical hysteresis ($V_{CC(on)}$ minus $V_{CC(off)}$) is provided to prevent erratic operation. The low $V_{CC(on)}$ level makes it ideal in applications where the controller is fed by an external power source (typically from an auxiliary power supply). Its maximum start−up level (11.25 V) is set low enough to be powered from traditional 12−V rails.

The startup current source being off when the PFC stage is in operation, the HV pin virtually draws no current. This helps minimize the losses in light−load conditions and hence, meet the most stringent standby requirements.

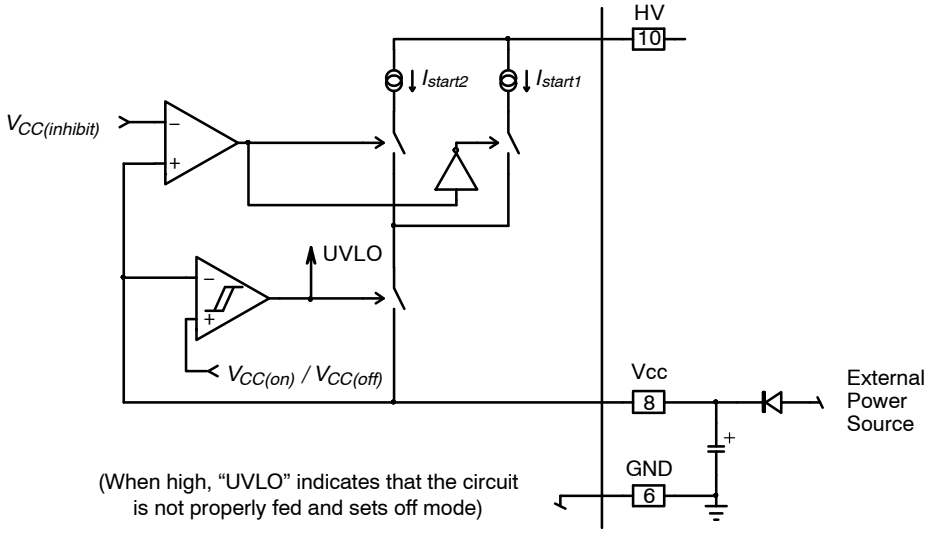


Figure 4. Internal Startup Current Source

The startup current sourced by the V_{CC} pin (I_{start2}) is 12 mA typically. As shown by Figure 4, the startup current is limited to I_{start1} (1 mA typically) when the V_{CC} voltage is below $V_{CC(inhibit)}$ (0.8 V typically). This feature prevents the circuit from overheating if the V_{CC} pin is accidentally grounded.

Thus, the following equation provides the V_{CC} capacitor charge time:

$$t_{ch} = \frac{C_{Vcc} \cdot V_{CC(inhibit)}}{I_{start1}} + \frac{C_{Vcc} \cdot (V_{CC(on)} - V_{CC(inhibit)})}{I_{start2}} \quad \text{(eq. 1)}$$

As an example, using 17 V for $V_{CC(on)}$ (NCP1618A typical V_{CC} startup threshold) and their typical values for the other parameters in play ($V_{CC(inhibit)}$, I_{start1} and I_{start2}), it comes for a 100−µF V_{CC} capacitance:

$$(t_{ch-100\mu F})_{typical} = \frac{100 \cdot 10^{-6} \cdot 0.8}{1 \cdot 10^{-3}} + \frac{100 \cdot 10^{-6} \cdot (17 - 0.8)}{12 \cdot 10^{-3}} \cong 215 \text{ ms} \quad \text{(eq. 2)}$$

THREE MODES OF OPERATION

Depending on the current cycle duration, the NCP1618 operates in either FCCrM or CCM. In FCCrM (or frequency clamped critical conduction mode), the circuit operates in critical conduction mode until the switching frequency exceeds the f_{clamp} clamp threshold (130 kHz typically). At that moment, as detailed in the next paragraph, the circuit operates in discontinuous conduction mode with valley turn−on.

Note that the circuit can transition from CrM to DCM and vice versa within half−line cycles. Typically DCM is obtained near the line zero crossing where current cycles tend to be shorter and CrM, at the top of the line sinusoid where the current cycles are longer. This is because the circuit enters DCM operation when the current cycle is shorter than T_{clamp} (clamp period corresponding to f_{clamp}: $T_{clamp} = 1 / f_{clamp}$) as it can easily be the case near the line zero crossing and in light−load conditions. Conversely, if the current cycle exceeds T_{clamp}, the system naturally enters the CrM operation mode. These transitions cause no discontinuity in the operation and power factor remains properly controlled.

CCM operation is obtained in heavy load conditions when the current cycle is longer than 112% of the CCM switching period. At that moment, the circuit operates as a CCM controller in all parts of the line sinusoid (no transitions to FCCrM) and remains in CCM for at least the CCM blanking time (T_{CCMend} of 360 ms typically). This is because the circuit recovers the FCCrM mode only if it cannot detect 8 consecutive current cycles longer than the CCM switching period for T_{CCMend}.

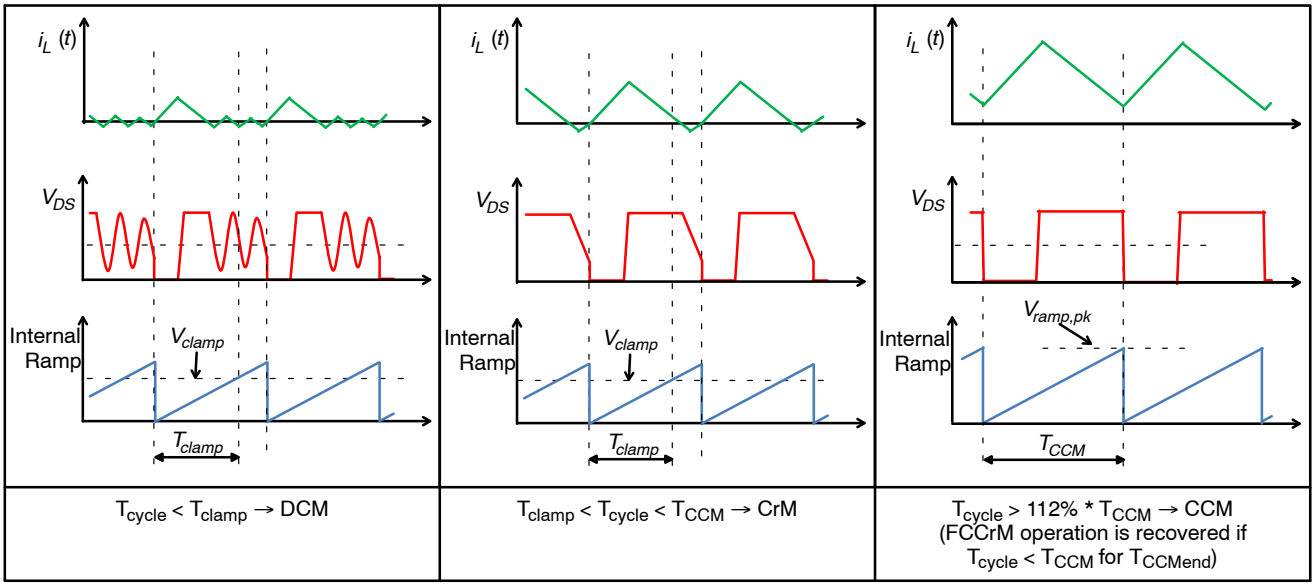


Figure 5. Three Operation Modes (MOSFET Drain−source Voltage is in Red, the Internal Ramp is in Green)

Finally, depending on the conditions, the circuit operates in CrM, DCM (with valley turn−on) or CCM.

Practically, the circuit compares the current cycle duration to two periods T_{clamp} and T_{CCM}:

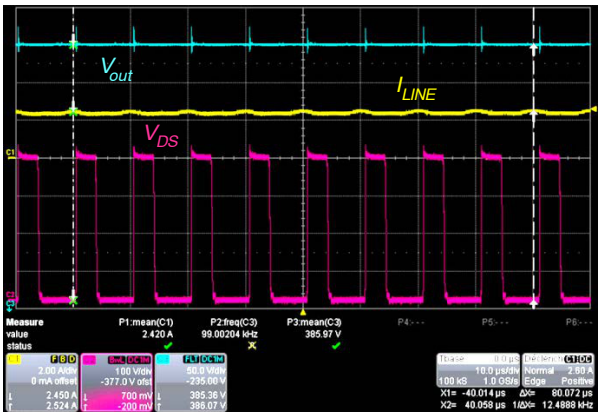
- If the current cycle duration is shorter than T_{clamp}, T_{clamp} forces the switching frequency and the system operates in DCM
- If the current cycle duration is longer than T_{clamp} but shorter than 112% of T_{CCM}, the system operates in CrM.
- If 8 consecutive current cycles happen to be longer than 112% of T_{CCM}, the system enters CCM mode with a switching frequency set to f_{CCM} = 1 / T_{CCM}. The system remains in this mode until the circuit cannot detect 8 consecutive current cycles longer than T_{CCM} for T_{CCMend} (360 ms typically).

  Figure 5 provides a simplified description of the manner the conduction mode is selected.

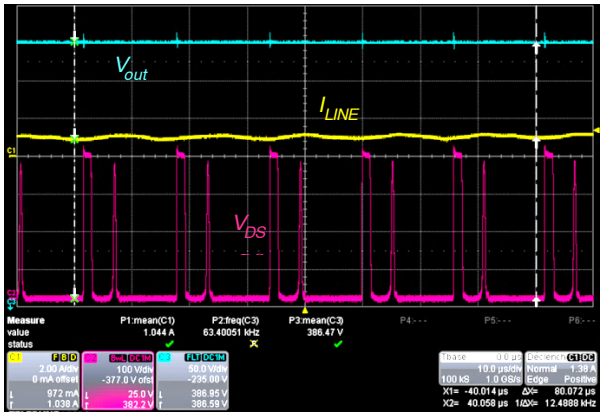
FREQUENCY−CLAMPED CRITICAL CONDUCTION MODE

As aforementioned, the NCP1618 tends to operate in critical conduction mode as long as the current switching cycle is short enough not to enter the CCM mode. However, if the current cycle happens to be shorter than the frequency−clamp period (T_{clamp} which is about 7.7 μs typically leading to a 130 kHz DCM frequency), the circuit delays the next cycle until the T_{clamp} time has elapsed. Thus, the circuit enters DCM operation. In DCM, the switching period is actually a bit longer than T_{clamp}. This is because of the below discussed modulation method but mainly because the next cycle is further delayed until the next valley is detected (left plot of Figure 5). Doing so, valley turn−on is obtained for minimized losses.

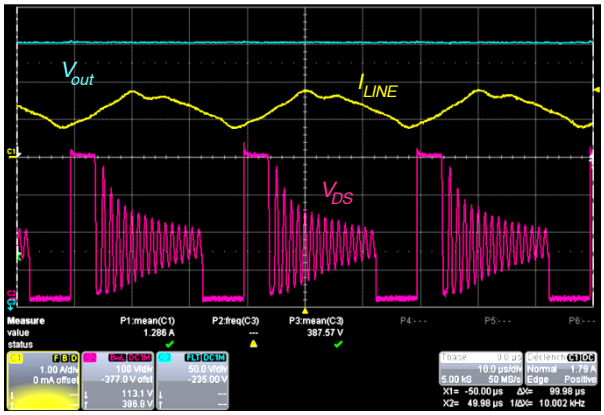
Frequency−Clamped operation is controlled by a proprietary circuitry which modulates the duty−ratio cycle−by−cycle to prevent any discontinuity in operation and ensure proper current shaping. Also, as shown by Figure 6, it automatically varies the valley at which the MOSFET turns on within the line sinusoid as necessary to maintain valley switching and clamp the frequency over the instantaneous input voltage range. For instance, DCM is more likely to occur near the line zero crossing and CrM at the top of the sinusoid. As the load further decays, current cycles become shorter and DCM operation is obtained over the entire line sinusoid. Furthermore, as detailed in the next section and illustrated by Figure 6c and Figure 6d, the DCM period clamp is increased below a certain load level for frequency foldback (a longer minimum switching period is forced causing frequency foldback). Anyway, in all cases, the NCP1618 scheme ensures a clean control preventing that repeated spurious changes in the turn−on valley possibly cause current distortion and audible noise.



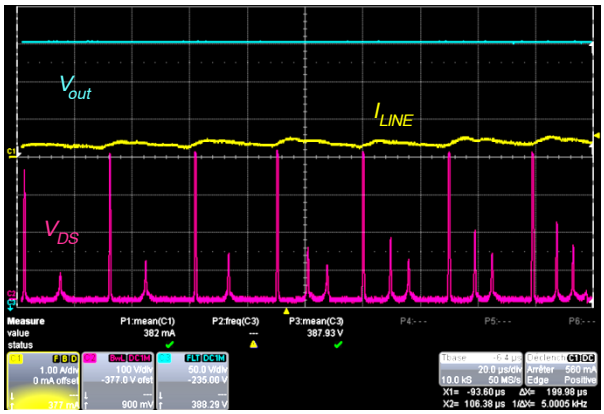
a) 40% load, top of the sinusoid



b) 40% load, near the line zero crossing



c) 20% load, top of the sinusoid



d) 20% load,near the line zero crossing

Figure 6. Operation of the 500 W NCP1618 Evaluation Board @ 115 Vrms

FREQUENCY FOLDBACK IN DCM OPERATION

The frequency clamp (or DCM period) is gradually decreased when the power demand drops below a certain threshold. The expression of this power threshold depends on the line range (see the “Line Range Detection” section). The threshold also depends on the circuit version. Table 1 provides the equation for Low line, where $V_{in,rms}$ is the line rms voltage, L is the boost inductor of the PFC stage and f_{CCM} is the switching frequency in CCM operation (65 kHz typically). The High Line power threshold is half Low Line power threshold.

The frequency clamp level linearly reduces as the power further decays to nearly reach (f_{clamp} / 10) when the power is close to zero. The circuit however forces a minimum 25−kHz operation to prevent audible noise. See next section.

DCM MINIMUM FREQUENCY (FOR DCM ONLY)

As aforementioned, the DCM frequency is gradually lowered in very light load conditions as a function of the load, to optimize the efficiency. This frequency foldback function can reduce the frequency to nearly 10 kHz. However, a specific ramp ensures that the switching frequency remains above audible frequencies.

This ramp generates a clock which overrides the clock provided by the DCM ramp (it forces next DRV pulse even if the DCM ramp clock is not generated yet). However, the minimum−frequency ramp remains synchronized to the drain source voltage for valley turn−on. Practically, as shown by Figure 7, the minimum−frequency ramp typically sets the clock signal when the switching period reaches 33 μs. The DRV output will then turn on back when the next valley is detected. If no valley can be detected within a 3 μs interval, DRV is forced high whatever the drain−source voltage is. As a result, the minimum frequency is typically between 30 kHz (33 μs switching period) if a valley is immediately detected and 28 kHz (36 μs switching period) if no valley can be detected.

Note that the frequency clamp can force a new DRV pulse only if the system is in dead−time. The minimum frequency clamp cannot cause CCM operation.

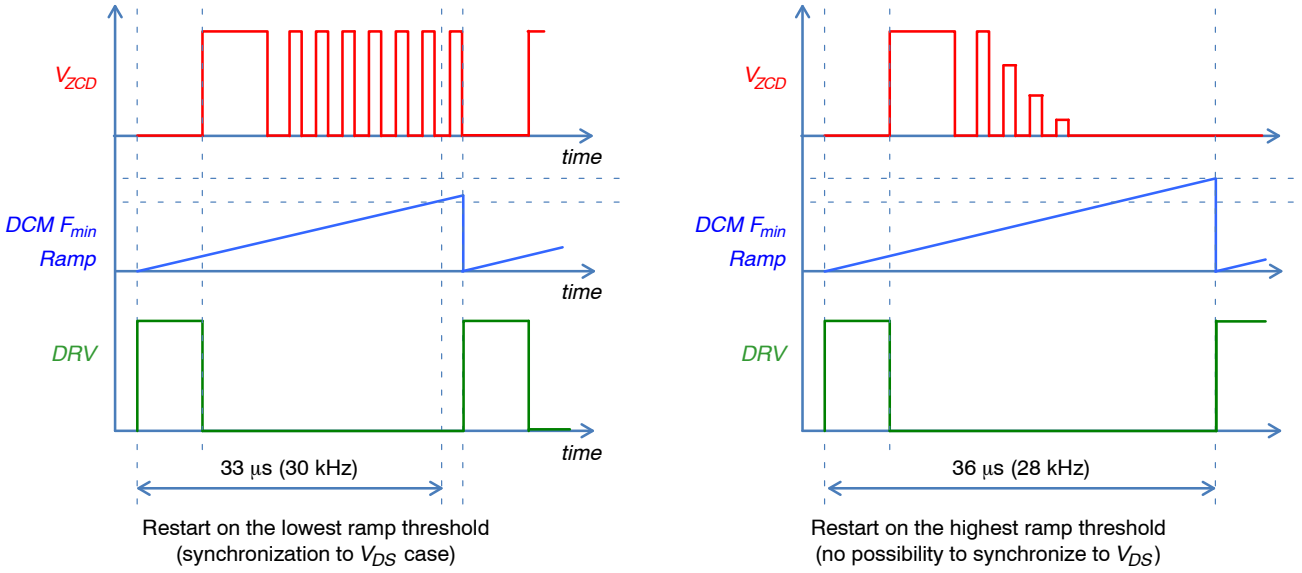


Figure 7. DCM Minimum Switching Frequency Ramp

JITTERING

In CCM operation, the NCP1618 features the jittering function which is an effective method to improve the EMI signature. An internal low−frequency signal modulates the oscillator swing which helps by spreading out energy in conducted noise analysis.

Practically, the CCM switching frequency is typically varied as follows:

- Jittering frequency: 119 Hz
- Pk to pk frequency variation: 10%

Jittering is not implemented in frequency clamped critical conduction mode (FCCrM including CrM and/or DCM sequences) where valley turn−on operation naturally leads to frequency variations.

CCM DETECTION

As aforementioned, the NCP1618 measures the duration of each current cycle (the current cycle is the total duration of the on−time + the demagnetization time) and compares it to T_{CCM}, which is the CCM switching period. The circuit enters CCM mode if it consecutively detects 8 current cycles longer than 112% of T_{CCM}. Conversely, the circuit leaves the CCM mode if the circuit does not detect 8 consecutive cycles exceeding T_{CCM} for the CCM blanking time (T_{CCMend} of 360 ms typically). Some versions (see Table 1) do not wait for conditions to enter CCM mode and CCM mode is forced, i.e. DCM/CRM modes are omitted when CCM mode is forced.

The following expressions provide the typical power thresholds for:

- CCM entering:

$$(P_{in,avg})_{CCM_{in}} = \frac{0.56 \cdot V_{in,rms}{}^2 \cdot (V_{out} - \sqrt{2} \cdot V_{in,rms})}{L \cdot f_{CCM} \cdot V_{out}} \quad \text{(eq. 3)}$$

- FCCrM recovery:

$$(P_{in,avg})_{CCM_{out}} = \frac{0.50 \cdot V_{in,rms}{}^2 \cdot (V_{out} - \sqrt{2} \cdot V_{in,rms})}{L \cdot f_{CCM} \cdot V_{out}} \quad \text{(eq. 4)}$$

Where L is the value of the PFC inductor, $V_{in,rms}$ is the line rms voltage, V_{out} is the output voltage and f_{CCM} is the CCM switching frequency (65 kHz typically).

NOTES:

- The 8 current cycles longer than 112% of T_{CCM} necessary to detect CCM are not validated unless the inductor current happens to exceed a minimum level within each cycle. Practically, the second criterion consists of comparing the internal current sense current (I_{CS}) to the following internal current references:
  - I_{CCM-H} (50 μA typically) when CCM is low.
  - I_{CCM-L} (30 μA typically) when CCM is high.
- Some options (see Table 1) meet the second criterion in low line only. In high line, it validates CCM cycles regardless of the I_{CS} current level.

CURRENT SENSE BLOCK

The NCP1618 is designed to monitor a negative voltage proportional to inductor current (I_L). As portrayed by Figure 8, a current sense resistor (R_{sense}) is inserted in the return path to generate a negative voltage (V_{Rsense}) proportional to I_L. The circuit uses V_{Rsense} to detect when I_L exceeds its maximum permissible level. To do so, the circuit incorporates an operational amplifier that sources the current necessary to maintain the CS pin at 0 V (refer to Figure 9). By inserting a resistor R_{OCP} between the *CS* pin and R_{sense}, we adjust the current that is sourced by the CS pin (I_{CS}) as follows:

$$-(R_{sense} \cdot I_L) + (R_{OCP} \cdot I_{CS}) = 0 \quad \text{(eq. 5)}$$

Which leads to:

$$I_{CS} = \frac{R_{sense}}{R_{OCP}} I_L \qquad \text{(eq. 6)}$$

In other words, the CS pin current (I_{CS}) is proportional to the inductor current. Three protection functions use I_{CS}: the over−current protection, the in−rush current detection and the overstress detection. It is also used in CCM to control the power−switch duty−ratio.

IMPORTANT NOTES:

- Resistor R_{OCP} has to be located as close as possible to CS pin. Please see recommended layout at the end of this document
- As detailed below, two external resistors adjust the current thresholds (R_{sense} and R_{OCP}), thus offering some flexibility on the R_{sense} selection which can be chosen for an optimal trade−off between noise immunity and losses.
- *However the R_{OCP} resistance must be selected higher or equal to 1.5 kΩ. If not, the protection against accidental short−to−ground failures of the CS pin may trip and thus, prevent operation of the circuit.*

Over−Current Protection (OCP)

If I_{CS} exceeds the OCP threshold ($I_{ILIMIT1}$ which is 200 μA typically) an over−current situation is detected and the MOSFET is immediately turned off (cycle−by−cycle current limitation). The maximum inductor current can hence be limited as follows:

$$I_{L(max)} = \frac{R_{OCP}}{R_{sense}} I_{LIMIT1} \qquad \text{(eq. 7)}$$

As an example, if R_{sense} = 30 mΩ and R_{OCP} = 2 kΩ, the maximum inductor current is typically set to:

$$I_{(L(max)} = \frac{2 \cdot 10^3}{30 \cdot 10^{-3}} \cdot 200 \cdot 10^{-6} \cong 13.3\ A \qquad \text{(eq. 8)}$$

In−rush Current Detection

The NCP1618 permanently monitors the input current and when in FCCrM, can delay the MOSFET turn on until (I_L) has vanished. This is one function of the I_{CS} comparison to the $I_{in-rush}$ threshold (10 μA typical). This feature helps maintain proper FCCrM operation when the ZCD signal is too distorted for accurate demagnetization detection like it can happen at very high line. The inrush comparator also serves to detect that the inductor current remains at a low value, as necessary for some functions like the CS pin short−to−ground accidental protection. Re−using above example (R_{sense} = 30 mΩ, R_{OCP} = 2 kΩ), the inrush level of the input current is typically set to:

$$I_{(L(inrush)} = \frac{2 \cdot 10^3}{30 \cdot 10^{-3}} \cdot 10 \cdot 10^{-6} \cong 0.67\ A \qquad \text{(eq. 9)}$$

Abnormal Current Detection (Overstress)

When the PFC stage is plugged to the mains, the bulk capacitor is abruptly charged to the line voltage. The charge current (named in−rush current) can be very huge even if an in−rush limiting circuitry is implemented. Also, if the inductor saturates, the input current can go far above the current limitation due to the reaction time of the overcurrent protection. If one of these cases leads the internal CS pin current (I_{CS}) to exceed $I_{ILIMIT2}$ (set to 150% of $I_{ILIMIT1}$), an abnormal current situation is detected, causing the DRV output to be kept low for 800 μs after the circuit has dropped below the in−rush level.

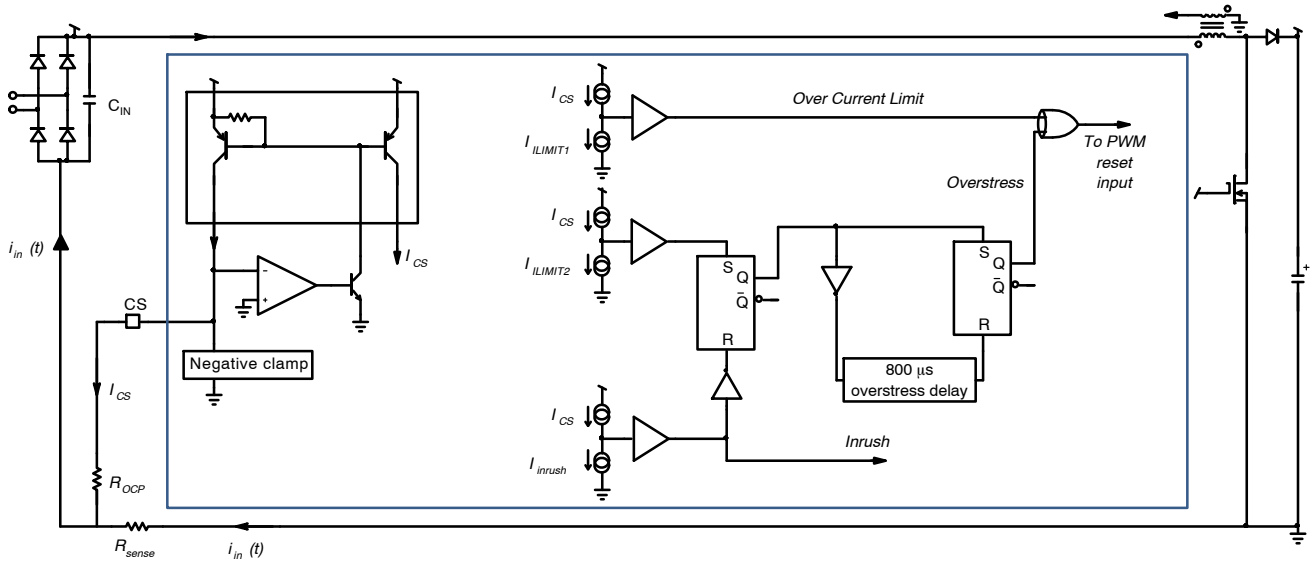


Figure 8. Current Protections

Re−using above example (R_{sense} = 30 mΩ, R_{OCP} = 2 kΩ), the overstress level of the input current is typically set to:

$$I_{in(OVS)} = \frac{2 \cdot 10^3}{30 \cdot 10^{-3}} \cdot 300 \cdot 10^{-6} = 20\ A \qquad \text{(eq. 10)}$$

Duty Ratio Control in CCM Mode

The NCP1618 re−uses the proven "predictive method" scheme implemented in NCP1653 and NCP1654 CCM PFC controllers. In other words, it directly computes the power switch on−time as a function of the inductor current. Practically, the I_{CS} current is modulated by the control signal and sourced by the V_M pin to build the CCM current information. The V_M pin signal is:

$$V_M = 0.4 \cdot R_M \cdot \frac{V_{RAMP,pk}}{V_{REGUL}} \cdot I_{CS} \quad \text{(eq. 11)}$$

Where V_{REGUL}, $V_{RAMP,pk}$ and R_M respectively are the regulation voltage (derived from $V_{CONTROL}$), the CCM oscillator peak value and the V_M pin resistor. Actually, a capacitor C_M is to be added across R_M to filter and remove the switching frequency component of the V_M pin voltage. Hence, replacing I_{CS} by its function of the inductor current given by Equation 6, it comes:

$$V_M = 0.4 \cdot R_M \cdot \frac{V_{RAMP,pk}}{V_{REGUL}} \cdot \frac{R_{sence}}{R_{OCP}} \cdot \langle I_L \rangle_{T_{SW}} \quad \text{(eq. 12)}$$

Now, $\langle I_L \rangle_{Tsw}$, the inductor current averaged over the switching frequency is the input current. Thus, Equation 12 can be changed into:

$$V_M = 0.4 \cdot \frac{R_M \cdot R_{sense}}{R_{OCP}} \cdot \frac{V_{RAMP,pk}}{V_{REGUL}} \cdot i_{in}(t) \quad \text{(eq. 13)}$$

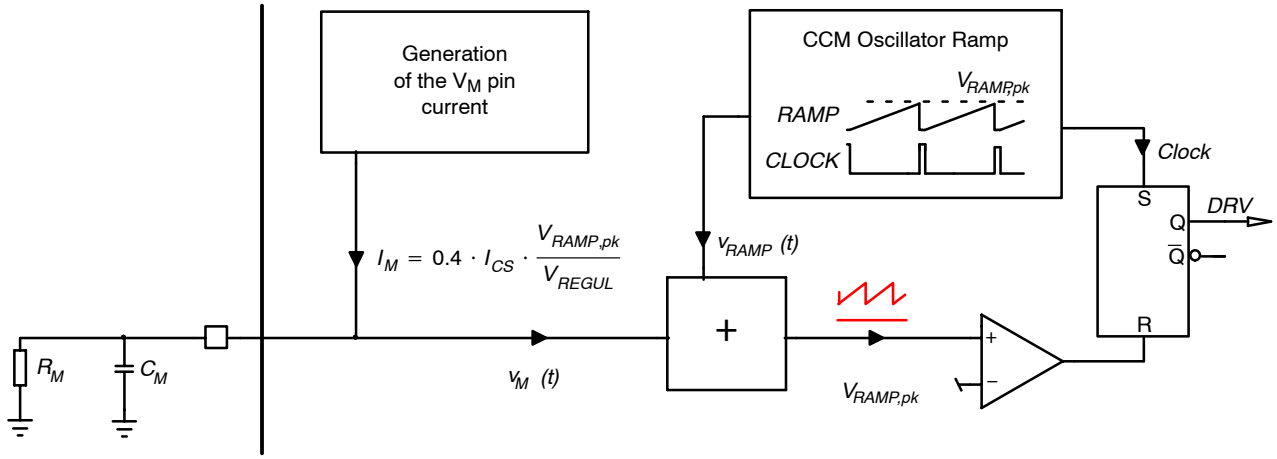


Figure 9. Duty Ratio Control in CCM Mode

Figure 9 sketches the manner the duty ratio is controlled in CCM.

Like in the NCP1653/4 controllers, when the power switch on−time starts, an oscillator ramp is added to the V_M pin voltage and the power switch opens when the sum reaches the oscillator upper threshold. Doing so, if $V_{RAMP,pk}$ designates the peak value of the oscillator ramp, the V_M voltage and the on−time (t_{on}) are linked as follows:

$$V_M = V_{RAMP,pk} \cdot \left(1 - \frac{t_{on}}{T_{SW}}\right) \quad \text{(eq. 14)}$$

Now, the off−duty−ratio of a boost converter operated in CCM is:

$$d_{off} = 1 - \frac{t_{on}}{T_{SW}} = \frac{v_{in}(t)}{V_{out}} \quad \text{(eq. 15)}$$

Combining Equations 13, 14 and 15, the following expression of the input current is obtained:

$$i_{in}(t) = 2.5 \cdot \frac{R_{OCP} \cdot V_{REGUL}}{R_M \cdot R_{sence}} \cdot \frac{v_{in}(t)}{V_{out}} \quad \text{(eq. 16)}$$

The input current is as targeted proportional to the input voltage.

The CCM regulation voltage (V_{REGUL}) is proportional to the regulation control signal provided by the "transconductance error amplifier and compensation" internal block ($V_{CONTROL}$) as follows:

- ($V_{CONTROL}$) in low−line conditions (see the "Line Range Detection" section)
- ($V_{CONTROL}$ / 4) in high−line conditions (see the "Line Range Detection" section)

Hence, the CCM input power expression is:

- Low−line conditions:

$$P_{in,avg} = \frac{2.5 \cdot R_{OCP} \cdot V_{in,rms}^2}{R_M \cdot Rsence} \cdot \frac{V_{CONTROL}}{V_{out}} \quad \text{(eq. 17)}$$

- High−line conditions:

$$P_{in,avg} = \frac{0.625 \cdot R_{OCP} \cdot V_{in,rms}^2}{R_M \cdot Rsence} \cdot \frac{V_{CONTROL}}{V_{out}} \quad \text{(eq. 18)}$$

NOTE: *The* R_M *resistance must be selected higher than 4.5 kΩ. If not, the circuit may not be able to charge the* V_M *pin to SKIP threshold* ($V_{SKIP(th)}$).

ZERO CROSSING DETECTION BLOCK

The NCP1618 optimizes the efficiency by turning on the MOSFET at the very valley when operating in critical and discontinuous conduction modes. For this purpose, the circuit is designed to monitor the voltage of a small winding taken off of the boost inductor. This auxiliary winding (called the “zero current detector” or ZCD winding) gives a scaled version of the inductor voltage which is easily usable by the controller. The PFC stage being a boost converter, this auxiliary winding voltage provides:

- $\left(-\frac{N_{AUX}}{N_P} \cdot v_{in}(t)\right)$
  during the MOSFET conduction time
- $\left(\frac{N_{AUX}}{N_P}(V_{out} - v_{in}(t))\right)$
  during the demagnetization time. This voltage used to detect the zero current detection can be small when the input voltage is nearly the output voltage.
- A voltage oscillating around zero during dead−times

Application note AND90011 discusses recommended circuitries for an accurate ZCD and OVP2 detections. Figure 10 provides one of these circuitries. In this circuit, R_7 being small, capacitor C_2 is charged to

$$\left(\frac{N_{AUX}}{N_P} \cdot v_{in}(t)\right)$$

during the on−time, so that during the demagnetization time, capacitor C_2 charges to

$$\left(\left(\frac{N_{AUX}}{N_P}(V_{out} - v_{in}(t))\right) + \left(\frac{N_{AUX}}{N_P} \cdot v_{in}(t)\right)\right),$$

that is,

$$\left(\frac{N_{AUX}}{N_P} \cdot V_{out}\right).$$

This circuitry hence provides a solid ZCD signal even if the input voltage is close to the output voltage. Also, a voltage representative of the output is obtained for an accurate over−voltage protection. As detailed in application note AND90012 (http://www.onsemi.com/pub_link/Collateral/AND90012−D.PDF), the time constants can be selected as follows in the case of 50 or 60 Hz line:

$$R_7 \cdot C_2 \cong 500\ \text{ns} \quad \text{(eq. 19)}$$

$$(R_7 + R_6) \cdot C_2 \cong 600\ \mu\text{s} \quad \text{(eq. 20)}$$

Diode D_2 ensures that when the auxiliary winding drops, the ZCD/OVP2 pin gets below the ZCD lower threshold ($V_{ZCD(th)L}$).

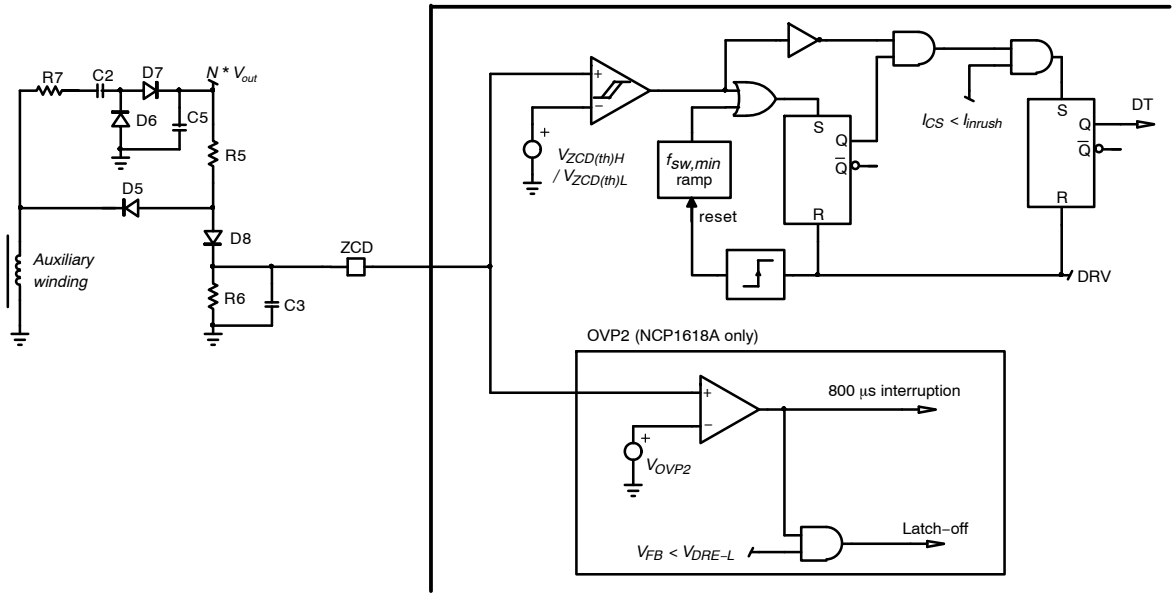


Figure 10. Zero Current Detection Block

Figure 10 shows how the NCP1618 detects the valley.

An internal comparator detects when ZCD pin voltage exceeds an upper threshold V_{ZCDH} (1 V typically). When this is the case, the inductor core is resetting and the ZCD latch is set. This latch will be reset when the next driver pulse occurs. Hence the output of the latch remains high during the whole off−time (demagnetization time + any possible dead time). The output of the comparator is also inverted to form a signal that is low when the ZCD pin voltage is higher than the V_{ZCDH} upper voltage reference of the ZCD comparator. As a result, V_{DMG} that is the AND combination of both signals is high when the ZCD pin voltage drops below the lower threshold of the ZCD comparator, that is, at the auxiliary winding falling edge. It is worth noting that as portrayed by Figure 11, V_{AUX} is also representative of the MOSFET drain−source voltage (“V_{DS}”). More specifically,

when V_{AUX} is below zero, V_{DS} is minimal (below the input voltage v_{in} (t)). That is why V_{DMG} is used to enable the driver so that the MOSFET turns on when its drain−source voltage is low. Valley switching reduces the losses and interference.

IMPORTANT NOTES:

- *Some options (see Table 1) does not feature the OVP2 protection. In this case, a simple resistor (or two series ones if required to pass safety tests) can be used between the auxiliary winding and the ZCD pin as shown by Figure 2 where R_{ZCD1} denotes this resistor.*
- *The ZCD pin impedance (for instance R_3 of Figure 10), must be higher than 7.5 kΩ not to trigger the ZCD pin short−to ground protection.*

If no ZCD can be detected when the circuit operates in FCCrM mode, the circuit cannot use the valley detection to start a new current cycle. In this case, the next DRV pulse is forced by the DCM minimum frequency ramp ($f_{sw,min}$ ramp of Figure 10) which acts as a watchdog.

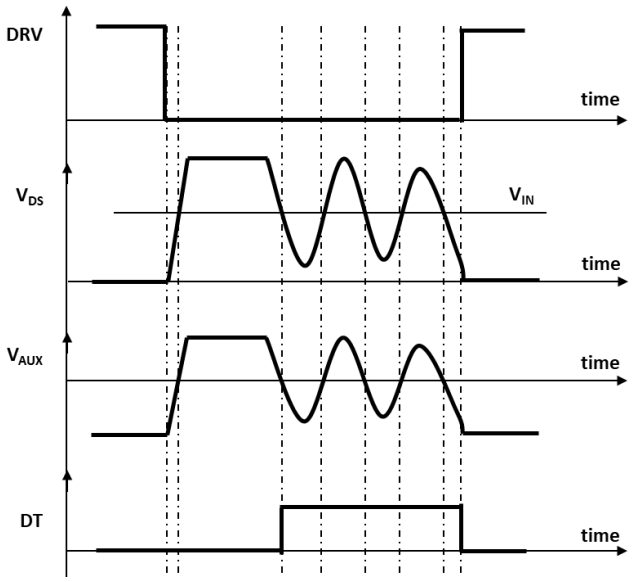


Figure 11. Zero Current Detection Timing Diagram (V_{AUX} is the Voltage Provided by the ZCD Winding)

Note that the circuit can detect faulty conditions of the ZCD pin:

- A permanent 1 μA current source pulls up the pin if it happens to be floating. The circuit is hence maintained off
- If the pin is grounded, no falling edge of the auxiliary winding can be detected. The DRV remains off until the DCM minimum frequency ramp initiates a new cycle. Before the new pulse is generated, the circuit senses the pin impedance by sourcing 250 μA. No DRV pulses are generated until the pin voltage exceeds V_{ZCDH}. Hence, the part is inhibited when the pin is grounded. Not to trigger this protection, the pin impedance (for instance R_3 of Figure 10. must be higher than 7.5 kΩ).

The ZCD pin is shortly grounded when the MOSFET turns off (ZCD leading edge blanking − LEB). The LEB of 100 ns typical, is implemented to prevent the OVP2 comparator from tripping due to turn−off noise.

OVP2

The ZCD pin signal (V_{ZCD}) can be used to detect an OVP fault.

Practically, it is compared to V_{OVP2} (4 V typically). If V_{ZCD} exceeds V_{OVP2}, the PFC stage stops operating for 800 μs. In addition, if when an OVP2 fault is detected, the FB voltage is below $V_{DRE−L}$, that is the threshold below which the dynamic response enhancer trips (95.5% of V_{REF} typically), the circuit detects that one of two networks for output voltage sensing is wrong. As a consequence, the circuit latches off. See Figure 9.

OUTPUT VOLTAGE CONTROL (REGULATION BLOCK)

The general structure is sketched by Figure 12.

A small 250 nA sink current is built−in to pull down the pin if the *FB* pin is accidentally open. In this case, V_{FB} being less than V_{UVP} (300 mV typically), the UVP protection trips and thus, protects the circuit if the *FB* pin is floating.

The fast OVP comparator is analogue and directly monitors the feedback pin voltage. The rest of the block which is digital, receives a digitized feedback value. The sampling rate is 10 kHz.

The digital “transconductance error amplifier and compensation” block provides the control signal $V_{CONTROL}$ (which is devoid of the PFC stage 120 or 100 Hz ripple) to control the duty ratio.

Practically, the signal V_{REGUL} does dictate the on−time. V_{REGUL} differs from $V_{CONTROL}$ only in the case of a soft−OVP event (see “soft−OVP” paragraph) and in CCM when in high line where (V_{REGUL} = $V_{CONTROL}$ / 4). In all other cases, (V_{REGUL} = $V_{CONTROL}$).

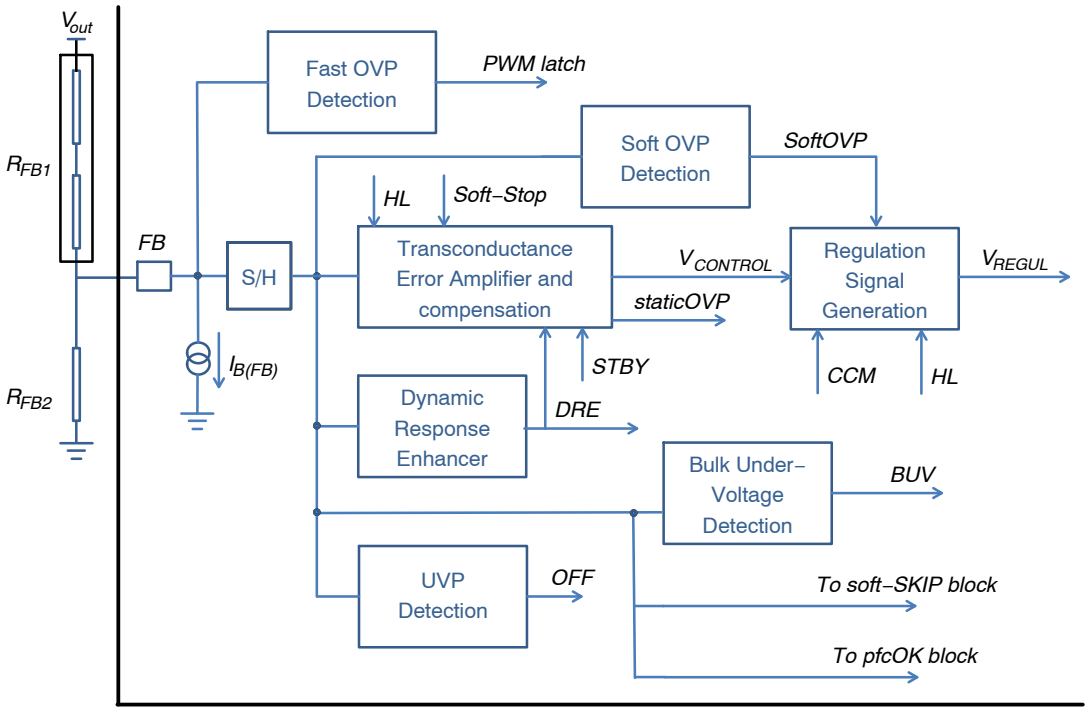


Figure 12. Regulation Circuitry

Output Voltage Levels

The regulation block and the soft−OVP, UVP and DRE comparators monitor the FB pin voltage. Based on the typical value of their parameters and if ($V_{out,nom}$)is the output voltage nominal value (e.g., 390 V), we can deduce the following typical levels:

- Output Regulation Level: $V_{out,nom} = V_{REF} / k_{FB}$
- Output Soft−OVP Level: $V_{out,SOVP} = 105\% \cdot V_{out,nom}$
- Output Fast−OVP Level: $V_{out,FOVP} = 107\% \cdot V_{out,nom}$
- Output UVP Level: $V_{out,UVP} = 12\% \cdot V_{out,nom}$
- Output DRE Level: $V_{out,DRE} = 95.5\% \cdot V_{out,nom}$
- Output BUV Level: $V_{out,BUV} = 72\% \cdot V_{out,nom}$
- Output Upper Soft−SKIP Level: $(V_{out,softSKIP})_H = 103\% \cdot V_{out,nom}$
- Output Lower Soft−SKIP Level: $(V_{out,softSKIP})_L = 98\% \cdot V_{out,nom}$

Where:

- V_{REF} is the regulation reference voltage (2.5 V typically)
- R_{FB1} and R_{FB2} are the feedback resistors (see Figure 1).
- k_{FB} is the scale down factor of the feedback resistors $\left(k_{FB} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}}\right)$.
- $V_{out,softSKIP-H}$ and $V_{out,softSKIP-L}$ are the levels between which the output voltage swings when in soft−SKIP mode (see the "Soft−SKIP Mode" section)

StaticOVP

The circuit stops providing DRV pulses when $V_{CONTROL}$ reaches its bottom level.

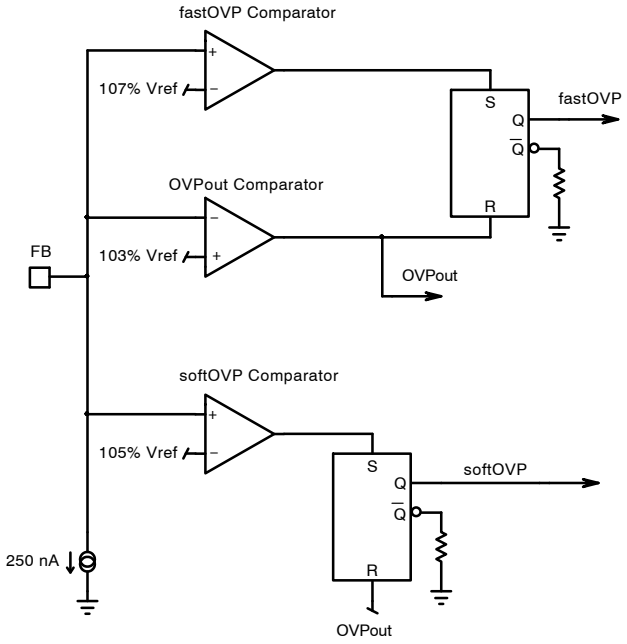


Figure 13. Fast and Soft OVP Protections

Soft−OVP

As sketched by Figure 13, the soft−OVP trips when the feedback voltage exceeds 105% of V_{REF} and remains in this mode until V_{FB} drops below 103% of V_{REF}. When the soft−OVP trips, it reduces the power delivery down to zero in 4 steps:

- Step 1: V_{REGUL} drops to 75% of the $V_{CONTROL}$ value for 400 µs
- Step 2: V_{REGUL} drops to 50% of the $V_{CONTROL}$ value for 400 µs
- Step 3: V_{REGUL} drops to 25% of the $V_{CONTROL}$ value for 400 µs
- Step 4: V_{REGUL} drops and remains to 0 until the soft−OVP fault is over, that is, when the output voltage drops below 103% of its regulation level.

FastOVP

As sketched by Figure 13, the fast−OVP trips when the feedback voltage exceeds 107% of V_{REF} and remains in this mode until V_{FB} drops below 103% of V_{REF}. The drive is immediately stopped when the fast OVP is triggered.

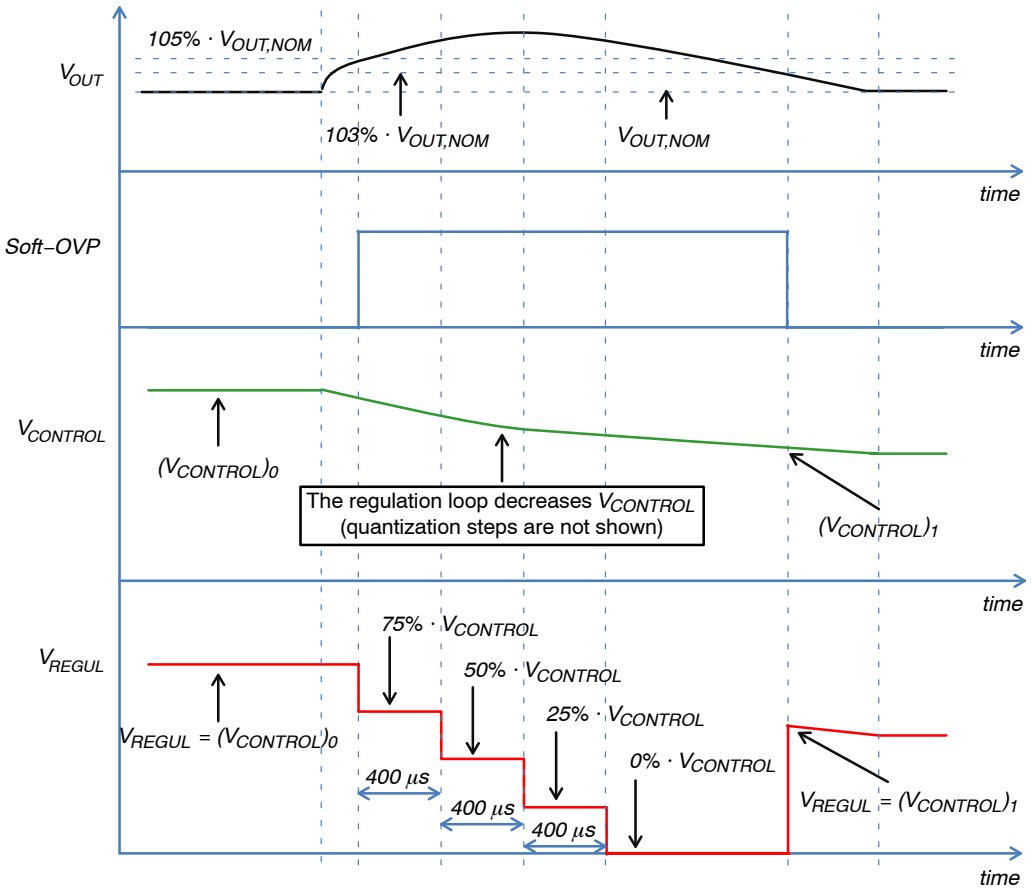


Figure 14. Soft−OVP

Dynamic Response Enhancer

The NCP1618 embeds a "dynamic response enhancer" circuitry (DRE) which firmly contains under−shoots. An internal comparator monitors the feed−back voltage on pin 1 (V_{FB}) and when V_{FB} is lower than 95.5% of the regulation reference voltage (V_{REF}), it speeds−up the charge of the compensation network. Practically a 10x increase in the loop gain is forced until the output voltage has reached 98% of its nominal value.

Soft−Stop Sequences

A soft−stop sequence is forced when the circuit must stop operating in a smooth manner to prevent bouncing effects possibly resulting from an abrupt interruption. Soft−stop gradually reduces $V_{CONTROL}$ to zero, in the following cases:

- A line−sag or a brownout fault is detected
- A BUV fault is detected
- When in soft−SKIP mode, the output voltage reaches its upper threshold, the active phase of the burst ends. At that moment, soft−stop leads to a gradual stop of the power delivery and a smooth idle phase start for a minimized risk of audible noise.

A soft−skip sequence is terminated when $V_{CONTROL}$ reaches its bottom level. In the soft−SKIP case, the soft−stop sequence is also immediately ended when the output voltage drops below the restart level, so that the restart of operation is not delayed until the total $V_{CONTROL}$ discharge.

SOFT−SKIP MODE

As detailed in application note AND90011 (http://www.onsemi.com/pub_link/Collateral/AND90011−D.PDF), the circuit is designed to be externally forced to enter the soft−SKIP mode by applying negative pulses on either the *pfcOK* pin or the V_M pin. In CCM mode, the V_M pin provides the current information necessary to modulate the duty−ratio. In CrM and DCM modes of operation, this pin is pulled−up to $V_{M,DCM}$ (2.5 V typically). If the pin is externally forced below $V_{SKIP(th)}$ (1.5 V typically) for 100 μs or more, the circuit enters the soft−SKIP mode.

The soft−SKIP mode can also be triggered by generating a negative pulse on the *pfcOK* pin. To do so, the *pfcOK* pin must be pulled down below V_{SKIP2} (0.4 V min) for T_{SKIP2} (33 μs max) or more. Note that in this case, the *pfcOK* signal may have to be filtered before being applied to the downstream converter so that the negative pulses do not stop its operation. Figure 15 illustrates a possible implementation with ON Semiconductor LLC controller NCP13992.

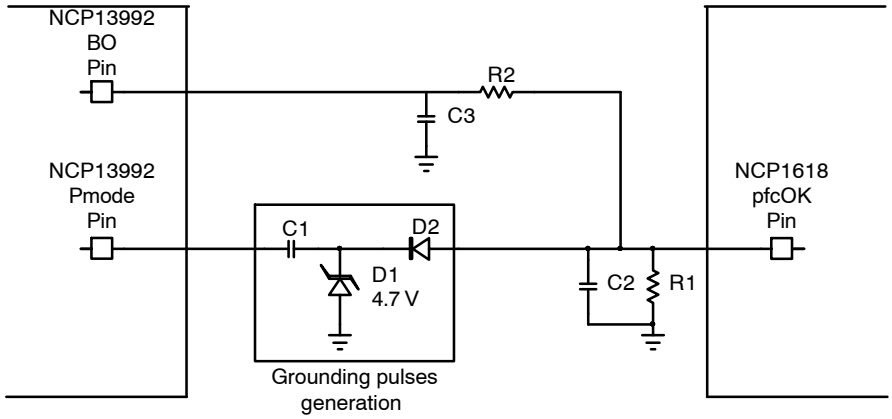


Figure 15. Circuitry to Control the Soft−SKIP Mode

When the V_M or *pfcOK* pins receive a grounding pulse, the circuit detects a soft−SKIP condition. As a result, as illustrated by Figure 16, the NCP1618:

- First charges up the output voltage to 103% of its nominal voltage (103% $V_{out,nom}$).
- Then, enters a soft−stop sequence to gradually reduce the line current and thus minimize the risk of audible noise. If the output voltage reaches the soft−OVP level (105% $V_{out,nom}$), the protection trips and the 4−step stop illustrated by Figure 14 takes place.
- When the soft−stop sequence (or the 4−step stop) is finished, the circuit enters the deep idle mode: the part stops switching and all the non−necessary circuitries are turned off so that the circuit consumption is reduced to a minimum ($I_{CC} = I_{CC3}$ which is 250 μA typically). Since no energy is provided to the bulk capacitor, the output voltage decays.
- When the output voltage drops below 98% of its nominal voltage (98% * $V_{out,nom}$), the circuit exits the deep idle mode. Operation resumes and the output voltage charges up to 103% of its nominal voltage again.
- When the output voltage reaches 103% of its nominal voltage, there are two possibilities:
  - The V_M or the *pfcOK* pins have received a grounding pulse during this latest charge to 103% $V_{out,nom}$. In this case, the circuit remains in soft−SKIP mode, i.e., the circuit enters a new deep idle mode phase at the end of the soft−stop (or the 4−step stop) sequence.
  - The V_M or the *pfcOK* pins have not received a grounding pulse during this latest charge to 103% $V_{out,nom}$. In this case, the circuit recovers the normal operation until the V_M or *pfcOK* pins receive a grounding pulse

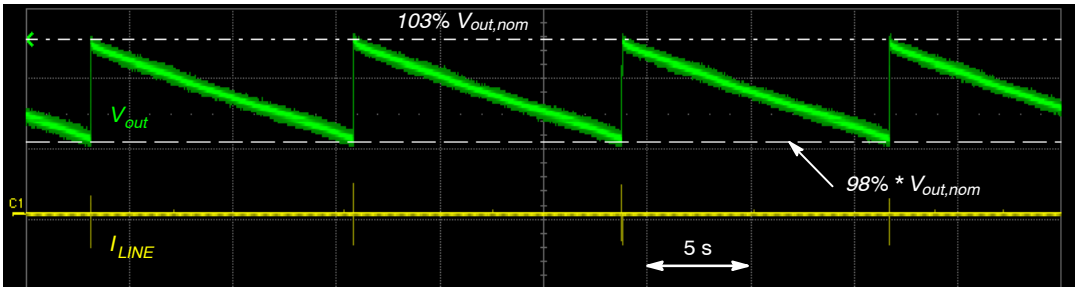


Figure 16. Soft−SKIP Operation

NOTES:

- The circuit cannot enter the soft−SKIP mode when it operates in CCM.
- The soft−stop sequence is interrupted if not finished when the output voltage reaches the soft−SKIP bottom threshold ($V_{out,nom}$) so that the circuit can resume normal operation.
- When in soft−SKIP mode, the NCP1618 is prevented from entering CCM during the active burst. This is to minimize the risk of audible noise by limiting burst energy. However, if during the soft−SKIP active burst, a sudden load increase causes the output voltage to drop below the DRE level (95.5% of $V_{out,nom}$) while V_M pin is above 1.5 V, the circuit can enter CCM if necessary to deliver the power. Such a situation normally occurring when the application gets loaded, the circuit will leave the soft−SKIP mode at the end of this burst when the output voltage is charged to 103% $V_{out,nom}$.

PFCOK SIGNAL

The *pfcOK* pin is designed to control the operation of the downstream converter. It is in high state when the PFC stage is in nominal operation and grounded when the PFC stage is in start−up phase or in a fault condition. Using the *pfcOK* signal to enable/disable it, the downstream converter can be optimally designed for the narrow voltage range nominally provided by the PFC stage in normal operation.

Practically, the *pfcOK* pin is grounded when the PFC stage enters operation and remains in low state until the output voltage has nearly reached its nominal level (practically when V_{FB} reaches 98%V_{REF}). At that moment, the *pfcOK* pin sources a current proportional to the feedback voltage ($k \cdot V_{FB}$). See Figure 17. Placing an external resistor between the *pfcOK* and GND pins, we obtain a voltage V_{pfcOK} which is proportional to the bulk voltage and can serve as a feedforward signal for the downstream converter. k typical value is 10 μA/V so that the pfcOK pin typically sources 25 μA when the FB voltage is 2.5 V (regulation level).

Conversely, when a major fault is detected (brown−out, UVLO, Thermal shutdown, OVP2 latch off, UVP and BUV), the internal OFF signal turns high and the *pfcOK* pin is grounded to prevent the downstream converter from operating in the abnormal conditions causing these faults.

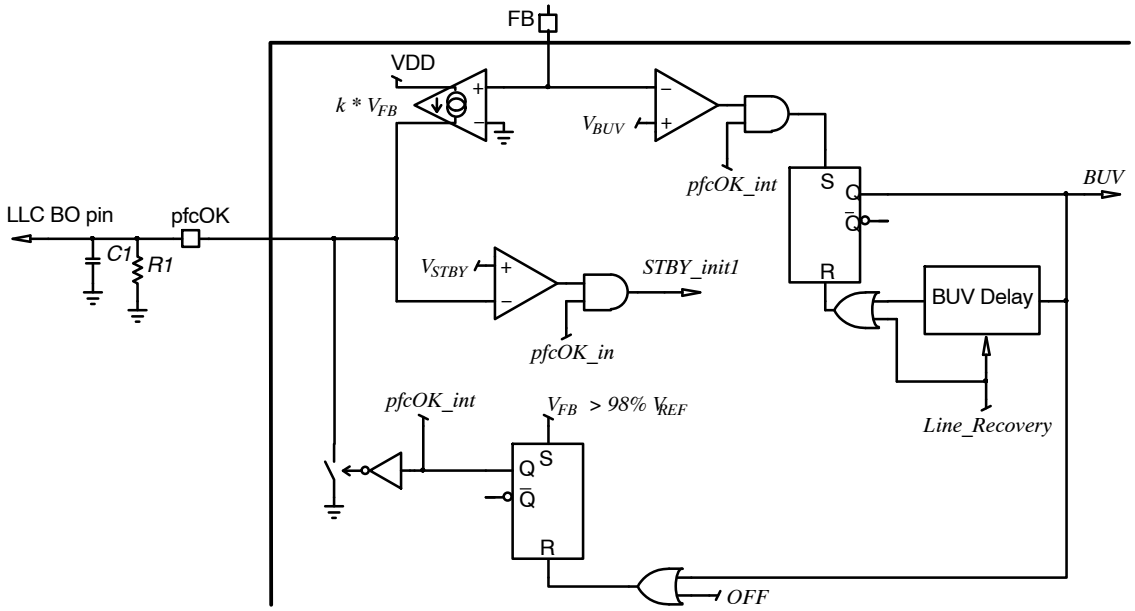


Figure 17. *pfcOK* Block

In particular, when the feedback voltage drops below the V_{BUV} internal reference (1.8 V typically), a BUV fault is detected (BUV stands for Bulk Under−voltage). Corresponding output voltage BUV threshold is:

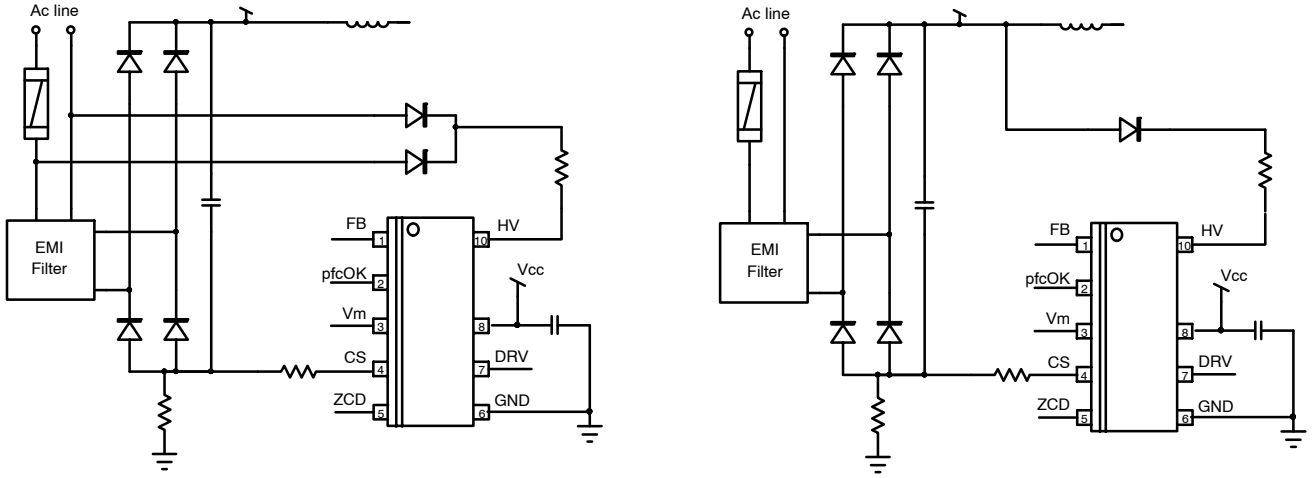
$$V_{out,BUV} = \frac{V_{BUV}}{V_{REF}} \cdot V_{out,nom} \qquad \text{(eq. 21)}$$

When a BUV fault is detected:

- The *pfcOK* pin is grounded
- A soft−stop sequence is started during which the power delivery gradually drops to zero
- When the soft−stop sequence ends, the PFC stops operating until the T_{BUV} delay has elapsed (515 ms typically). However, if the BUV protection trips during a line sag condition, the T_{BUV} delay is bypassed and operation immediately resumes when the line recovers. The wakeup information is provided by signal "*Line_Recovery*" generated by the line−sag block (see Figure 20). This enables a rapid operation recovery when the line fault is over.

INPUT VOLTAGE SENSING

The high voltage (HV) pin is a multi−functional pin, which in addition to the startup current source, provides access to the brownout, line sag, line range detectors and X2 capacitor discharge. The brownout / line−sag detector detects too low line levels and the line range detector determines the presence of either 110 V or 220 V ac mains. Depending on the detected input voltage range, the NCP1618 internally adjusts device parameters to optimize the system performance. Line and neutral are diode "ORed" before connecting to the HV pin as shown in Figure 17. The diodes prevent the pin voltage from going below ground. Whatever the HV input connection is, a small resistor (R_{HV}) in series with the diodes can limit the current during transient events. This resistor (of 1 or 2 kΩ for instance, 3 kΩ maximally), must be low enough. If not, the HV pin voltage may drop below HV_{MIN} (38 V) during the VCC charge phase because of the voltage drop the start−up current generates across R_{HV}. In such a case, the start−up current source may reduce, leading to a longer V_{CC} charge. Also, R_{HV} must be able to dissipate the power produced by the startup current when the NCP1618 charges up the V_{CC} capacitor.



a) The line terminals are sensed

b) The input voltage is sensed

Figure 18. High−Voltage Input Connection

LINE−SAG DETECTION

Tests can be made which consist of rapidly and repeatedly plug and unplug the power supply. If no specific function is implemented, a huge current can take place when the power supply is powered. This is because during the mains interruption, $V_{CONTROL}$ dramatically rises since no more power can be delivered to the output.

The line−sag detection block detects short mains interruption to prevent an excessive stress when the line is back. As sketched by Figure 19, a line−sag situation is detected when the input voltage remains below $V_{BO(stop)}$ for $T_{SAG(blank)}$.

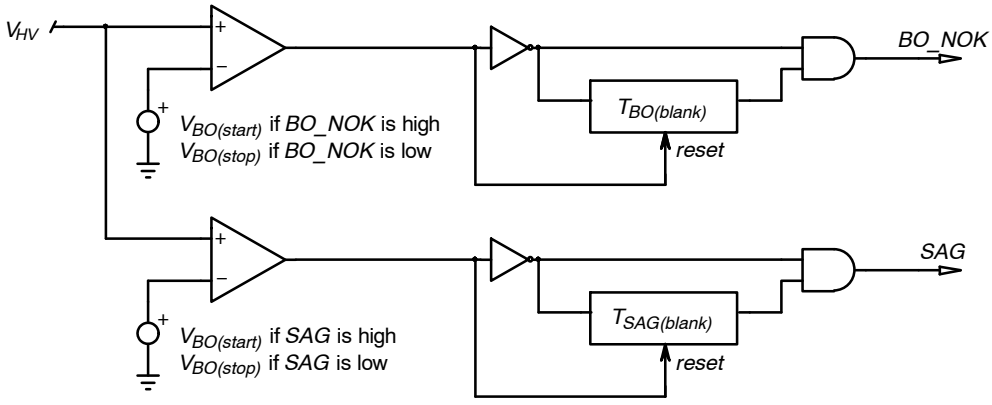


Figure 19. Line−Sag and Brown−Out Detection

When a line−sag condition is detected, the NCP1618 starts a soft−stop sequence to gradually discharge $V_{CONTROL}$ down−to−zero and hence, to smoothly stop operation. It also disables the CCM mode to reduce more rapidly the power delivery during the line−sag period. When the line recovers, it is required to restart the operation as soon as possible and in a clean manner. Signal "Line_Recovery" of Figure 20 provides the wakeup information.

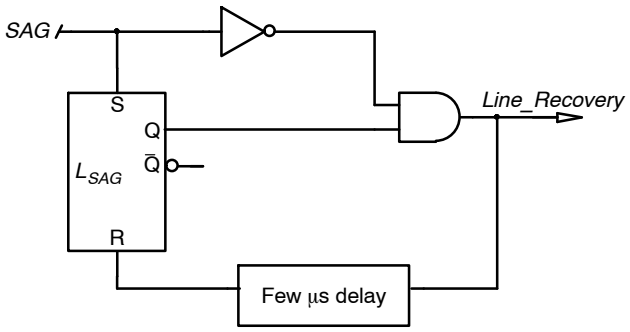


Figure 20. "Line_Recovery" Signal

The signal "*Line_Recovery*":

- Resets the BUV timer. It is because a long line−sag event is likely to cause a BUV detection. When a BUV fault is detected, no restart is possible until the BUV timer has elapsed. If a BUV fault is detected during a line−sag sequence, we want operation to be resumed as a soon as the line recovers (see Figure 17).
- Interrupts the soft−stop discharge if not completed and ground $V_{CONTROL}$ for a clean start−up.

BROWN−OUT PROTECTION

The controller is enabled once V_{HV} is above the upper brownout threshold, $V_{BO(start)}$, and V_{CC} reaches $V_{CC(on)}$. Figure 21 shows typical power−up waveforms. The brownout timer ($t_{BO(blank)}$) is enabled once V_{HV} drops below the lower brownout threshold, $V_{BO(stop)}$ and a brown−out fault is detected if V_{HV} doesn't exceed $V_{BO(stop)}$ before the brownout timer expires. The timer is set long enough to pass line−dropout tests.

Figure 21 illustrates a line−dropout event.

The circuit operates normally and suddenly, the line reduces to a low level. Due to the dropout, the HV voltage drops below the $V_{BO(stop)}$ level. The blanking time $t_{BO(blank)}$ is started and a brown−out fault is detected since the HV voltage has remained below $V_{BO(start)}$ until the timer expires. As a result, the PFC stage stops operating and the *pfcOK* pin is grounded. If as sketched in Figure 21, no external power source maintains the V_{CC} voltage, V_{CC} swings between $V_{CC(off)}$ and $V_{CC(on)}$. When the line recovers, the circuit does not immediate resume operation but first turns on the HV startup to charge V_{CC} up to $V_{CC(on)}$ so that a clean restart is obtained. If V_{CC} is already higher than $V_{CC(on)}$ when the line recovers, the NCP1618 restarts immediately.

In Figure 21, it is assumed that V_{CC} is maintained by the downstream converter until *pfcOK* drops to zero. It is also supposed that the output voltage remains above the bulk under−voltage threshold – $V_{out,BUV}$ – when the BO fault is detected. If a BUV fault had been detected before the brown−out timer elapsed, the *pfcOK* pin would have already been grounded when the BO fault is detected. The DRV pulses shown after the line−sag illustrate the soft−stop sequence. Note that when in high state, the *pfcOK* signal is proportional to the output voltage. Its gradual decay during the main dropout is representative of the output voltage drop until the BO fault is detected causing the *pfcOK* grounding.

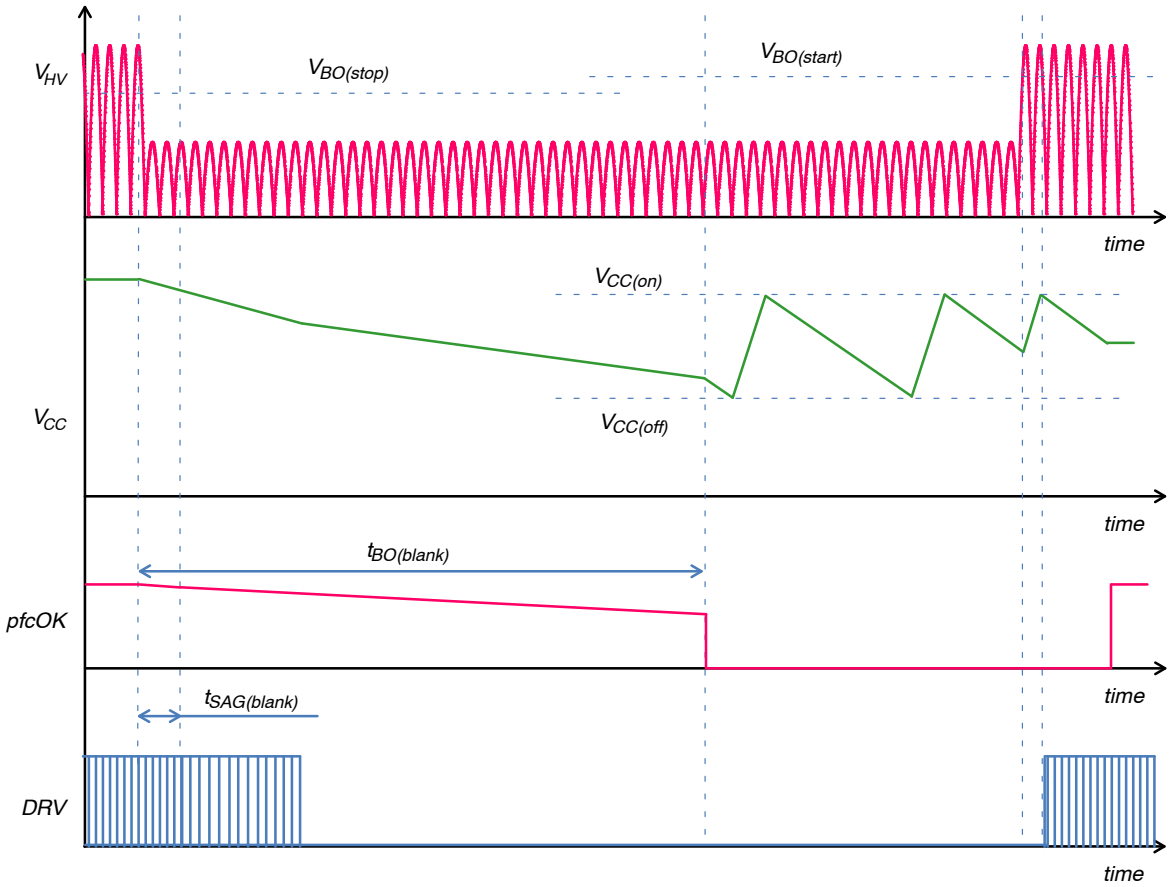


Figure 21. Brown−Out Sequence (In this Figure, it is Assumed that V_{CC} is Maintained by the Downstream Converter until *pfcOK* Drops to Zero)

LINE RANGE DETECTION

The input voltage range is detected based on the peak voltage measured at the HV pin.

The controller compares V_{HV} to the high−line select threshold, $V_{lineselect(HL)}$, typically 236 V. A blanking time $T_{filter(HV)}$ of 300 μs typically, prevents erroneous detection due to noise. Once V_{HV} exceeds $V_{lineselect(HL)}$, the PFC stage operates in “high−line” (Europe/Asia).

The controller switches back to “low−line” mode if V_{HV} remains below $V_{lineselect(LL)}$ (which is 222 V typically, i.e., 14 V less than $V_{lineselect(HL)}$, thus offering an hysteresis) for the t_{line} timer delay (25 ms typically).

If the controller transitions to “low−line”, it is prevented from switching back to “high−line” until the lockout timer $t_{line(lockout)}$ (typically 500 ms), expires. The timer and logic is included to prevent unwanted noise from toggling the operating line level.

The line range detection circuit optimizes the operation for universal (wide input mains) applications. Practically, in “high−line”:

- The regulation bandwidth and the CCM gain are divided by 4
- The $V_{CONTROL}$ below which frequency foldback starts is reduced by 2.

X2 CAPACITORS DISCHARGE

Safety agency standards require the input filter capacitors to be discharged once the ac line voltage is removed. A resistors network is the most common method to meet this requirement. Unfortunately, such a solution consumes power across all operating modes and these losses are generally unacceptable when high efficiency is required in light− and no−load conditions.

The NCP1618 integrates an active circuitry to discharge the input filter capacitors upon removal of the ac line voltage. The line removal detection circuitry is always active to ensure safety compliance.

The line removal is detected by digitally sampling the voltage present at the *HV* pin, and monitoring its slope. As illustrated by Figure 22, a timer, $t_{line(removal)}$, is used to detect when the slope of the input signal is below the resolution level. The timer is reset any time a positive or negative slope is detected. Once the timer expires, a line removal condition is acknowledged initiating an X2 capacitor discharge. In this case, the *HV* pin sinks $I_{HV(discharge)}$, the drive is disabled and the *pfcOK* signal transitions low.

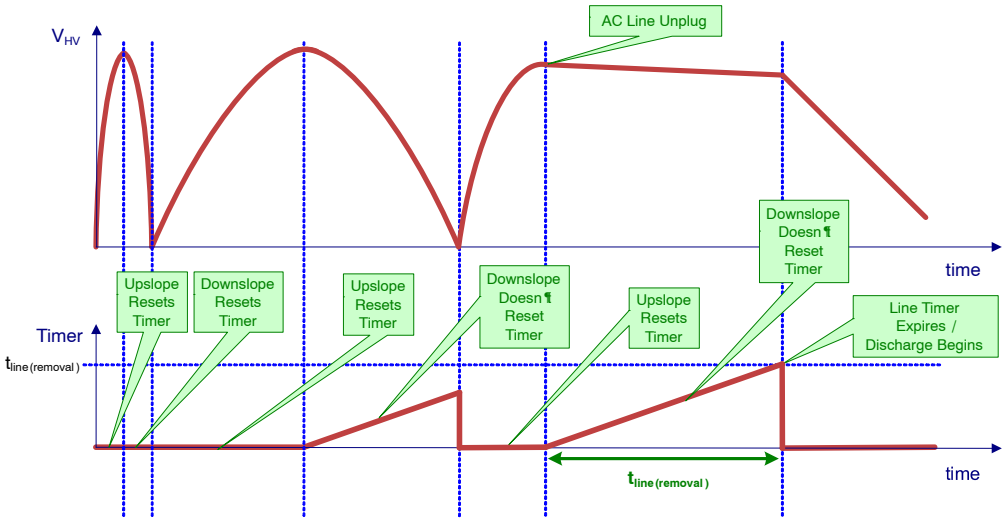


Figure 22. Line Removal Detection Timing

The discharging process continues until the voltage at HV pin (across the X2 capacitor) is lower than the $V_{HV(discharge)}$ level. This feature allows the device to discharge large X2 capacitors in the input line filter to a safe level – refer to Figure 23.

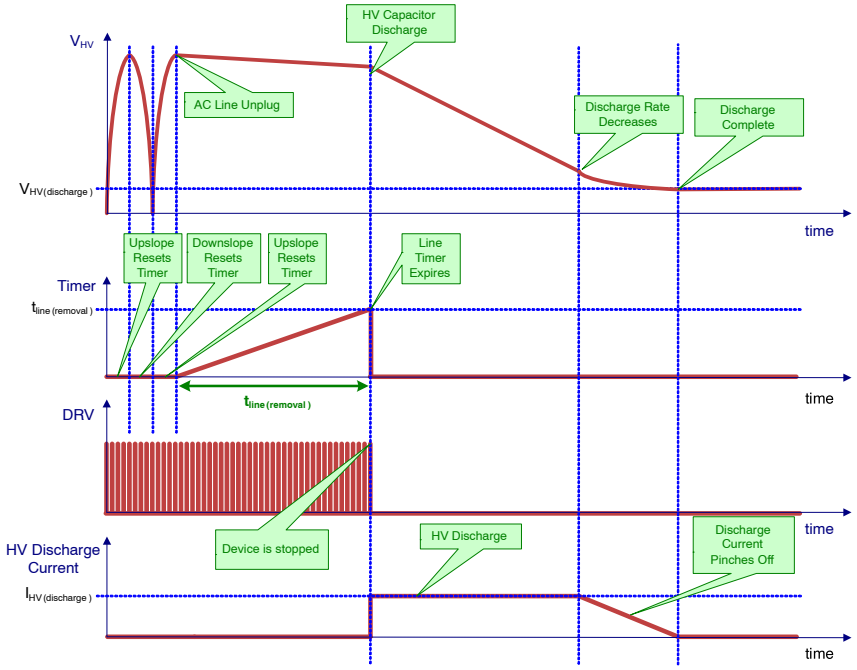


Figure 23. X2 Discharge Timing

It is important to note that the HV pin cannot be connected to any dc voltage due to this feature, i.e. directly to bulk capacitor. The diodes connecting the AC line to the HV pin must be placed after the system fuse.

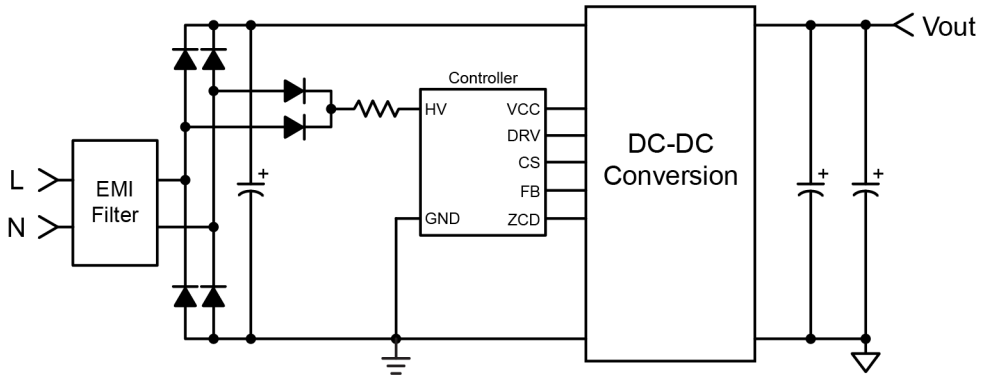


Figure 24. HV Pin Connection for X2 Capacitor Discharging Function

The HV pin can directly receive the voltage provided by diodes as shown by Figure 3. However, it can be useful to place a resistor (R_{HV}) in series with the HV pin to improve surge immunity. The R_{HV} resistance must remain low. This is because as aforementioned the discharge phase ends when the HV voltage goes below $V_{HV(discharge)}$. At this point, still considering the Figure 24 connection, the actual voltage across the line filter capacitor is:

$V_{HV(discharge)} + (R_{HV} * I_{HV(discharge)}) + 2*V_F$

where V_F is the forward voltage of the conducting diodes.

In the event that line voltage is reapplied during a discharge phase, the circuit will simply continue to discharge until the line zero crossing occurs, at which point V_{HV} will drop to $V_{HV(discharge)}$ and a new start−up cycle will commence.

OFF MODE

The circuit turns off when the circuit detects one of the following major faults:

- BONOK: a brown−out fault is detected (too low a line voltage for proper operation).
- BUV: too low a bulk voltage is detected for proper operation of the downstream converter.
- TSD: The thermal shutdown protection stops the circuit operation when the junction temperature (T_J) exceeds 150°C typically. The controller remains off until T_J goes below nearly 100°C.
- UVLO: Incorrect feeding of the circuit (refer to the STARTUP SEQUENCE / *VCC* MANAGEMENT section)
- UVP: an Output Under−Voltage situation is detected when V_{FB} is less than V_{UVP} (12% of V_{REF}, typically)
- STDWN: if an OVP2 condition is detected on the ZCD pin while the FB pin voltage is not above V_{DRE-H} (95.5% of V_{REF}, typically), the circuit latches off.

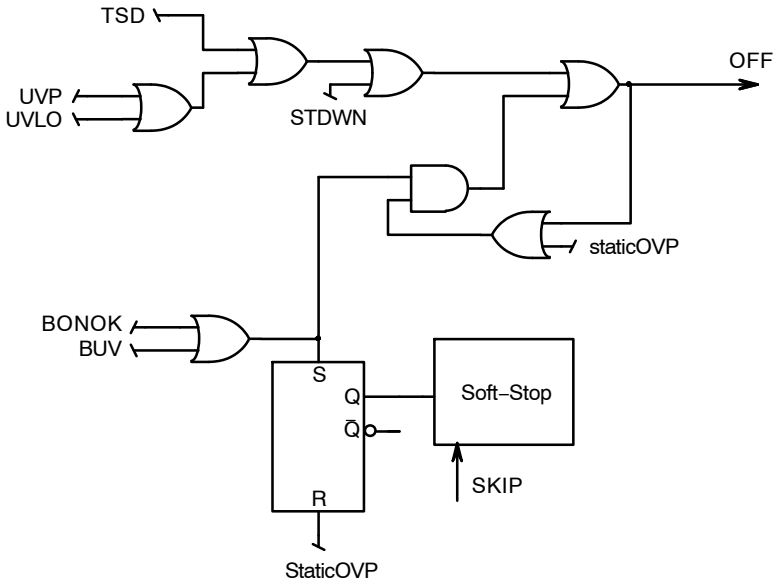


Figure 25. Faults Leading to the OFF Mode

When one of the TSD, UVP, UVLO and STDWN faults is detected, the part immediately turns off:

- The DRV pin is disabled.
- The pfcOK pin is grounded
- The circuit consumption drops to I_{CC1}

When a BUV fault is detected, *pfcOK* immediately turns low to disable the downstream converter but the part does not stop operating. Instead, a soft−stop sequence is forced to gradually decay the power delivery until the *staticOVP* level is reached. At that moment, the circuit turns off.

When a BONOK fault is detected, *pfcOK* keeps high and the part enters a soft−stop sequence to gradually decay the power delivery until the *staticOVP* level is reached. At that moment, the circuit turns off leading the drive pin to be disabled, the *pfcOK* output to be grounded and the circuit consumption to be reduced.

In the OFF mode, if it is not maintained by an external power source, V_{CC} cycles up and down between the $V_{CC(on)}$ and $V_{CC(off)}$ levels. When the fault having caused the off mode is removed, the circuit does not recover until V_{CC} reaches $V_{CC(on)}$. Practically:

- The circuit immediately restarts if V_{CC} is above $V_{CC(on)}$
- If when the fault is removed, V_{CC} is below $V_{CC(on)}$ and the start−up current source is on, the circuit continues charging V_{CC} and resumes operation when V_{CC} exceeds $V_{CC(on)}$.
- If when the fault is removed, V_{CC} is below $V_{CC(on)}$ and the start−up current source is off, the circuit immediately (without waiting for the $V_{CC} < V_{CC(off)}$ condition) enters a V_{CC} charging phase and resumes operation when V_{CC} exceeds $V_{CC(on)}$.

Figure 21 illustrates this recovering process in the case of a brown−out case.

FAILURE DETECTION

When manufacturing a power supply, elements can be accidentally shorted or improperly soldered. Such failures can also happen to occur later on because of the components fatigue or excessive stress, soldering defaults or external interactions. In particular, adjacent pins of controllers can be shorted, a pin can be grounded or badly connected. Such open/short situations are generally required not to cause fire, smoke nor big noise. The NCP1618 integrates functions that ease meeting this requirement. Among them, we can list:

- *Floating feedback pin*

  A 250 nA sink current source pulls down the FB voltage so that the UVP protection trips and prevents the circuit from operating if this pin is floating. This current source is small (450 nA maximum) so that its impact on the output regulation and OVP levels remain negligible with the resistor dividers typically used to sense the bulk voltage.
- *Improper connection of the ZCD pin*

  The ZCD pin sources a 1 μA current to pull up the pin voltage and hence disable the part if the pin is floating. If the ZCD pin is grounded before operation, the circuit cannot monitor the ZCD signal and no DRV pulse can be generated until the DCM minimum frequency ramp has elapsed. At that moment, the circuit sources a 250 μA current source to pull−up the ZCD pin voltage. No drive pulse is initiated until the ZCD pin voltage exceeds the ZCD 1 V threshold. Hence, if the pin is grounded, the circuit stops operating. *Circuit operation requires the pin impedance to be 7.5 kΩ or more, the tolerance of the NCP1618 impedance testing function being considered over the −40°C to 125°C temperature range.*
- *Improper connection of the CS pin*

  A comparator to 250 mV senses the CS pin. If the CS pin exceeds this level for 1 or 2 μs, the part is off for the 800 μs delay time. In addition, the CS pin sources a 1 μA current to pull up the pin voltage and hence disable the part if the pin is floating. The CS short−to−ground is also detected as follows: whenever the input voltage is higher than the brown−out threshold and no I_{CS} current higher than $I_{in-rush}$ is detected at the end of a MOSFET conduction phase (DRV high), the circuit sources a 250 μA current source to pull−up the CS pin voltage. No drive pulse is initiated until the CS pin voltage exceeds the 250 mV fault threshold. Hence, if the pin is grounded, the circuit stops operating. *Circuit operation requires the pin impedance to be 1.5 kΩ or more, the tolerance of the NCP1618 impedance testing function being considered over the −40°C to 125°C temperature range.*

RECOMMENDED LAYOUT

The correct layout is key step towards to reliable operation of designed application. The recommended layout of NCP1618 PFC controller is illustrated in Figure 26. The most important part of layout is connection components between CS pin of IC and sensing power resistor. The components, especially R_OCP2 has to be placed as close as possible to CS pin to limit possibility of noise coupling to high impedance trace.

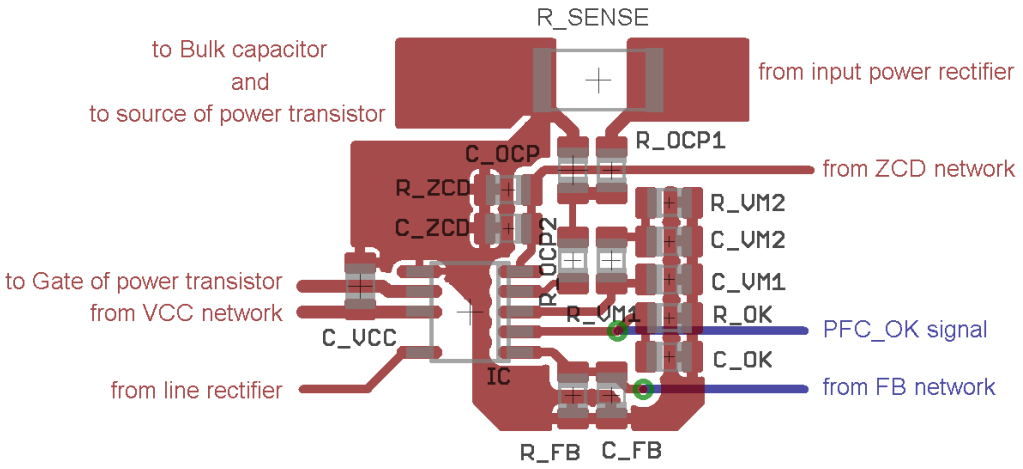


Figure 26. Recommended Layout of NCP1618 PFC Controller

ORDERING INFORMATION

Device Order Number	Specific Device Marking	Package Type	Shipping†
NCP1618BDR2G	NCP1618B	SOIC−9 NB (Pb−Free)	2500 / Tape & Reel
NCP1618CDR2G	NCP1618C	SOIC−9 NB (Pb−Free)	2500 / Tape & Reel
NCP1618DDR2G	NCP1618D	SOIC−9 NB (Pb−Free)	2500 / Tape & Reel
NCP1618FDR2G	NCP1618F	SOIC−9 NB (Pb−Free)	2500 / Tape & Reel
NCP1618HDR2G	NCP1618H	SOIC−9 NB (Pb−Free)	2500 / Tape & Reel
NCP1618JDR2G	NCP1618J	SOIC−9 NB (Pb−Free)	2500 / Tape & Reel
NCP1618KDR2G	NCP1618K	SOIC−9 NB (Pb−Free)	2500 / Tape & Reel
NCP1618LDR2G	NCP1618L	SOIC−9 NB (Pb−Free)	2500 / Tape & Reel

DISCONTINUED (Note 5)

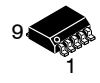
Device Order Number	Specific Device Marking	Package Type	Shipping†
NCP1618ADR2G	NCP1618A	SOIC−9 NB (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

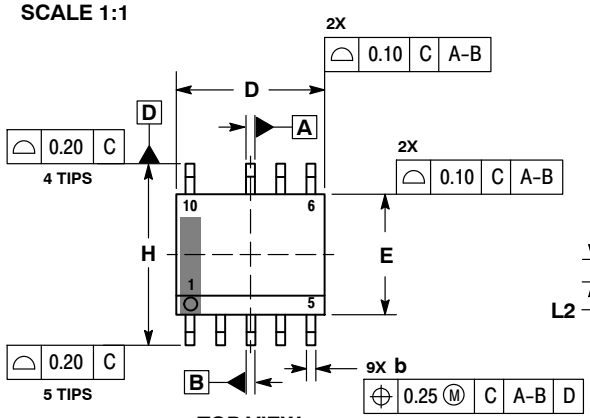
7. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

SOIC−9 NB
CASE 751BP
ISSUE A

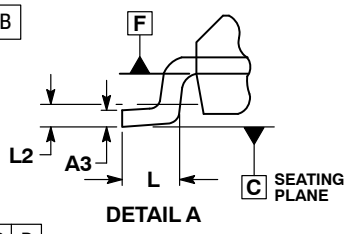
DATE 21 NOV 2011



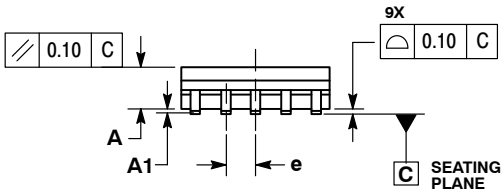
SCALE 1:1



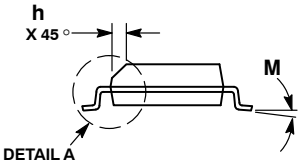
TOP VIEW



DETAIL A



SIDE VIEW

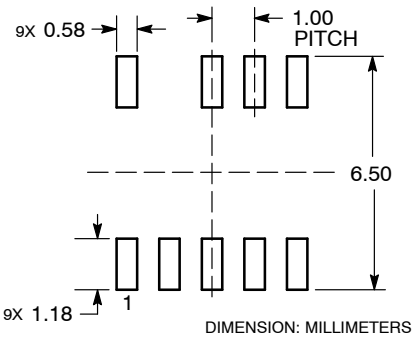


END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF 'b' AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	1.25	1.75
A1	0.10	0.25
A3	0.17	0.25
b	0.31	0.51
D	4.80	5.00
E	3.80	4.00
e	1.00 BSC	
H	5.80	6.20
h	0.37 REF	
L	0.40	1.27
L2	0.25 BSC	
M	0°	8°

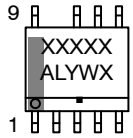
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G", may or not be present.

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