NCP1607

Cost Effective Power Factor Controller

The NCP1607 is an active power factor controller specifically designed for use as a pre−converter in ac−dc adapters, electronic ballasts, and other medium power off line converters (typically up to 250 W). It utilizes Critical Conduction Mode (CRM) to ensure unity power factor across a wide range of input voltages and power levels. The NCP1607 minimizes the number of external components. The integration of comprehensive safety protection features makes it an excellent choice for designing robust PFC stages. It is available in a SOIC−8 package.

General Features

- "Unity" Power Factor
- No Need for Input Voltage Sensing
- Latching PWM for Cycle by Cycle On Time Control (Voltage Mode)
- High Precision Voltage Reference (±1.6% over the Temperature Range)
- Very Low Startup Current Consumption (≤ 40 μA)
- Low Typical Operating Current (2.1 mA)
- Source 500 mA / Sink 800 mA Totem Pole Gate Driver
- Undervoltage Lockout with Hysteresis
- Pin to Pin Compatible with Industry Standards
- This is a Pb−Free Device
- This Device uses Halogen−Free Molding Compound

Safety Features

- Programmable Overvoltage Protection
- Open Feedback Loop Protection
- Accurate and Programmable On Time Control
- Accurate Overcurrent Detector

Typical Applications

- AC−DC Adapters, TVs, Monitors
- Off Line Appliances Requiring Power Factor Correction
- Electronic Light Ballast

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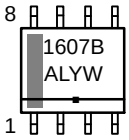
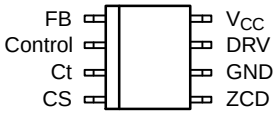
SO−8
D SUFFIX
CASE 751

MARKING DIAGRAMS



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN CONNECTION



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP1607BDR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

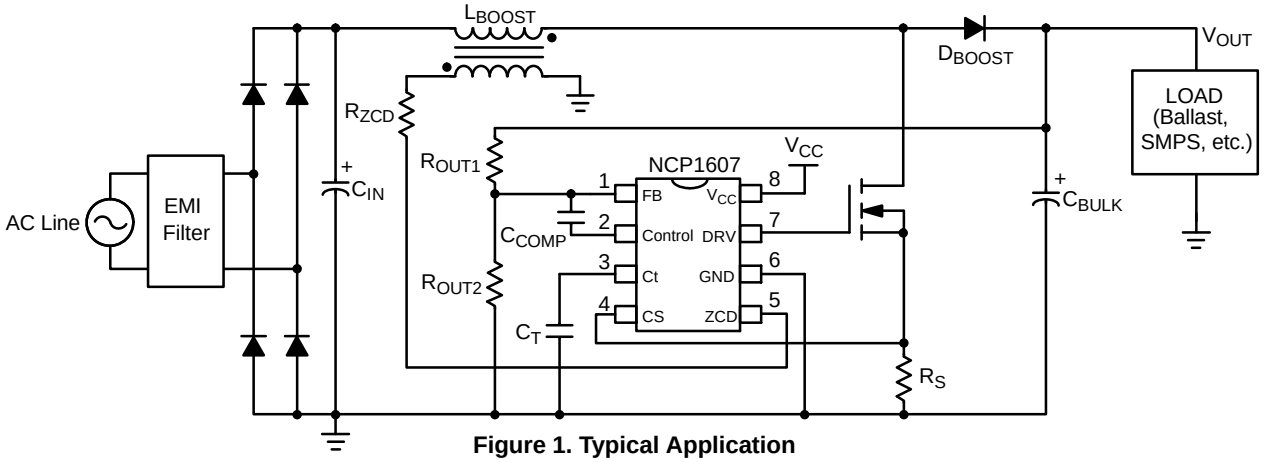


Figure 1. Typical Application

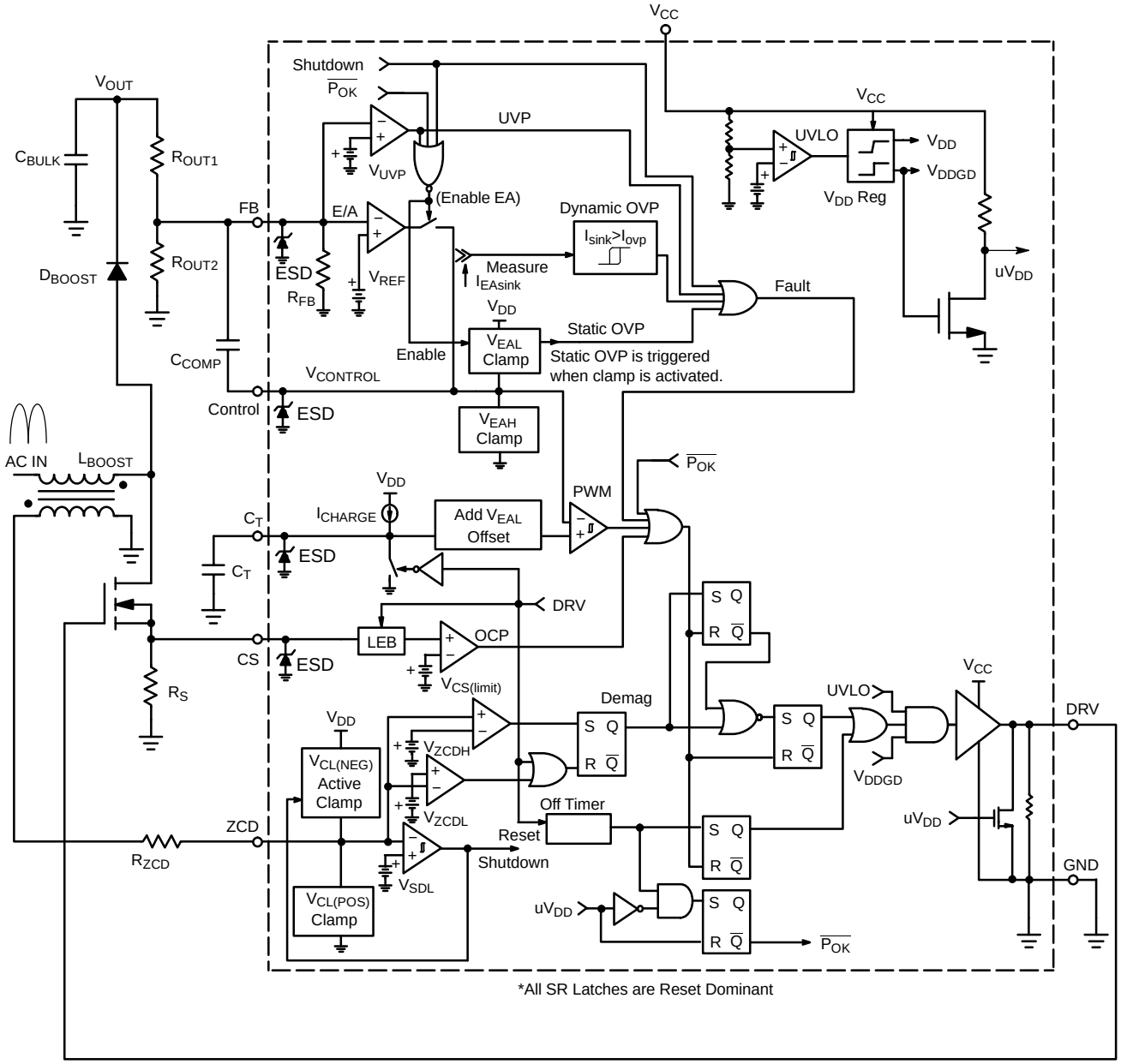


Figure 2. Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Name	Function
1	FB	The FB pin is the inverting input of the internal error amplifier. An external resistor divider scales the output voltage to the internal reference voltage to maintain regulation. The feedback information is also used for the programmable overvoltage and undervoltage protections. The controller is disabled when this pin is below the undervoltage protection threshold, V_{UVP}, typically 0.3 V.
2	Control	The Control pin is the output of the internal error amplifier. A compensation network is placed between the Control and FB pins to set the loop bandwidth. A low enough bandwidth is needed to obtain a high power factor ratio and a low THD.
3	Ct	The Ct pin sources a current to charge an external timing capacitor. The circuit controls the power switch on time by comparing the Ct voltage to an internal voltage derived from the regulation block. The Ct pin discharges the external timing capacitor at the end of the switching cycle.
4	CS	The CS pin limits the cycle−by−cycle current through the power switch. When the CS voltage exceeds the internal threshold, the MOSFET driver turns off. The sense resistor that connects to the CS pin programs the maximum switch current.
5	ZCD	The voltage of an auxiliary winding is applied to this pin to detect when the inductor is demagnetized for critical conduction mode operation. The controller is disabled when this pin is grounded.
6	GND	Analog ground.
7	DRV	Integrated MOSFET driver capable of driving a high gate charge power MOSFET.
8	V_{CC}	The V_{CC} pin is the positive supply of the controller. The controller is enabled when V_{CC} exceeds $V_{CC(on)}$ and remains enabled until V_{CC} decreases below $V_{CC(off)}$.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to 20	V
Supply Current	I_{CC}	±20	mA
DRV Voltage	V_{DRV}	−0.3 to 20	V
DRV Sink Current	$I_{DRV(sink)}$	800	mA
DRV Source Current	$I_{DRV(source)}$	500	mA
FB Voltage	V_{FB}	−0.3 to 10	V
FB Current	I_{FB}	±10	mA
Control Voltage	$V_{CONTROL}$	−0.3 to 10	V
Control Current	$I_{CONTROL}$	−2 to 10	mA
Ct Voltage	V_{Ct}	−0.3 to 6	V
Ct Current	I_{Ct}	±10	mA
CS Voltage	V_{CS}	−0.3 to 6	V
CS Current	I_{CS}	±10	mA
ZCD Voltage	V_{ZCD}	−0.3 to 10	V
ZCD Current	I_{ZCD}	±10	mA
Power Dissipation and Thermal Characteristics D suffix, Plastic Package, Case 751 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance Junction−to−Air	 P_D(SO) $R_{\theta JA}$(SO)	 450 178	 mW °C/W
Operating Junction Temperature Range	T_J	−40 to 125	°C
Maximum Junction Temperature	$T_{J(MAX)}$	150	°C
Storage Temperature Range	T_{STG}	−65 to 150	°C
Lead Temperature (Soldering, 10 s)	T_L	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Pins 1 − 8: Human Body Model 2000 V per JEDEC Standard JESD22−A114E,
   Charged Device Model 1000 V per JEDEC Standard JESD22−C101E.
2. This device contains latch−up protection and exceeds ±100 mA per JEDEC Standard JESD78.

ELECTRICAL CHARACTERISTICS

(For typical values, T_J = 25°C. For min/max values, T_J = −40°C to +125°C, unless otherwise specified, V_{CC} = 12 V, V_{FB} = 2.4 V, V_{CS} = 0 V, $V_{CONTROL}$ = open, V_{ZCD} = open, C_{DRV} = 1 nF, C_T = 1 nF)

Characteristics	Symbol	Min	Typ	Max	Unit
V_{CC} UNDERVOLTAGE LOCKOUT SECTION					
V_{CC} Startup Threshold (Undervoltage Lockout Threshold, Vcc rising) −25°C < T_J < +125°C −40°C < T_J < +125°C	$V_{CC(on)}$	 11.0 10.9	 11.8 11.8	 13.0 13.1	V
V_{CC} Disable Voltage after Turn On (Undervoltage Lockout Threshold, V_{CC} falling) −25°C < T_J < +125°C −40°C < T_J < +125°C	$V_{CC(off)}$	 8.7 8.5	 9.5 9.5	 10.3 10.5	V
Undervoltage Lockout Hysteresis	H_{UVLO}	2.2	2.5	2.8	V
DEVICE CONSUMPTION					
I_{CC} consumption during startup: 0 V < V_{CC} < $V_{CC(on)}$ − 200 mV	$I_{CC(startup)}$	−	23.5	40	μA
I_{CC} consumption after turn on at No Load, 70 kHz switching	I_{CC1}	−	1.4	2.0	mA
I_{CC} consumption after turn on at 70 kHz switching	I_{CC2}	−	2.17	3.0	mA
I_{CC} consumption after turn on at no switching (such as during OVP fault, UVP fault, or grounding ZCD)	$I_{CC(fault)}$	−	1.2	1.6	mA
REGULATION BLOCK (ERROR AMPLIFIER)					
Voltage Reference T_J = 25 °C −25°C < T_J < +125°C −40°C < T_J < +125°C	V_{REF}	 2.475 2.465 2.460	 2.50 2.50 2.50	 2.525 2.535 2.540	V
V_{REF} Line Regulation from $V_{CC(on)}$ + 200 mV < V_{CC} < 20 V, T_J = 25°C	V_{REF}(line)	−2.0	−	2.0	mV
Error Amplifier Current Capability: (Note 3) Sink ($V_{Control}$ = 4 V, V_{FB} = 2.6 V): Source ($V_{Control}$ = 4 V, V_{FB} = 2.4 V):	I_{EA}	 8.0 −2.0	 17 −6.0	 − −	mA
Error Amplifier Open Loop DC Gain (Note 4)	G_{OL}	−	80	−	dB
Unity Gain Bandwidth (Note 4)	BW	−	1.0	−	MHz
FB Bias Current (V_{FB} = 2.5 V)	I_{FB}	0.25	0.53	1.25	μA
FB Pull Down Resistor (V_{FB} = 2.5 V)	R_{FB}	2.0	4.7	10	MΩ
Control Pin Bias Current (FB = 0 V and $V_{CONTROL}$ = 4.0 V)	$I_{CONTROL}$	−1.0	−	1.0	μA
$V_{CONTROL}$ ($I_{EASOURCE}$ = 0.5 mA, V_{FB} = 2.4 V)	V_{EAH}	4.9	5.3	5.7	V
$V_{CONTROL}$ (I_{EASINK} = 0.5 mA, V_{FB} = 2.6 V)	V_{EAL}	1.85	2.1	2.4	V
$V_{EA(diff)}$ = V_{EAH} − V_{EAL}	$V_{EA(diff)}$	3.0	3.2	3.4	V
CURRENT SENSE BLOCK					
Overcurrent Voltage Threshold	$V_{CS(limit)}$	0.45	0.5	0.55	V
Leading Edge Blanking Duration	t_{LEB}	150	256	350	ns
Overcurrent Voltage Propagation Delay	t_{CS}	40	100	170	ns
CS Bias Current (V_{CS} = 2 V)	I_{CS}	−1.0	−	1.0	μA
ZERO CURRENT DETECTION					
Zero Current Detection Threshold (V_{ZCD} rising)	V_{ZCDH}	1.9	2.1	2.3	V
Zero Current Detection Threshold (V_{ZCD} falling)	V_{ZCDL}	1.45	1.6	1.75	V
V_{ZCDH} − V_{ZCDL}	$V_{ZCD(HYS)}$	300	500	800	mV
Maximum ZCD bias Current (V_{ZCD} = 5 V)	I_{ZCD}	−2.0	−	+2.0	μA
Upper Clamp Voltage (I_{ZCD} = 2.5 mA)	$V_{CL(POS)}$	5.0	5.7	6.5	V
Current Capability of the Positive Clamp at V_{ZCD} = $V_{CL(POS)}$ + 200 mV:	$I_{CL(POS)}$	5.0	8.5	−	mA
Negative Active Clamp Voltage (I_{ZCD} = −2.5 mA)	$V_{CL(NEG)}$	0.45	0.6	0.75	V

3. Parameter values are valid for transient conditions only.
4. Parameter characterized and guaranteed by design, but not tested in production.

ELECTRICAL CHARACTERISTICS

(For typical values, T_J = 25°C. For min/max values, T_J = −40°C to +125°C, unless otherwise specified, V_{CC} = 12 V, V_{FB} = 2.4 V, V_{CS} = 0 V, $V_{CONTROL}$ = open, V_{ZCD} = open, C_{DRV} = 1 nF, C_T = 1 nF)

Characteristics	Symbol	Min	Typ	Max	Unit
Current Capability of the Negative Active Clamp: in normal mode (V_{ZCD} = 300 mV) in shutdown mode (V_{ZCD} = 100 mV)	$I_{CL(NEG)}$	 2.5 35	 3.7 70	 5.0 100	 mA μA
Shutdown Threshold (V_{ZCD} falling)	V_{SDL}	150	205	250	mV
Enable Threshold (V_{ZCD} rising)	V_{SDH}	−	290	350	mV
Shutdown Comparator Hysteresis	$V_{SD(HYS)}$	−	85	−	mV
Zero Current Detection Propagation Delay	t_{ZCD}	−	100	170	ns
Minimum Detectable ZCD Pulse Width	t_{SYNC}	−	70	−	ns
Drive off Restart Timer	t_{START}	75	179	300	μs
RAMP CONTROL					
Ct Charge Current (V_{CT} = 0 V) −25°C < T_J < +125°C −40°C < T_J < +125°C	I_{CHARGE}	243 235	270 270	297 297	μA
Time to discharge a 1 nF Ct capacitor from V_{CT} = 3.4 V to 100 mV.	$t_{CT(discharge)}$	−	−	100	ns
Maximum Ct level before DRV switches off −25°C < T_J < +125°C −40°C < T_J < +125°C	V_{CTMAX}	2.9 2.9	3.2 3.2	3.3 3.4	V
PWM Propagation Delay	t_{PWM}	−	142	220	ns
OVER AND UNDERVOLTAGE PROTECTION					
Dynamic Overvoltage Protection (OVP) Triggering Current: T_J = 25°C T_J = −40°C to +125°C	I_{OVP}	 9.0 8.7	 10.5 −	 11.8 12.1	μA
Hysteresis of the dynamic OVP current before the OVP latch is released	$I_{OVP(HYS)}$	−	8.5	−	μA
Static OVP Threshold Voltage	V_{OVP}	−	V_{EAL} + 100 mV	−	V
Undervoltage Protection (UVP) Threshold Voltage	V_{UVP}	0.25	0.302	0.4	V
GATE DRIVE SECTION					
Gate Drive Resistance: R_{OH} @ I_{SOURCE} = 100 mA R_{OL} @ I_{SINK} = 100 mA	 R_{OH} R_{OL}	 − −	 12 6.0	 18 10	Ω
Drive voltage rise time from 10% V_{CC} to 90% V_{CC}	t_{rise}	−	30	80	ns
Drive voltage fall time from 90% V_{CC} to 10% V_{CC}	t_{fall}	−	25	70	ns
Driver output voltage at V_{CC} = $V_{CC(on)}$ − 200 mV and I_{sink} = 10 mA	$V_{OUT(start)}$	−	−	0.2	V

3. Parameter values are valid for transient conditions only.
4. Parameter characterized and guaranteed by design, but not tested in production.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

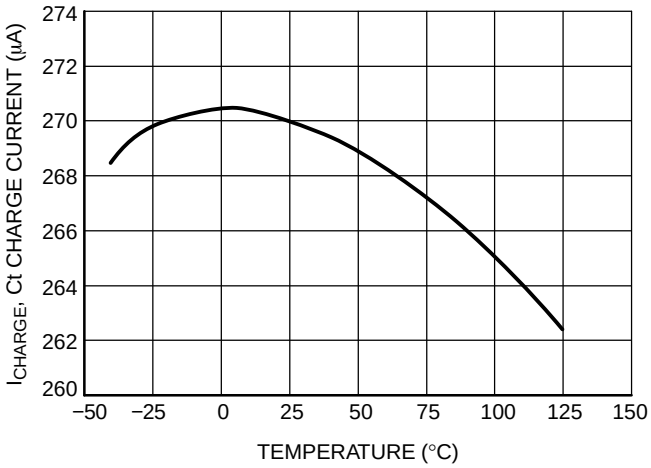


Figure 3. Ct Charge Current vs. Temperature

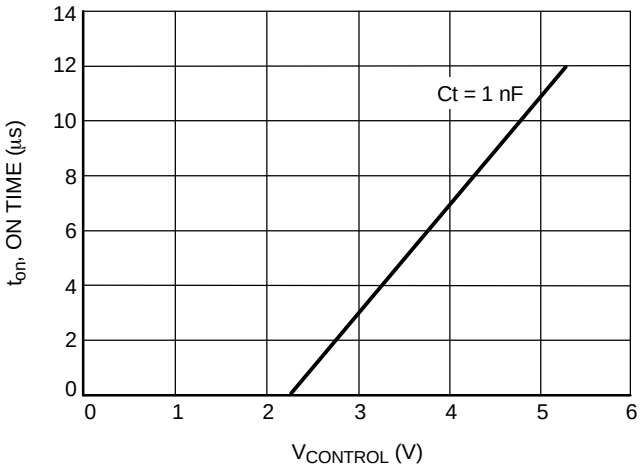


Figure 4. On Time vs. $V_{CONTROL}$ Level

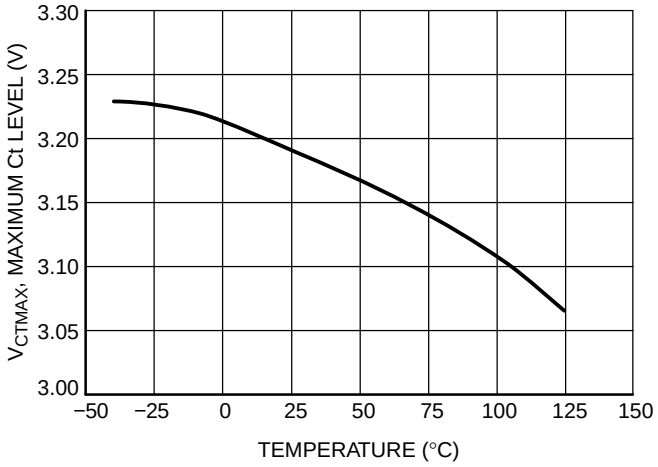


Figure 5. Maximum Ct Level vs. Temperature

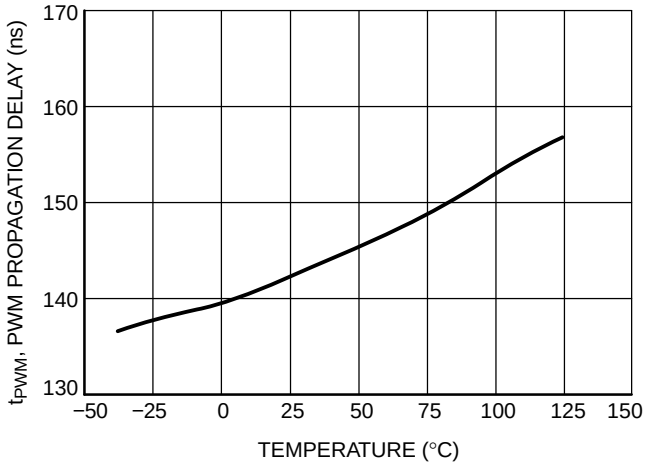


Figure 6. PWM Propagation Delay vs. Temperature

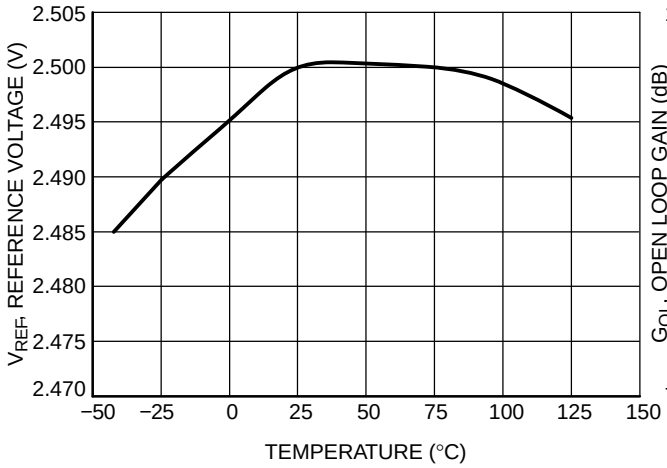


Figure 7. Reference Voltage vs. Temperature

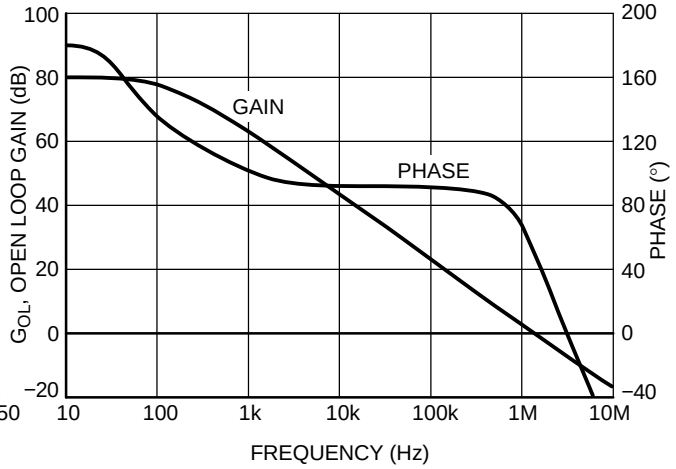


Figure 8. Error Amplifier Open Loop Gain and Phase

TYPICAL CHARACTERISTICS

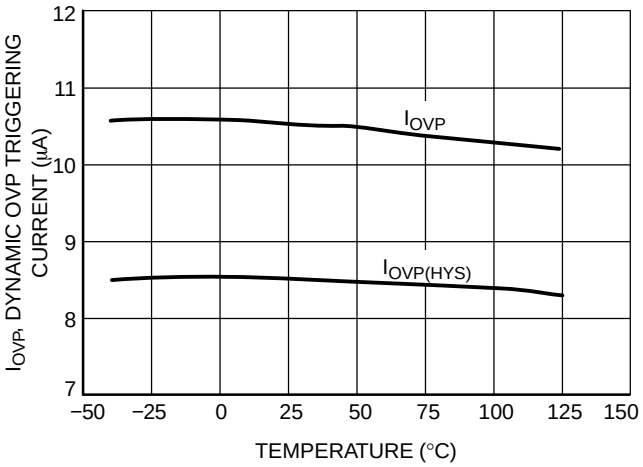


Figure 9. Dynamic OVP Triggering Current vs. Temperature

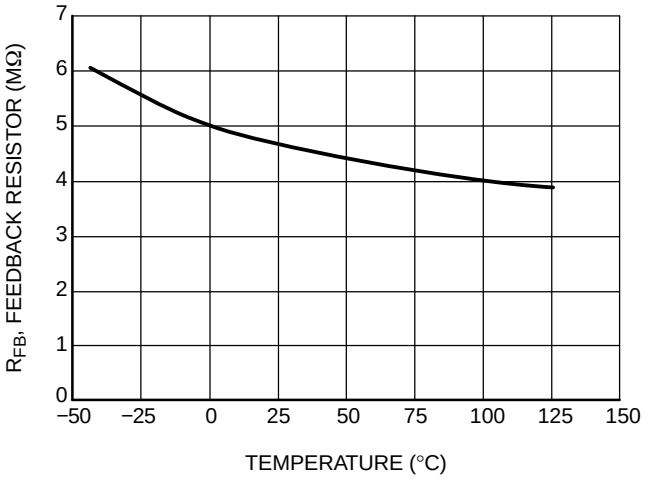


Figure 10. Feedback Resistor vs. Temperature

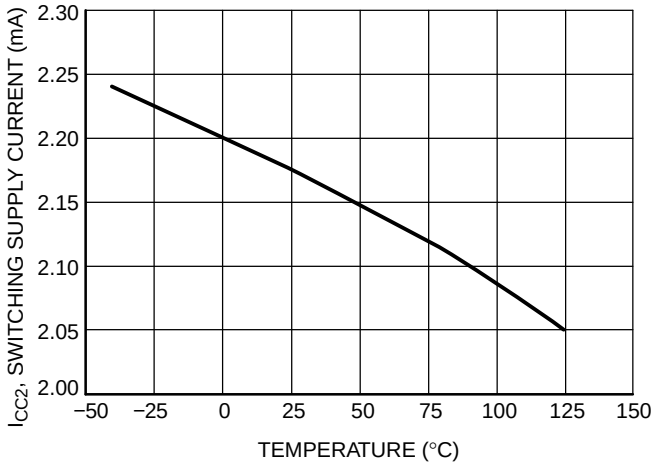


Figure 11. Switching Supply Current vs. Temperature

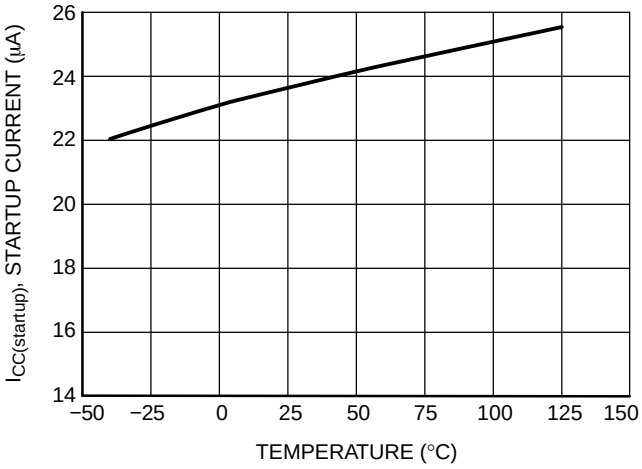


Figure 12. Startup Current vs. Temperature

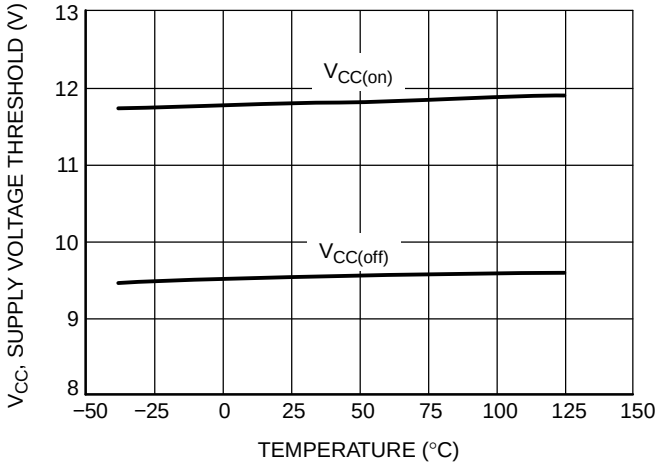


Figure 13. Supply Voltage Thresholds vs. Temperature

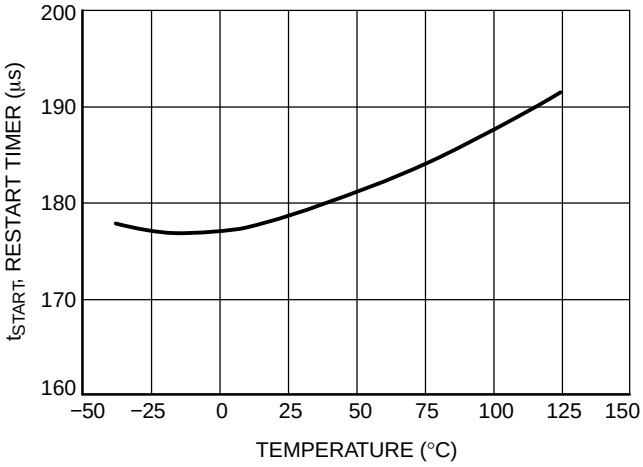


Figure 14. Restart Timer vs. Temperature

TYPICAL CHARACTERISTICS

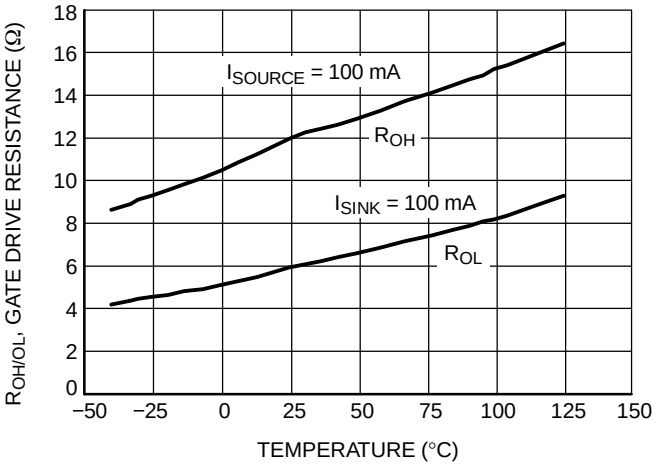


Figure 15. Gate Drive Resistance vs. Temperature

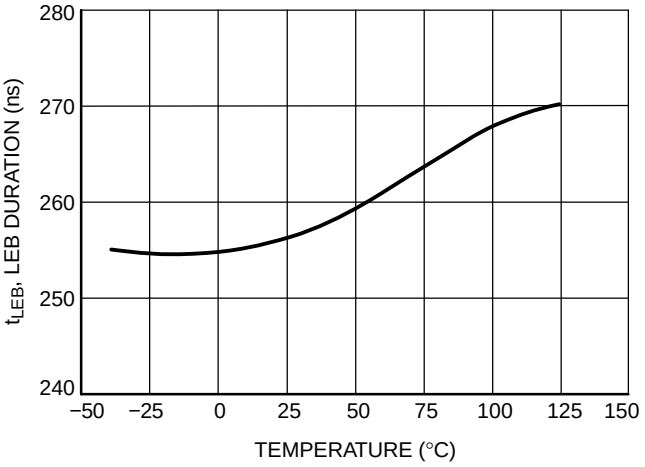


Figure 16. LEB Duration vs. Temperature

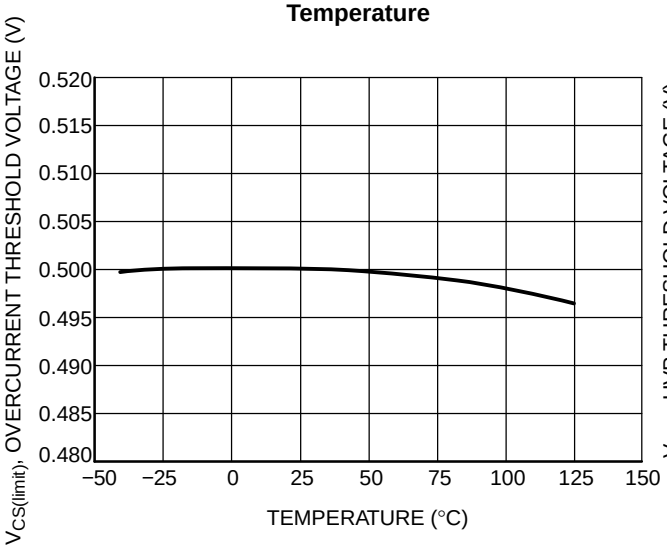


Figure 17. Overcurrent Threshold Voltage vs. Temperature

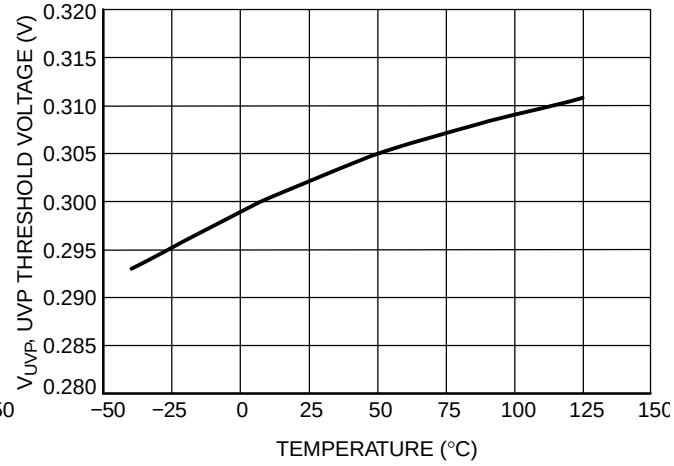


Figure 18. Undervoltage Protection Threshold Voltage vs. Temperature

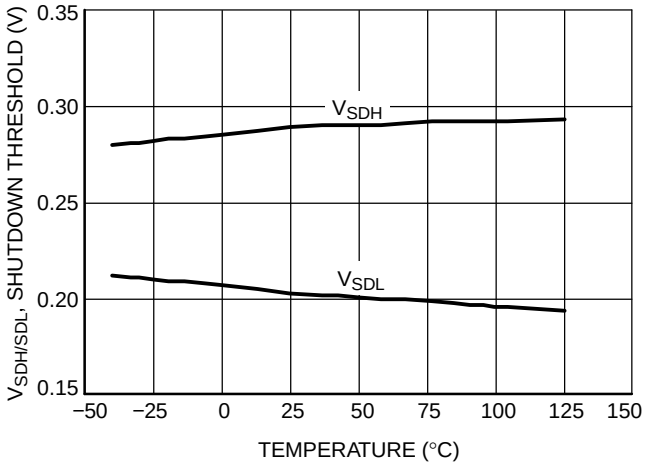


Figure 19. Shutdown Thresholds vs. Temperature

Introduction

The NCP1607 is a voltage mode power factor correction (PFC) controller designed to drive cost effective pre−converters to meet input line harmonic regulations. This controller operates in critical conduction mode (CRM) for optimal performance in applications up to 250 W. Its voltage mode scheme enables it to obtain unity power factor without the need for a line sensing network. The output voltage is accurately controlled by a high precision error amplifier. The controller also implements a comprehensive array of safety features for robust designs. The key features of the NCP1607 are as follows:

- Constant on time (Voltage Mode) CRM operation. High power factor ratios are easily obtained without the need for input voltage sensing. This allows for optimal standby power consumption.
- Accurate and Programmable On Time Limitation. The NCP1607 uses an accurate current source and an external capacitor to generate the on time.
- High Precision Voltage Reference. The error amplifier reference voltage is guaranteed at 2.5 V ±1.6% over process, temperature, and voltage supply levels. This results in very accurate output voltages.
- Very Low Startup Current Consumption. The circuit consumption is reduced to a minimum (< 40 μA) during the startup phase, allowing fast, low loss, charging of V_{CC}. The architecture of the NCP1607 gives a controlled undervoltage lockout level and provides ample V_{CC} hysteresis during startup.
- Powerful Output Driver. A Source 500 mA / Sink 800 mA totem pole gate driver is used to provide rapid turn on and turn off times. This allows for improved efficiencies and the ability to drive higher power MOSFETs. Additionally, a combination of active and passive circuitry is used to ensure that the driver output voltage does not float high while V_{CC} is below its turn on level.
- Programmable Overvoltage Protection (OVP). The adjustable OVP feature protects the PFC stage against excessive output overshoots that could damage the application. These events can typically occur during the startup phase or when the load is abruptly removed.
- Protection against Open Feedback Loop (Undervoltage Protection). Undervoltage protection (UVP) disables the PFC stage when the output voltage is excessively low. This also protects the circuit in case of a failure in the feedback network: if no voltage is applied to FB because of a poor connection or if the FB pin is floating, UVP is activated shutting down the converter.
- Overcurrent Limitation. The peak current is accurately limited on a pulse by pulse basis. The level is adjustable by modifying the current sense resistor. An integrated LEB filter reduces the chance of noise prematurely triggering the overcurrent limit.
- Shutdown Features. The PFC pre−converter is placed in a shutdown mode by grounding the FB pin or the ZCD pin. During this mode, the I_{CC} current consumption is reduced and the error amplifier is disabled.

Application information

Most electronic ballasts and switching power supplies use a diode bridge rectifier and a bulk storage capacitor to produce a dc voltage from the utility ac line (Figure 20). This DC voltage is then processed by additional circuitry to drive the desired output.

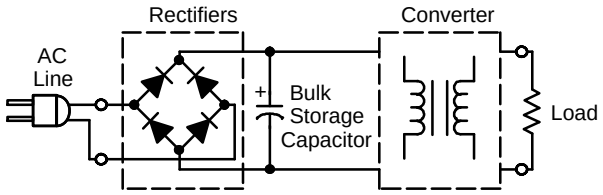


Figure 20. Typical Circuit without PFC

This simple rectifying circuit draws power from the line when the instantaneous ac voltage exceeds the capacitor voltage. Since this occurs near the line voltage peak, the resulting current draw is non sinusoidal and contains a very high harmonic content. This results in a poor power factor (typically < 0.6) and consequently, the apparent input power is much higher than the real power delivered to the load. Additionally, if multiple devices are tied to the same input line, the effect is magnified and a “line sag” effect can be produced (see Figure 21).

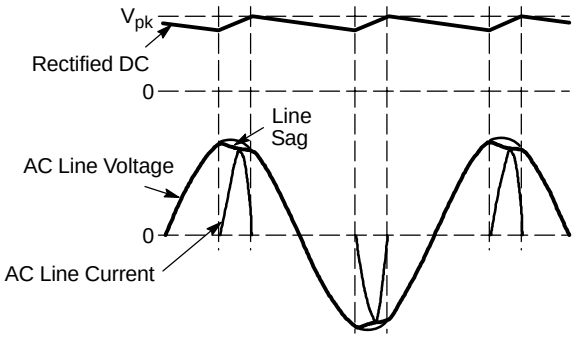


Figure 21. Typical Line Waveforms without PFC

Increasingly, government regulations and utility requirements necessitate control over the line current harmonic content. To meet this need, power factor correction is implemented with either a passive or active circuit. Passive circuits usually contain a combination of large capacitors, inductors, and rectifiers that operate at the ac line frequency. Active circuits incorporate some form of a high frequency switching converter that regulates the

input current to stay in phase with the input voltage. These circuits operate at a higher frequency and so they are smaller, lighter in weight, and more efficient than a passive circuit. With proper control of an active PFC stage, almost any complex load can be made to appear in phase with the ac line, thus significantly reducing the harmonic current content. Because of these advantages, active PFC circuits have become the most popular way to meet harmonic content requirements. Generally, they consist of inserting a PFC pre−regulator between the rectifier bridge and the bulk capacitor (Figure 22).

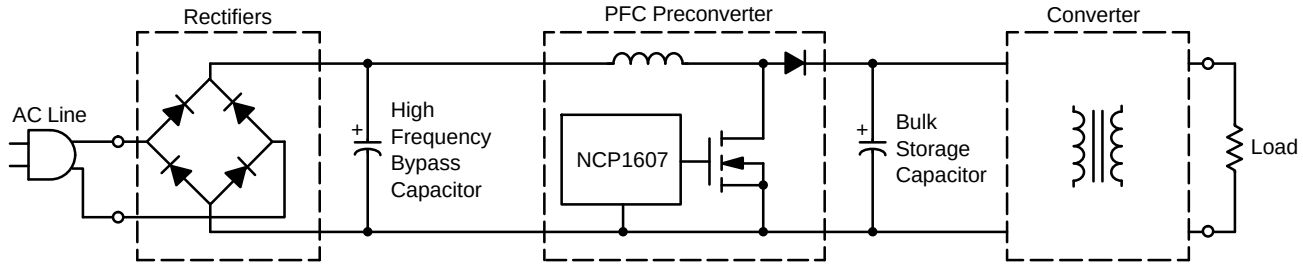


Figure 22. Active PFC Pre−Converter with the NCP1607

The boost (or step up) converter is the most popular topology for active power factor correction. With the proper control, it produces a constant voltage while drawing a sinusoidal current from the line. For medium power (<300 W) applications, critical conduction mode (also called borderline conduction mode) is the preferred control method. Critical conduction mode (CRM) occurs at the boundary between discontinuous conduction mode (DCM) and continuous conduction mode (CCM). In CRM, the next driver on time is initiated when the boost inductor current reaches zero. CRM operation is an ideal choice for medium power PFC boost stages because it combines the lower peak currents of CCM operation with the zero current switching of DCM operation. The operation and waveforms in a PFC boost converter are illustrated in Figure 23.

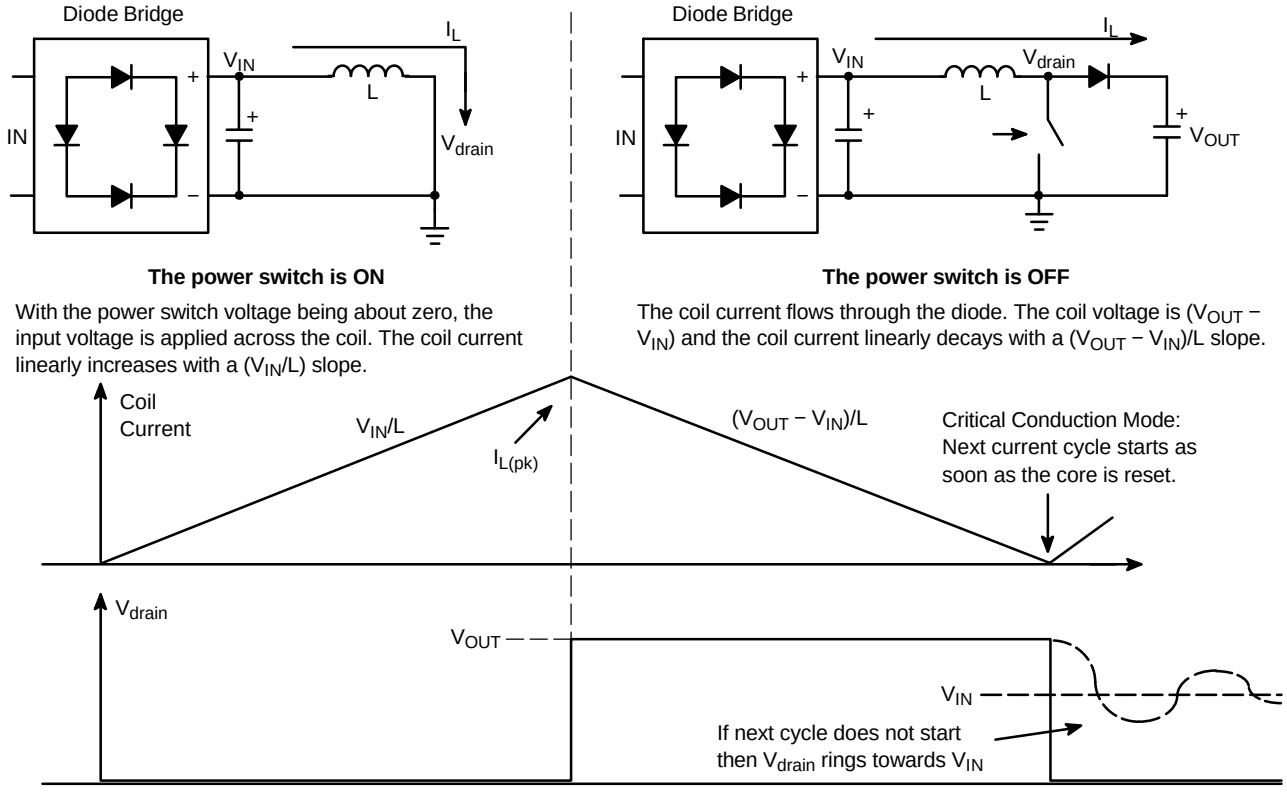


Figure 23. Schematic and Waveforms of an Ideal CRM Boost Converter

When the switch is closed, the inductor current increases linearly to its peak value. When the switch opens, the inductor current linearly decreases to zero. At this point, the drain voltage of the switch (V_d) is essentially floating and begins to drop. If the next switching cycle does not start, then the voltage will ring with a dampened frequency around V_{in}. A simple derivation of equations (such as found in AND8123), leads to the result that good power factor correction in CRM operation is achieved when the on time is constant across an ac cycle and is equal to:

$$t_{on} = \frac{2 \cdot P_{OUT} \cdot L}{\eta \cdot Vac^2} \qquad \text{(eq. 1)}$$

A simple plot of this switching over an ac line cycle is illustrated in Figure 24. The off time varies based on the instantaneous line voltage, but the on time is kept constant. This naturally causes the peak inductor current ($I_{L(pk)}$) to follow the ac line voltage.

The NCP1607 represents an ideal method to implement this constant on time CRM control in a cost effective and robust solution. The device incorporates an accurate regulation circuit, a low power startup circuit, and advanced protection features.

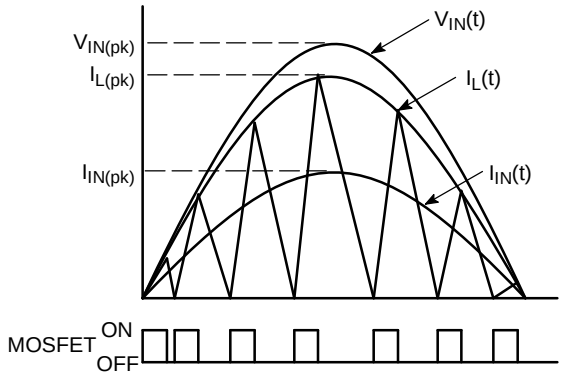


Figure 24. Inductor Waveform During CRM Operation

ERROR AMPLIFIER REGULATION

The NCP1607 is configured to regulate the boost output voltage based on its built in error amplifier (EA). The error amplifier's negative terminal is pinned out to FB, the positive terminal is tied to a 2.5 V ± 1.6% reference, and the output is pinned out to Control (Figure 25).

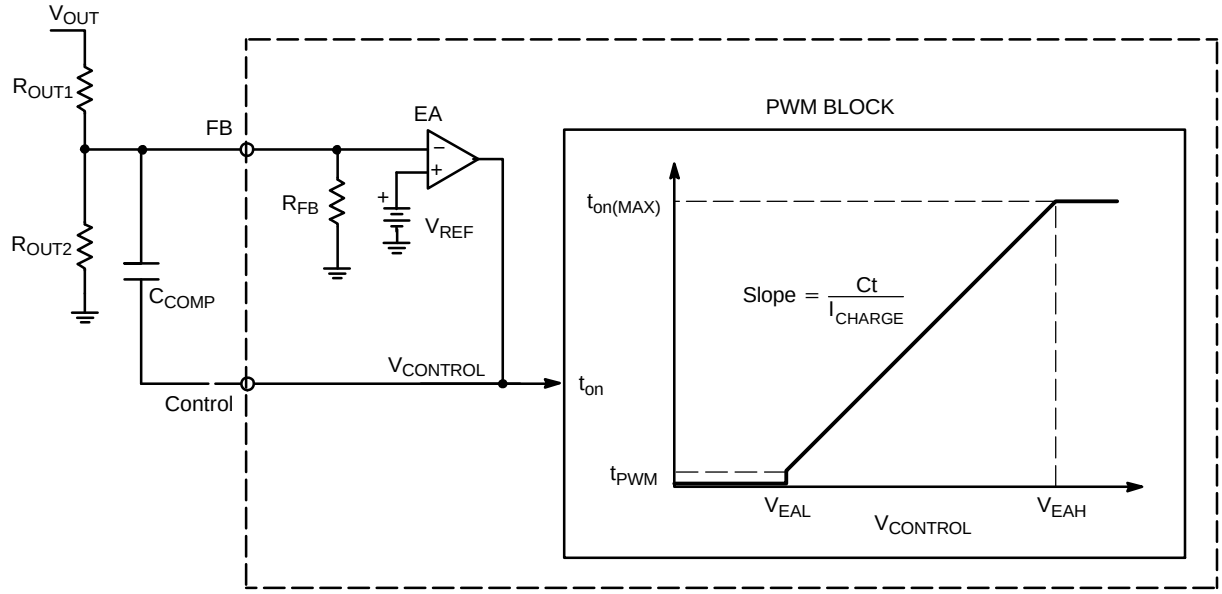


Figure 25. Error Amplifier and On Time Regulation Circuits

A resistor divider from the boost output to the input of the EA sets the FB level. If the output voltage is too low, then the FB level will drop and the EA will cause the control voltage to increase. This increases the on time of the driver, which increases the power delivered and brings the output back into regulation. Alternatively, if the output voltage (and hence FB voltage) is too high, then the control level decreases and the driver on times are shortened. In this way, the circuit regulates the output voltage (V_{OUT}) so that the V_{OUT} portion that is applied to FB through the resistor divider R_{OUT1} and R_{OUT2} is equal to the internal reference (2.5 V). The output voltage is set using Equation 2:

$$V_{OUT} = V_{REF} \cdot \left(\frac{R_{OUT1} + R_{EQ}}{R_{EQ}} \right) \qquad \text{(eq. 2)}$$

Where R_{EQ} is the parallel combination of R_{OUT2} and R_{FB}. R_{EQ} is calculated using Equation 3:

$$R_{EQ} = \frac{R_{OUT2} \cdot R_{FB}}{R_{OUT2} + R_{FB}} \qquad \text{(eq. 3)}$$

A compensation network is placed between the FB and Control pins to reduce the speed at which the EA responds to changes in the boost output. This is necessary due to the nature of an active PFC circuit. The PFC stage absorbs a sinusoidal current from a sinusoidal line voltage. Hence, the converter provides the load with a power that matches the average demand only. Therefore, the output capacitor must “absorb” the difference between the delivered power and the power consumed by the load. This means that when the power fed to the load is lower than the demand, the output capacitor discharges to compensate for the lack of power. Alternatively, when the supplied power is higher than that absorbed by the load, the output capacitor charges to store the excess energy. The situation is depicted in Figure 26.

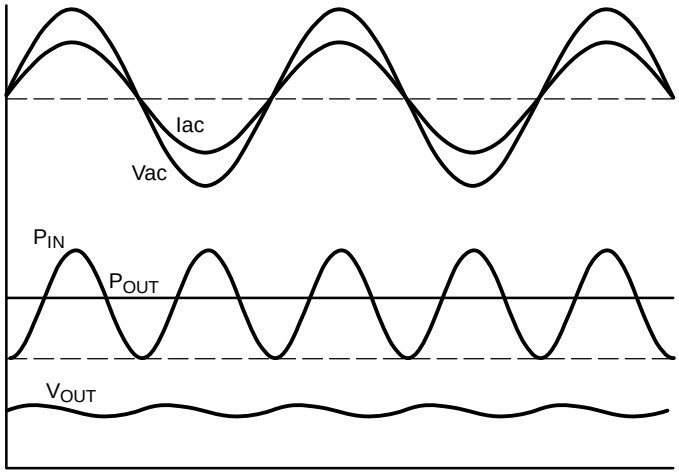


Figure 26. Output Voltage Ripple for a Constant Output Power

As a consequence, the output voltage exhibits a ripple at a frequency of either 100 Hz (for 50 Hz mains such as in Europe) or 120 Hz (for 60 Hz mains in the USA). This ripple must not be taken into account by the regulation loop because the error amplifier’s output voltage must be kept constant over a given ac line cycle for a proper shaping of the line current. Due to this constraint, the regulation bandwidth is typically set below 20 Hz. For a simple type 1 compensation network, only a capacitor is placed between FB and Control (see Figure 1). In this configuration, the capacitor necessary to attenuate the bulk voltage ripple is given by:

$$C_{COMP} = \frac{10^{\frac{G}{20}}}{4 \cdot \pi f_{line} \cdot R_{OUT1}} \qquad \text{(eq. 4)}$$

where G is the attenuation level in dB (commonly 60 dB)

ON TIME SEQUENCE

Since the NCP1607 is designed to control a CRM boost converter, its switching pattern must accommodate constant on times and variable off times. The Controller generates the on time via an external capacitor connected to pin 3 (Ct). A current source charges this capacitor to a level determined by the Control pin voltage. Specifically, Ct is charged to $V_{CONTROL}$ minus the V_{EAL} offset (2.1 V typical). Once this level is exceeded, the drive is turned off (Figure 27).

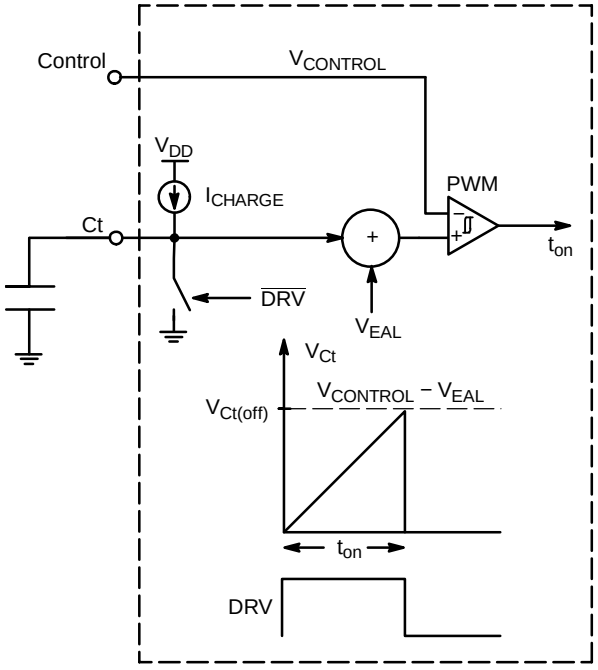


Figure 27. On Time Generation

Since $V_{CONTROL}$ varies with the RMS line level and output load, this naturally satisfies equation 1. And if the values of compensation components are sufficient to filter

out the bulk voltage ripple, then this on time is truly constant over the ac line cycle.

Note that the maximum on time of the controller occurs when $V_{CONTROL}$ is at its maximum. Therefore, the Ct capacitor must be sized to ensure that the required on time can be delivered at full power and the lowest input voltage condition. The maximum on time is given by:

$$t_{on(MAX)} = \frac{Ct \cdot V_{CTMAX}}{I_{CHARGE}} \quad \text{(eq. 5)}$$

Combining this equation with equation 1, gives:

$$Ct \geq \frac{2 \cdot P_{OUT} \cdot L \cdot I_{CHARGE}}{\eta \cdot Vac^2 \cdot V_{CTMAX}} \quad \text{(eq. 6)}$$

where V_{CTMAX} = 2.9 V (min)
I_{CHARGE} = 297 μA (max)

OFF TIME SEQUENCE

While the on time is constant across the ac cycle, the off time in CRM operation varies with the instantaneous input voltage. The NCP1607 determines the correct off time by sensing the inductor voltage. When the inductor current drops to zero, the drain voltage ("V_{drain}" in Figure 23) is essentially floating and naturally begins to drop. If the switch is turned on at this moment, then CRM operation will be achieved. To measure this high voltage directly on the inductor is generally not economical or practical. Rather, a smaller winding is taken off of the boost inductor. This winding, called the zero current detector (ZCD) winding, gives a scaled version of the inductor output and is more useful to the controller.

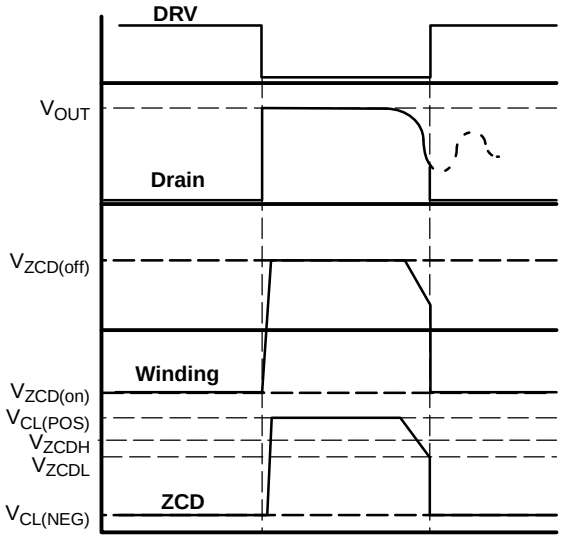


Figure 28. Voltage Waveforms for Zero Current Detection

Figure 28 gives typical operating waveforms with the ZCD winding. When the drive is on, a negative voltage appears on the ZCD winding. And when the drive is off, a positive voltage appears. When the inductor current drops to zero, then the ZCD voltage falls and starts to ring around zero volts. The NCP1607 detects this falling edge and starts the next driver on time. To ensure that a ZCD event has truly occurred, the NCP1607's logic (Figure 29) waits for the ZCD pin voltage to rise above V_{ZCDH} (2.1 V typical) and then fall below V_{ZCDL} (1.6 V typical). In this way, CRM operation is easily achieved.

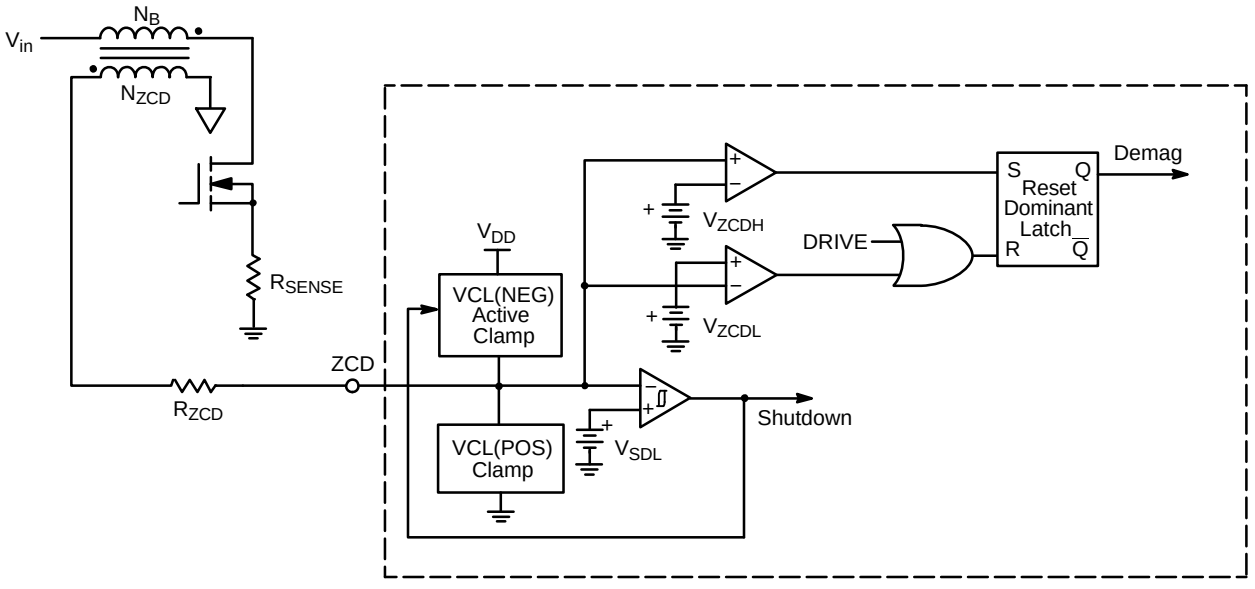


Figure 29. Implementation of the ZCD Winding

To prevent negative voltages on the ZCD pin, the pin is internally clamped to $V_{CL(NEG)}$ (600 mV typical) when the ZCD winding is negative. Similarly, the ZCD pin is clamped to $V_{CL(POS)}$ (5.7 V typical), when the voltage rises too high. Because of these clamps, a resistor (R_{ZCD} in Figure 29) is necessary to limit the current from the ZCD winding to the ZCD pin.

At startup, there is no energy in the ZCD winding and therefore no voltage signal to activate the ZCD comparators. This means that the driver could never turn on. Therefore, to enable the PFC stage to startup under these conditions, an internal watchdog timer is integrated into the controller. This timer turns the drive on if the driver has been off for more than 180 μs (typical). This feature is deactivated during a fault mode (OVP, UVP, or Shutdown), and reactivated when the fault is removed.

STARTUP

Generally, a resistor connected between the ac input and V_{CC} (pin 8) charges the V_{CC} capacitor to the $V_{CC(on)}$ level (12 V typical). Because of the very low consumption of the NCP1607 during this stage (< 40 μA), most of the current goes directly to charging up the V_{CC} capacitor. This provides faster startup times and reduced standby power dissipation. When the V_{CC} voltage exceeds the $V_{CC(on)}$ level, the internal references and logic of the NCP1607 turn on. The controller has an undervoltage lockout (UVLO) feature which keeps the part active until V_{CC} drops below $V_{CC(off)}$ (9.5 V typical). This hysteresis allows ample time for the auxiliary winding to take over and supply the necessary power to V_{CC} (Figure 30).

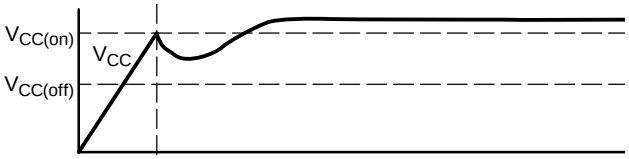


Figure 30. Typical V_{CC} Startup Waveform

When the PFC pre−converter is loaded by a switch mode power supply (SMPS), then it is often preferable to have the SMPS controller startup first. The SMPS can then supply the NCP1607 V_{CC} directly. Advanced controllers, such as the NCP1230 or NCP1381, can control when to turn on the PFC stage (see Figure 31) leading to optimal system performance. This setup also eliminates the startup resistors and therefore improves the no load power dissipation of the system.

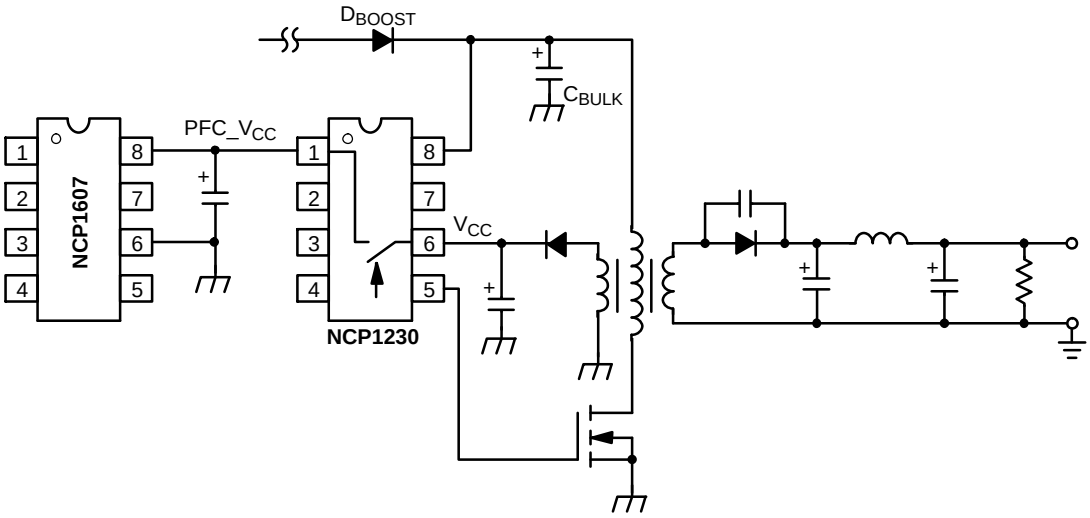


Figure 31. NCP1607 Supplied by a Downstream SMPS Controller (NCP1230)

QUICK START and SOFT START

At startup, the error amplifier is enabled and Control is pulled up to V_{EAL} (2.1 V typical). This is the lowest level of control voltage which produces output drives. This feature, called “quick start,” eliminates the delay at startup associated with charging the compensation network to its minimum level. This also produces a natural “soft−start” mode where the controller’s power ramps up from zero to the required power (see Figure 32).

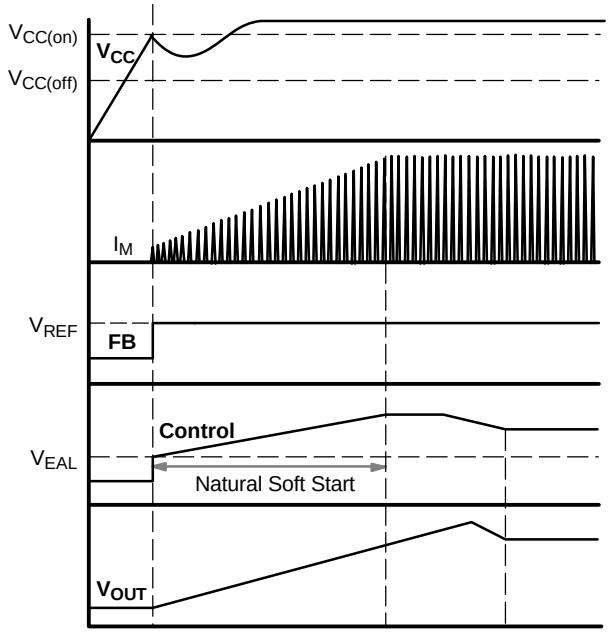


Figure 32. Startup Timing Diagram Showing the Natural Soft Start of the Control Pin

OUTPUT DRIVER

The NCP1607 includes a powerful output driver capable of peak currents of Source 500 mA / Sink 800 mA. This enables the controller to efficiently drive power MOSFETs for medium power (up to 300 W) applications. Additionally, the driver stage is equipped with both passive and active pull down clamps (Figure 33). The clamps are active when V_{CC} is off and force the driver output to well below the threshold voltage of a power MOSFET.

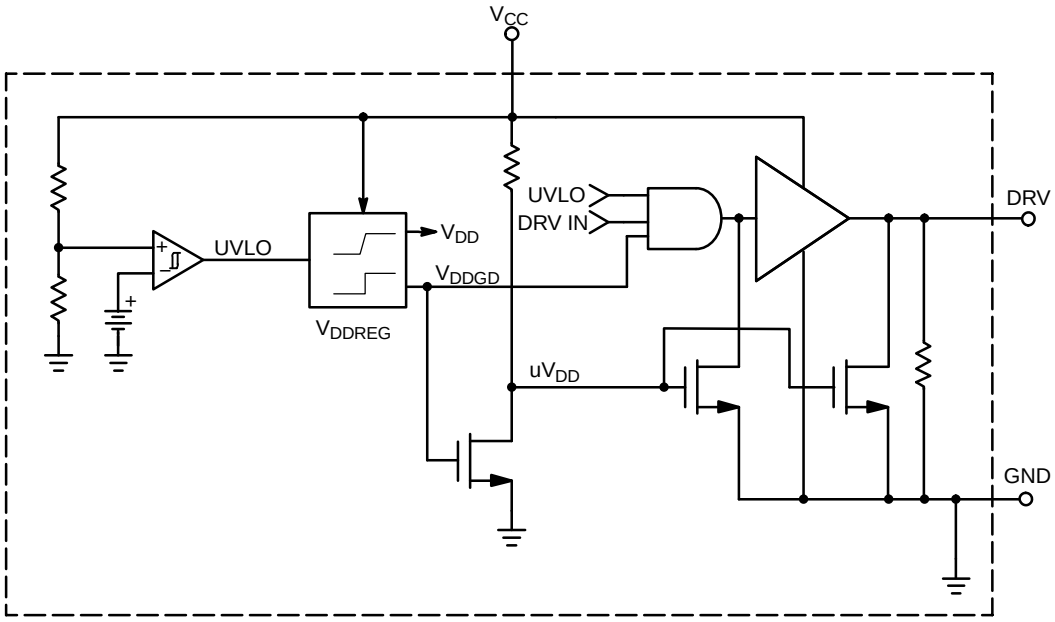


Figure 33. Output Driver Stage and Pull Down Clamps

Overvoltage Protection

The low bandwidth of the feedback network makes active PFC stages very slow systems. One consequence of this is the risk of huge overshoots in abrupt transient phases (startup, load steps, etc.). For reliable operation, it is critical that some form of overvoltage protection (OVP) effectively prevents the output voltage from rising too high. The NCP1607 detects these excessive V_{OUT} levels and disables the driver until the output voltage returns to nominal levels. This keeps the output voltage within an acceptable range. The limit is adjustable so that the overvoltage level can be optimally set. The level must not be so low that it is triggered by the 100 or 120 Hz ripple of the output voltage, but it must be low enough so as not to require a larger voltage rating of the output capacitor. Figure 34 depicts the operation of the OVP circuitry.

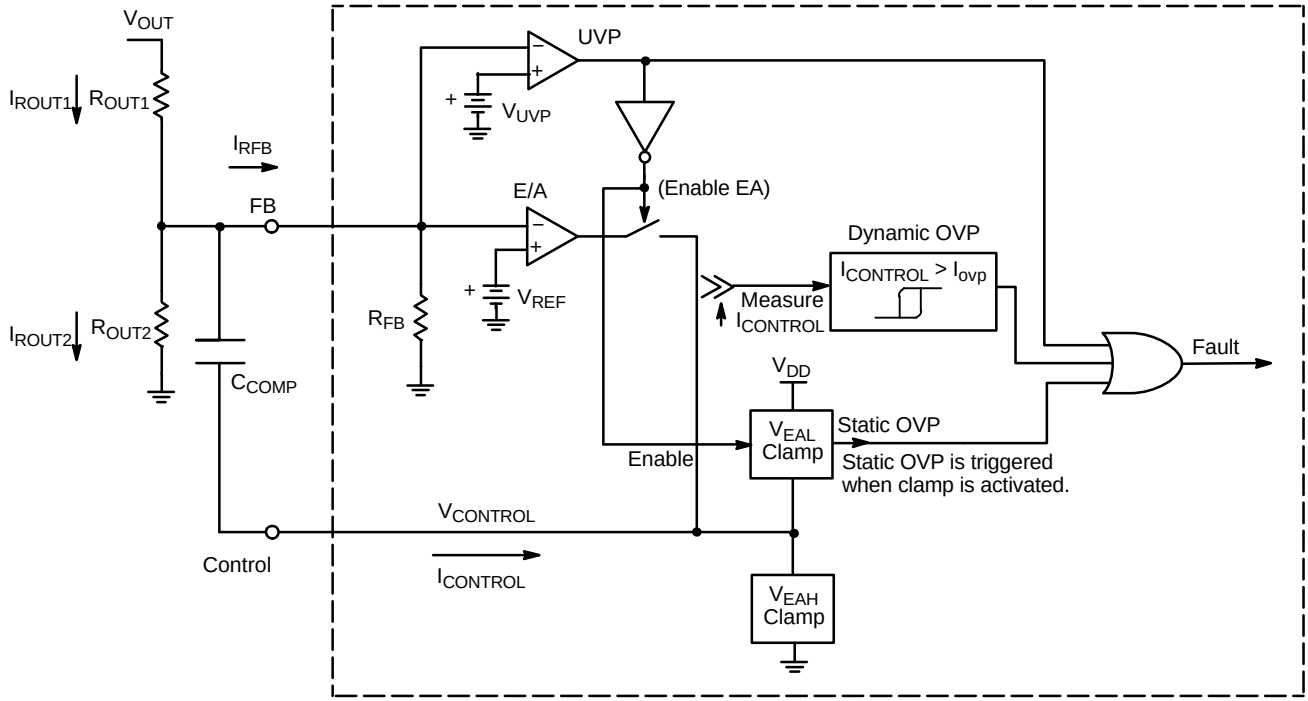


Figure 34. OVP and UVP Circuit Blocks

When the output voltage is in steady state equilibrium, R_{OUT1} and R_{OUT2} regulate the FB voltage to V_{REF}. During this equilibrium state, no current flows through the compensation capacitor (C_{COMP} shown in Figure 34). These facts allow the following equations to be derived:

- The R_{OUT1} current is:

$$I_{ROUT1} = \frac{V_{OUT} - V_{REF}}{R_{OUT1}} \quad \text{(eq. 7)}$$

- The R_{EQ} current is:

$$I_{EQ} = \frac{V_{REF}}{R_{EQ}} = I_{ROUT2} + I_{FB} \quad \text{(eq. 8)}$$

- And since no current flows through C_{COMP},

$$I_{ROUT1} = \frac{V_{OUT} - V_{REF}}{R_{OUT1}} - \frac{V_{REF}}{R_{EQ}} \quad \text{(eq. 9)}$$

Under stable conditions, Equations 7 through 9 are true. Conversely, when V_{OUT} is not at the target voltage, the output of the error amplifier sinks or sources the current necessary to maintain V_{REF} on pin 1.

In the case of an overvoltage condition:

- The error amplifier maintains V_{REF} on pin 1, and the R_{EQ} current remains the same as the steady state value:

$$I_{EQ} = \frac{V_{REF}}{R_{EQ}} \quad \text{(eq. 10)}$$

- The R_{OUT1} current is increased and is calculated using Equation 11:

$$I_{ROUT1} = \frac{V_{OUT(OVP)} - V_{REF}}{R_{OUT1}} = \frac{V_{OUT} + \Delta V_{OUT} - V_{REF}}{R_{OUT1}} \quad \text{(eq. 11)}$$

where ΔV_{OUT} is the output voltage excess.

- The error amplifier sinks:

$$I_{Control} = I_{ROUT1} - I_{EQ} = \frac{V_{OUT} + \Delta V_{OUT} - V_{REF}}{R_{OUT1}} - \frac{V_{REF}}{R_{EQ}} \quad \text{(eq. 12)}$$

The combination of Equations 2 and 12 yield a simple expression of the current sunk by the error amplifier:

$$I_{CONTROL} = \frac{\Delta V_{OUT}}{R_{OUT1}}$$

The current absorbed by pin 2 ($I_{Control}$) is proportional to the output voltage excess. The circuit senses this current and disables the drive (pin 7) when $I_{Control}$ exceeds I_{OVP} (10.4 μA typical). The OVP threshold is calculated using Equation 13.

$$V_{OUT(OVP)} = V_{OUT} + R_{OUT1} \cdot I_{OVP} \quad \text{(eq. 13)}$$

The OVP limit is set by adjusting R_{OUT1}. R_{OUT1} is calculated using Equation 14.

$$R_{OUT1} = \frac{V_{OUT(OVP)} - V_{OUT}}{I_{OVP}} \quad \text{(eq. 14)}$$

For example, if 440 V is the maximum output voltage and 400 V is the target output voltage, then R_{OUT1} is calculated using Equation 14.

$$R_{OUT1} = \frac{440 - 400}{10.4\mu} = 3.846\ \text{M}\Omega$$

If R_{OUT1} is selected as 4 MΩ, then $V_{OUT(OVP)}$ = 442 V.

STATIC OVERVOLTAGE PROTECTION

If the OVP condition lasts for a long time, it may happen that the error amplifier output reaches its minimum level (i.e. Control = V_{EAL}). It would then not be able to sink any current and maintain the OVP fault. Therefore, to avoid any discontinuity in the OVP disabling effect, the circuit incorporates a comparator which detects when the lower level of the error amplifier is reached. This event, called "static OVP", disables the output drives. Once the OVP event is over, and the output voltage has dropped to normal, then Control rises above the lower limit and the driver is re−enabled (Figure 35).

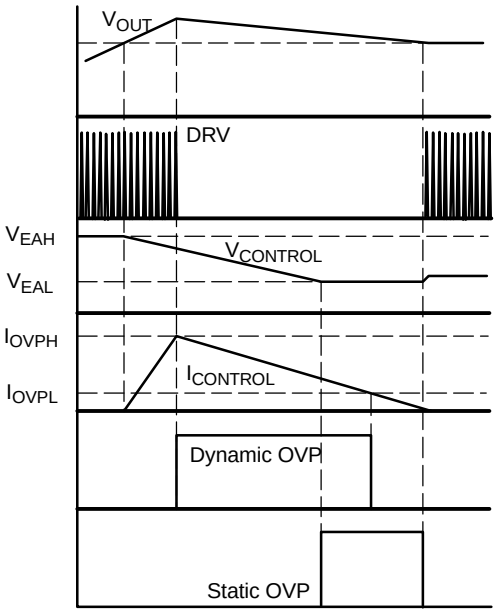


Figure 35. OVP Timing Diagram

NCP1607 Undervoltage Protection (UVP)

When the PFC stage is plugged in, the output voltage is forced to roughly equate the peak line voltage. The NCP1607 detects an undervoltage fault when this output voltage is unusually low, such that the feedback voltage is below V_{UVP} (300 mV typical). In an UVP fault, the drive output and error amplifier (EA) are disabled. The latter is done so that the EA does not source a current which would increase the FB voltage and prevent the UVP event from being accurately detected. The UVP feature helps to protect the application if something is wrong with the power path to the bulk capacitor (i.e. the capacitor cannot charge up) or if the controller cannot sense the bulk voltage (i.e. the feedback loop is open).

Furthermore, the NCP1607 incorporates a novel startup sequence which ensures that undervoltage conditions are always detected at startup. It accomplishes this by waiting approximately 180 μs after V_{CC} reaches $V_{CC(on)}$ before enabling the error amplifier (Figure 36). During this wait time, it looks to see if the feedback (FB) voltage is greater than the UVP threshold. If not, then the controller enters a UVP fault and leaves the error amplifier disabled. However, if the FB pin voltage increases and exceeds the UVP level, then the controller will start the application up normally.

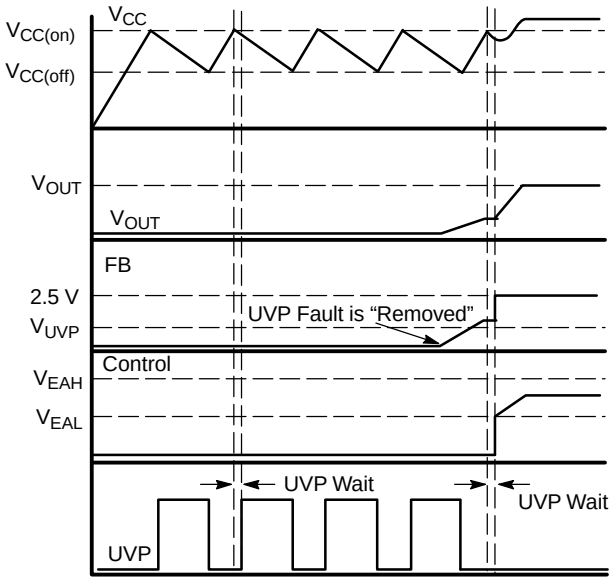


Figure 36. The NCP1607's Startup Sequence with and without a UVP Fault

The voltage on the output which exits a UVP fault is given by:

$$V_{OUT(UVP)} = \frac{R_{OUT1} + R_{EQ}}{R_{EQ}} \cdot V_{UVP} \qquad \text{(eq. 15)}$$

If R_{OUT1} = 4 MΩ and R_{EQ} = 25.16 kΩ, then the V_{OUT} UVP threshold is 48 V. This corresponds to an input voltage of approximately 34 Vac.

Open Feedback Loop Protection

The NCP1607 features comprehensive protection against open feedback loop conditions by including OVP, UVP, and Floating Pin Protection (FPP). Figure 37 illustrates three conditions in which the feedback loop is open. The corresponding number below describes each condition shown in Figure 37.

1. **UVP Protection:** The connection from resistor R_{OUT1} to the FB pin is open. R_{OUT2} pulls down the FB pin to ground. The UVP comparator detects a UVP fault and the drive is disabled.
2. **OVP Protection:** The connection from resistor R_{OUT2} to the FB pin is open. R_{OUT1} pulls up the FB pin to the output voltage. The ESD diode clamps the FB voltage to 10 V and R_{OUT1} limits the current into the FB pin. The V_{EAL} clamp detects a static OVP fault and the drive is disabled.
3. **FPP Protection:** The FB pin is floating. The internal pulldown resistor R_{FB} pulls down the FB voltage below the UVP threshold. The UVP comparator detects a UVP fault and the drive is disabled.

UVP and OVP protect the system from low bulk voltages and rapid operating point changes respectively, while the FPP protects the system against floating feedback pin conditions. If FPP is not implemented and a manufacturing error causes the feedback pin to float, then the feedback voltage is dependent on the coupling within the system and the surrounding environment. The coupled feedback voltage may be within the regulation limits (i.e. above the UVP threshold, but below V_{REF}) and cause the controller to deliver excessive power. The result is that the output voltage rises until a component fails due to the voltage stress.

The tradeoff for including FPP is that the value of R_{FB} causes an error in the output voltage. The output voltage including the error caused by R_{FB} ($\overline{V_{OUT}}$) is calculated using Equation 16:

$$\overline{V_{OUT}} = V_{OUT} + R_{OUT1} \cdot \frac{V_{REF}}{R_{FB}} \qquad \text{(eq. 16)}$$

Using the values from the OVP calculation, the output voltage including the error caused by R_{FB} is equal to:

$$\overline{V_{OUT}} = 400 + 4\ M \cdot \frac{2.5}{4.7\ M} = 402\ V$$

The error caused by R_{FB} is compensated by adjusting R_{OUT2}. The parallel combination of R_{FB} and R_{OUT2} form an equivalent resistor R_{EQ} that is calculated using Equation 17.

$$R_{EQ} = R_{OUT1} \cdot \frac{V_{REF}}{V_{OUT} - V_{REF}} \qquad \text{(eq. 17)}$$

$$R_{EQ} = 4\ M \cdot \frac{2.5}{400 - 2.5} = 25.16\ k\Omega$$

R_{EQ} is used to calculate R_{OUT2}.

$$R_{OUT2} = \frac{R_{EQ} \cdot R_{FB}}{R_{FB} - R_{EQ}} \qquad \text{(eq. 18)}$$

$$R_{OUT2} = \frac{25.16\ k \cdot 4.7\ M}{4.7\ M - 25.16\ k} = 25.29\ k\Omega$$

The compensated output voltage is calculated using Equation 19.

$$V_{OUT} = V_{REF} \cdot \left(\frac{R_{OUT1} + R_{OUT2}}{R_{OUT2}}\right) + R_{OUT1} \cdot \frac{V_{REF}}{R_{FB}} \qquad \text{(eq. 19)}$$

$$V_{OUT} = 2.5 \cdot \left(\frac{4\ M + 25.29\ k}{25.29\ k}\right) + 4\ M \cdot \frac{2.5}{4.7\ M} = 400\ V$$

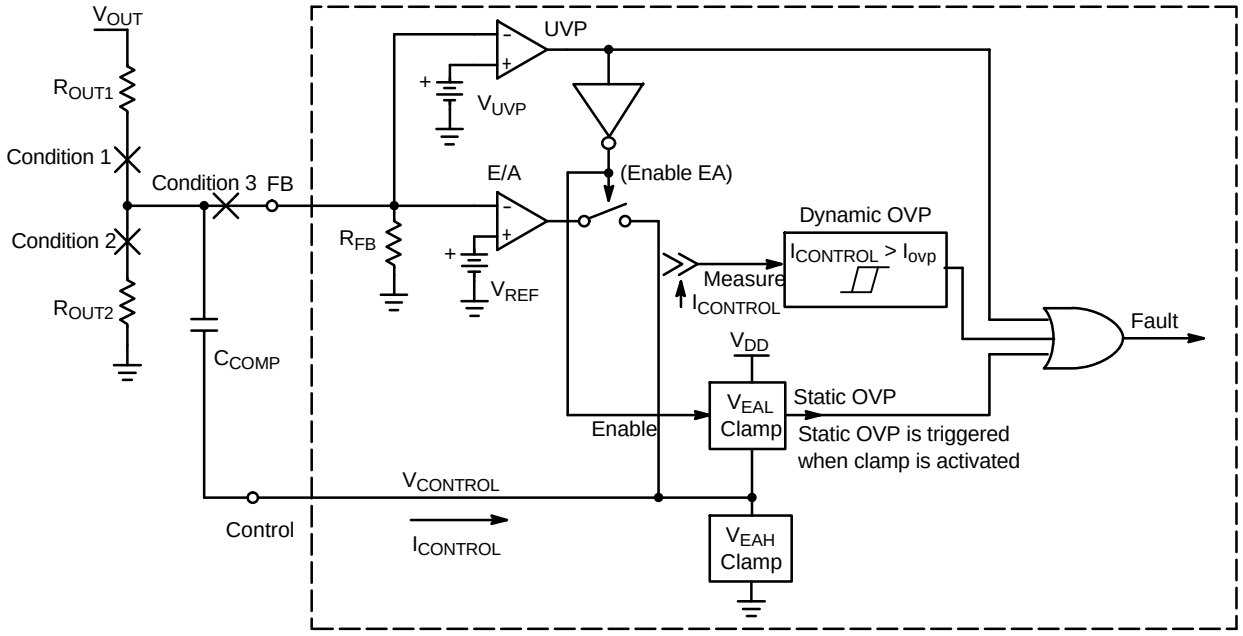


Figure 37. Open Feedback Loop Protection

Overcurrent Protection (OCP)

A dedicated pin on the NCP1607 senses the peak current and limits the driver on time if this current exceeds $V_{CS(limit)}$. This level is 0.5 V (typical). Therefore, the maximum peak current can be adjusted by changing R_{SENSE} according to:

$$I_{peak} = \frac{V_{CS(limit)}}{R_S} \qquad \text{(eq. 20)}$$

An internal LEB filter (Figure 38) reduces the likelihood of switching noise falsely triggering the OCP limit. This filter blanks out the first 250 ns (typical) of the current sense signal. If additional filtering is necessary, a small RC filter can be added between R_{SENSE} and the CS pin.

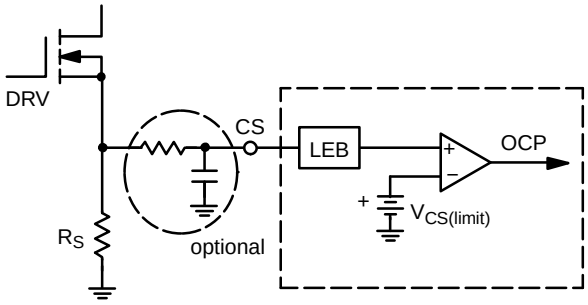


Figure 38. OCP Circuitry with Optional External RC Filter

SHUTDOWN MODE

The NCP1607 allows for two methods to place the controller into a standby mode of operation. The FB pin can be pulled below the UVP level (300 mV typical) or the ZCD pin can be pulled below the V_{SDL} level (200 mV typical). If the FB pin is used for shutdown (Figure 39(a)), care must be taken to ensure that no significant leakage current exists on the shutdown circuitry. This could impact the output voltage regulation. If the ZCD pin is used for shutdown (Figure 39(b)), then any parasitic capacitance created by the shutdown circuitry will add to the delay in detecting the zero inductor current event.

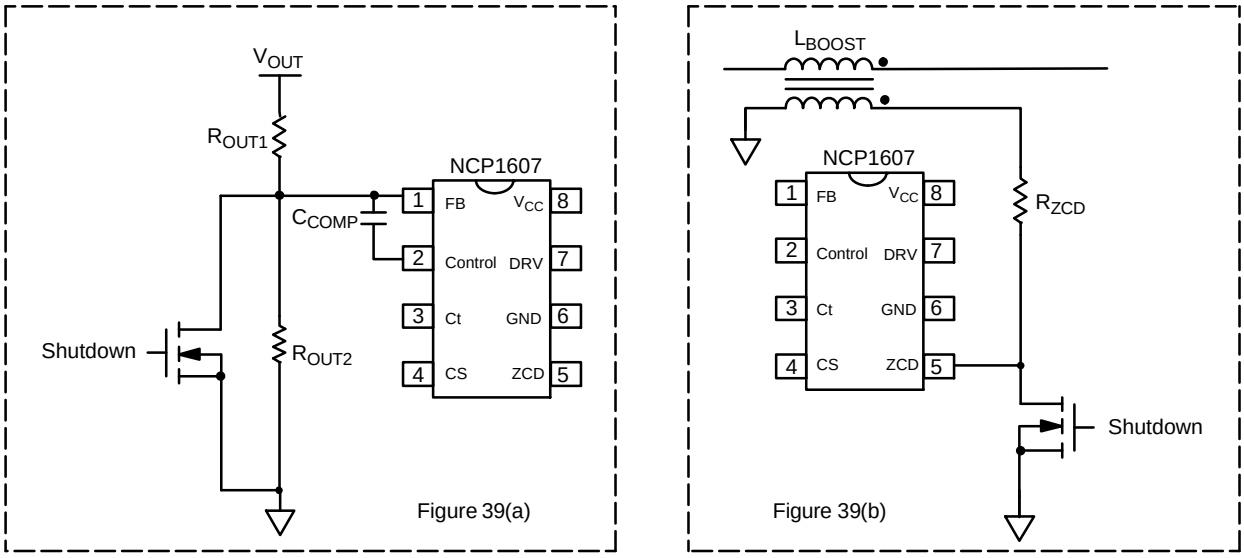


Figure 39. Shutting Down the PFC Stage by Pulling FB to GND (A) or Pulling ZCD to GND (B)

To activate the shutdown feature on ZCD, the internal clamp must first be overcome. This clamp will draw a maximum of $I_{CL(NEG)}$ (5.0 mA maximum) before releasing and allowing the ZCD pin voltage to drop low enough to shutdown the part (Figure 40). After shutdown, the comparator includes approximately 90 mV of hysteresis to ensure noise free operation. A small current source (70 μA typical) is also activated to pull the unit out of the shutdown condition when the external pull down is released.

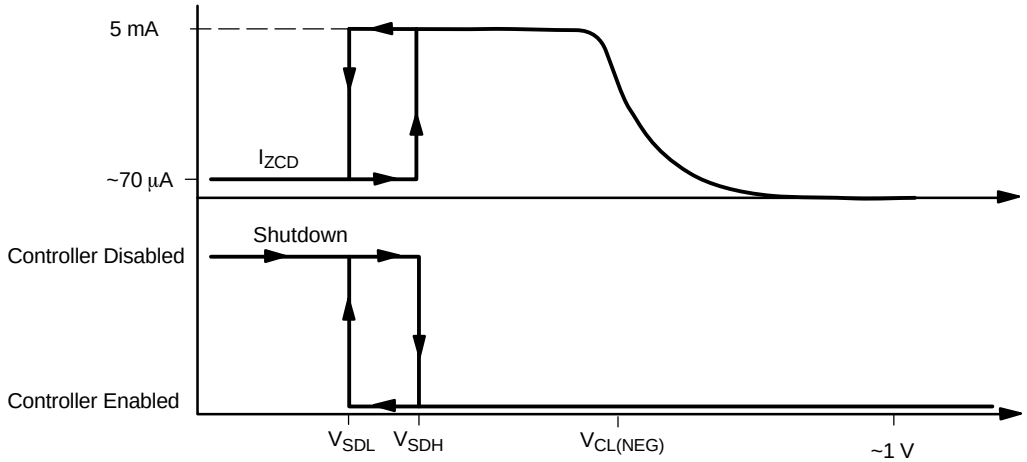


Figure 40. Shutdown Comparator and Current Draw to Overcome Negative Clamp

Application Information

ON Semiconductor provides an electronic design tool, a demonstration board and an application note to facilitate the design of the NCP1607 and reduce development cycle time. All the tools can be downloaded or ordered at *www.onsemi.com*.

The electronic design tool allows the user to easily determine most of the system parameters of a boost pre−converter. The demonstration board is a boost pre−converter that delivers 100 W at 400 V. The circuit schematic is shown in Figure 41. The pre−converter design is described in Application Note AND8353/D.

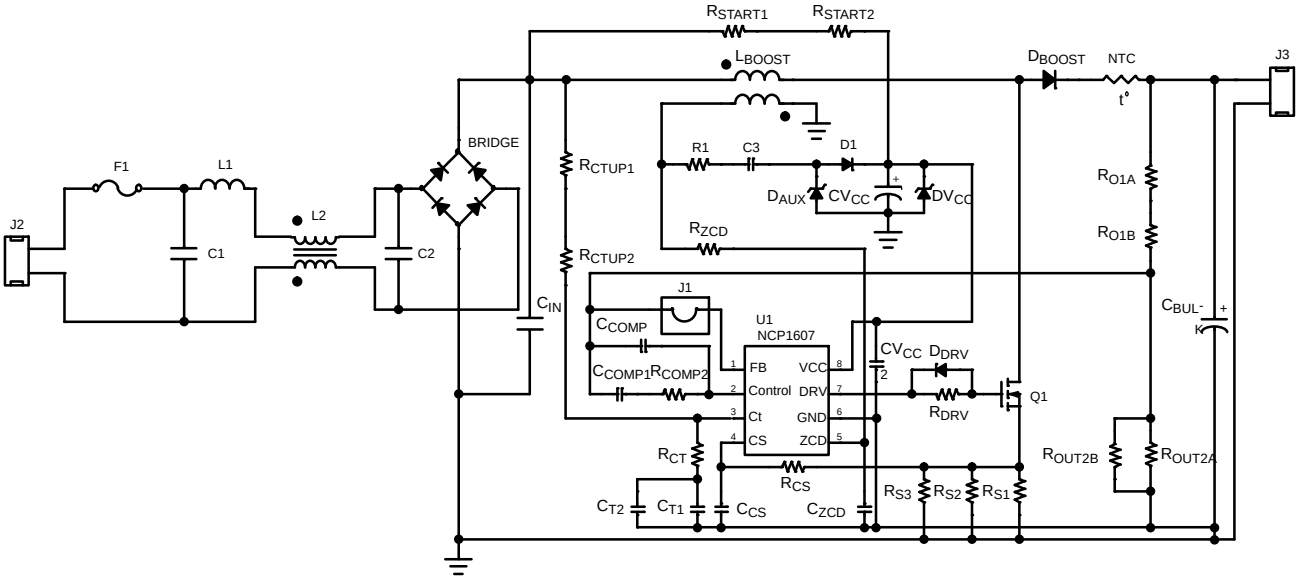


Figure 41. Application Board Circuit Schematic

BOOST DESIGN EQUATIONS Components are identified in Figure 1

RMS Input Current	$Iac = \frac{P_{OUT}}{\eta \cdot Vac}$	η (the efficiency of only the Boost PFC stage) is generally in the range of 90 − 95%
Maximum Inductor Peak Current	$I_{pk(MAX)} = \frac{2 \cdot \sqrt{2} \cdot P_{OUT}}{\eta \cdot Vac_{LL}}$	Where Vac_{LL} is the minimum line input voltage. $I_{pk(MAX)}$ occurs at the lowest line voltage.
Inductor Value	$L \le \frac{2 \cdot Vac^2 \cdot \left(\frac{V_{OUT}}{\sqrt{2}} - Vac\right)}{V_{OUT} \cdot Vac \cdot I_{pk(MAX)} \cdot f_{SW(min)}}$	$f_{SW(MIN)}$ is the minimum desired switching frequency. The maximum L must be calculated at low line and high line.
Maximum On Time	$t_{on(MAX)} = \frac{2 \cdot L \cdot P_{OUT}}{\eta \cdot Vac_{LL}^{\ 2}}$	The maximum on time occurs at the lowest line voltage and maximum output power.
Off Time	$t_{off} = \frac{t_{on}}{\frac{V_{OUT}}{Vac \cdot \lvert\sin(\theta)\rvert \cdot \sqrt{2}} - 1}$	The off time is greatest at the peak of the ac line voltage and approaches zero at the ac line zero crossings. Theta (θ) represents the angle of the ac line voltage.
Frequency	$f_{SW} = \frac{Vac^2 \cdot \eta}{2 \cdot L \cdot P_{OUT}} \cdot \left(1 - \frac{Vac \cdot \lvert\sin\theta\rvert \cdot \sqrt{2}}{V_{OUT}}\right)$	
Pin 3 Capacitor	$Ct \ge \frac{2 \cdot P_{OUT} \cdot L \cdot I_{CHARGE}}{\eta \cdot Vac^2 \cdot V_{CTMAX}}$	I_{CHARGE} and V_{CTMAX} are given in the NCP1607 specification table.
Boost Turns to ZCD Turns Ratio	$N_B : N_{ZCD} \le \frac{V_{OUT} - Vac_{HL} \cdot \sqrt{2}}{V_{ZCDH}}$	Where Vac_{HL} is the maximum line input voltage. The turns ratio must be low enough so as to trigger the ZCD comparators at high line.
Resistor from ZCD winding to the ZCD pin (pin 5)	$R_{ZCD} \ge \frac{Vac_{HL} \cdot \sqrt{2}}{I_{CL(NEG)} \cdot (N_B : N_{ZCD})}$	R_{ZCD} must be large enough so that the shutdown comparator is not inadvertently activated.
Boost Output Voltage	$V_{OUT} = V_{REF} \cdot \frac{R_{OUT1} + R_{EQ}}{R_{EQ}}$ $R_{EQ} = \frac{R_{OUT2} \cdot R_{FB}}{R_{OUT2} + R_{FB}}$	
Maximum V_{OUT} voltage prior to OVP activation and the necessary R_{OUT1} and R_{OUT2}.	$V_{OUT(OVP)} = V_{OUT} + \left(I_{OVP} \cdot R_{OUT1}\right)$ $R_{OUT1} = \frac{V_{OUT(OVP)} - V_{OUT}}{I_{OVP}}$ $R_{EQ} = R_{OUT1} \cdot \frac{V_{REF}}{V_{OUT} - V_{REF}}$ $R_{OUT2} = \frac{R_{EQ} + R_{FB}}{R_{FB} - R_{EQ}}$	I_{OVP} is given in the NCP1607 specification table.
Minimum output voltage necessary to exit undervoltage protection (UVP)	$V_{OUT(UVP)} = V_{UVP} \cdot \frac{R_{OUT1} + R_{EQ}}{R_{EQ}}$	V_{UVP} is given in the NCP1607 specification table.
Bulk Cap Ripple	$V_{ripple(pk-pk)} = \frac{P_{OUT}}{C_{BULK} \cdot 2 \cdot \pi \cdot f_{line} \cdot V_{OUT}}$	Use f_{line} = 47 Hz for worst case at universal lines. The ripple must not exceed the OVP level for V_{OUT}.
Inductor RMS Current	$I_{L(RMS)} = \frac{2 \cdot P_{OUT}}{\sqrt{3} \cdot Vac_{LL} \cdot \eta}$	
Boost Diode RMS Current	$I_{D(RMS)MAX} = \frac{4}{3} \cdot \sqrt{\frac{2 \cdot \sqrt{2}}{\pi}} \cdot \frac{P_{OUT}}{\eta \cdot \sqrt{Vac_{LL} \cdot V_{OUT}}}$	

BOOST DESIGN EQUATIONS Components are identified in Figure 1

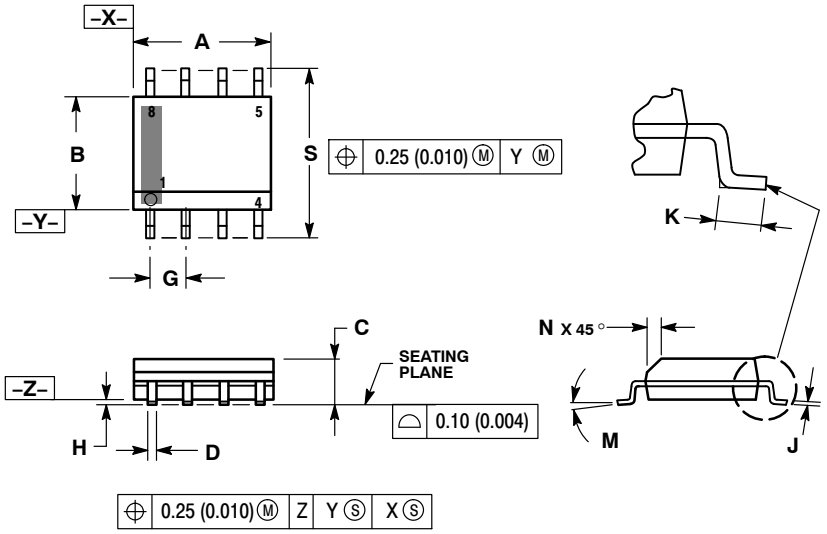
MOSFET RMS Current	$I_{M(RMS)MAX} = \frac{2}{\sqrt{3}} \cdot \frac{P_{out}}{\eta \cdot Vac_{LL}} \cdot \sqrt{1 - \left(\frac{8 \cdot \sqrt{2} \cdot Vac_{LL}}{3\pi \cdot V_{out}}\right)}$	
MOSFET Sense Resistor	$R_S = \frac{V_{CS(limit)}}{I_{pk(MAX)}}$ $P_{RS} = I_{M(RMS)}{}^2 \cdot R_S$	$V_{CS(limit)}$ is given in the NCP1607 specification table.
Bulk Capacitor RMS Current	$I_{C(RMS)} = \sqrt{\frac{32 \cdot \sqrt{2} \cdot P_{OUT}{}^2}{9 \cdot \pi \cdot Vac_{LL} \cdot V_{OUT} \cdot \eta^2} - (I_{LOAD(RMS)})^2}$	
Type 1 C_{COMP}	$C_{COMP} = \frac{10^{G/20}}{4 \cdot \pi \cdot f_{line} \cdot R_{OUT1}}$	G is the desired attenuation in decibels (dB). Typically it is 60 dB.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

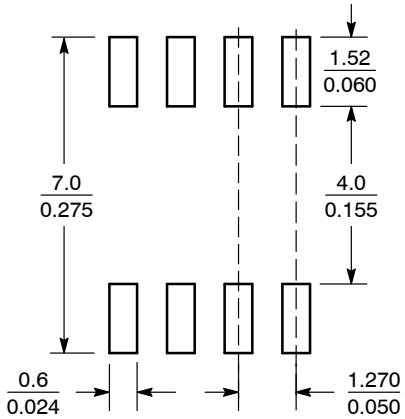
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

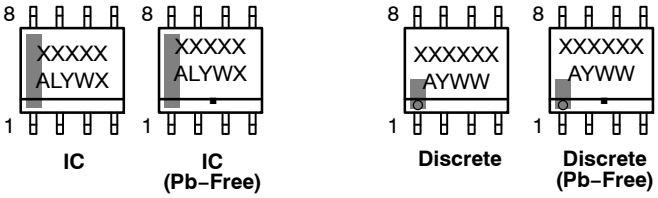
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−8 NB**	**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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