NCP1589A, NCP1589B

Synchronous Buck Controller, Low Voltage

The NCP1589A/B is a low cost PWM controller designed to operate from a 5 V or 12 V supply. This device is capable of producing an output voltage as low as 0.8 V. This device is capable of converting voltage from as low as 2.5 V. This 10-pin device provides an optimal level of integration to reduce size and cost of the power supply. Features include a 1.5 A gate driver design and an internally set 300 kHz or 600 kHz oscillator. In addition to the 1.5 A gate drive capability, other efficiency enhancing features of the gate driver include adaptive non-overlap circuitry. The NCP1589A/B also incorporates an externally compensated error amplifier. Protection features include programmable short circuit protection and undervoltage lockout (UVLO).

Features
- \( V_{CC} \) Range from 4.5 V to 13.2 V
- 300 kHz and 600 kHz Internal Oscillator
- Boost Pin Operates to 30 V
- Voltage Mode PWM Control
- Precision 0.8 V Internal Reference
- Adjustable Output Voltage
- Internal 1.5 A Gate Drivers
- 80% Max Duty Cycle
- Input Under Voltage Lockout
- Programmable Current Limit
- This is a Pb-Free Device

Applications
- Graphics Cards
- Desktop Computers
- Servers / Networking
- DSP & FPGA Power Supply
- DC–DC Regulator Modules

MARKING DIAGRAM

DFN10 CASE 485C

1589x = Specific Device Code
x = A or B
A = Assembly Location
L = Wafer Lot (Optional)
Y = Year
W = Work Week
\( \cdot \) = Pb-Free Device
(Note: Microdot may be in either location)

PIN CONNECTIONS

BOOT LX UG LG GND

1 2 3 4 5
10 9 8 7 6

VGOOD PGOOD FB VOS

VCC COMP/DISB

(Top View)

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package</th>
<th>Shipping†</th>
</tr>
</thead>
<tbody>
<tr>
<td>NCP1589AMNTWG</td>
<td>DFN10</td>
<td>3000 / Tape &amp; Reel</td>
</tr>
<tr>
<td>NCP1589BMNTWG</td>
<td>DFN10</td>
<td>3000 / Tape &amp; Reel</td>
</tr>
<tr>
<td>NCP1589AMNTXG</td>
<td>DFN10</td>
<td>3000 / Tape &amp; Reel</td>
</tr>
<tr>
<td>NCP1589BMNTXG</td>
<td>DFN10</td>
<td>3000 / Tape &amp; Reel</td>
</tr>
</tbody>
</table>

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
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Figure 1. Typical Application Diagram

Figure 2. Detailed Block Diagram
## PIN FUNCTION DESCRIPTION

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>BOOT</td>
<td>Supply rail for the floating top gate driver. To form a boost circuit, use an external diode to bring the desired input voltage to this pin (cathode connected to BOOT pin). Connect a capacitor (CBOOT) between this pin and the LX pin. Typical values for CBOOT range from 0.1 μF to 1 μF. Ensure that CBOOT is placed near the IC.</td>
</tr>
<tr>
<td>2</td>
<td>LX</td>
<td>Switch node pin. This is the reference for the floating top gate driver. Connect this pin to the source of the top MOSFET.</td>
</tr>
<tr>
<td>3</td>
<td>UG</td>
<td>Top gate MOSFET driver pin. Connect this pin to the gate of the top N−channel MOSFET.</td>
</tr>
<tr>
<td>4</td>
<td>LG</td>
<td>Bottom gate MOSFET driver pin. Connect this pin to the gate of the bottom N−channel MOSFET.</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>IC ground reference. All control circuits are referenced to this pin.</td>
</tr>
<tr>
<td>6</td>
<td>VCC</td>
<td>Supply rail for the internal circuitry. Operating supply range is 4.5 V to 13.2 V. Decouple with a 1 μF capacitor to GND. Ensure that this decoupling capacitor is placed near the IC.</td>
</tr>
<tr>
<td>7</td>
<td>COMP/DISB</td>
<td>Compensation Pin. This is the output of the error amplifier (EA) and the non−inverting input of the PWM comparator. Use this pin in conjunction with the FB pin to compensate the voltage−control feedback loop. Pull this pin low for disable.</td>
</tr>
<tr>
<td>8</td>
<td>FB</td>
<td>This pin is the inverting input to the error amplifier. Use this pin in conjunction with the COMP pin to compensate the voltage−control feedback loop. Connect this pin to the output resistor divider (If used) or directly to Vout.</td>
</tr>
<tr>
<td>9</td>
<td>VOS</td>
<td>Voltage Offset Sense</td>
</tr>
<tr>
<td>10</td>
<td>PGOOD</td>
<td>Power Good output. Pulled Low if VOS is ±10% of 0.8 V Vref.</td>
</tr>
</tbody>
</table>

## ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Symbol</th>
<th>VMAX</th>
<th>VMIN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main Supply Voltage Input</td>
<td>VCC</td>
<td>15 V</td>
<td>−0.3 V</td>
</tr>
<tr>
<td>Bootstrap Supply Voltage Input</td>
<td>BOOT</td>
<td>35 V *</td>
<td>−0.3 V</td>
</tr>
<tr>
<td>Switching Node (Bootstrap Supply Return)</td>
<td>LX</td>
<td>35 V</td>
<td>−5 V</td>
</tr>
<tr>
<td>High−Side Driver Output (Top Gate)</td>
<td>UG</td>
<td>30 V *</td>
<td>−0.3 V</td>
</tr>
<tr>
<td>Low−Side Driver Output (Bottom Gate)</td>
<td>LG</td>
<td>VCC + 0.3 V</td>
<td>−0.3 V</td>
</tr>
<tr>
<td>Feedback, VOS</td>
<td>FB, VOS</td>
<td>5.0 V</td>
<td>−0.3 V</td>
</tr>
<tr>
<td>COMP/DISB</td>
<td>COMP/DISB</td>
<td>3.6 V</td>
<td>−0.3 V</td>
</tr>
<tr>
<td>PGOOD</td>
<td>PGOOD</td>
<td>7 V</td>
<td>−0.3 V</td>
</tr>
</tbody>
</table>

## MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Resistance, Junction−to−Ambient</td>
<td>R_{JUA}</td>
<td>165</td>
<td>°C/W</td>
</tr>
<tr>
<td>Thermal Resistance, Junction−to−Case</td>
<td>R_{JUC}</td>
<td>45</td>
<td>°C/W</td>
</tr>
<tr>
<td>Operating Junction Temperature Range</td>
<td>T_J</td>
<td>0 to 150</td>
<td>°C</td>
</tr>
<tr>
<td>Operating Ambient Temperature Range</td>
<td>T_A</td>
<td>0 to 70</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>T_{stg}</td>
<td>−55 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>Moisture Sensitivity Level</td>
<td>MSL</td>
<td>1</td>
<td>–</td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

This device is ESD sensitive. Use standard ESD precautions when handling.
NCP1589A, NCP1589B

**ELECTRICAL CHARACTERISTICS** (0°C < TA < 70°C; 4.5 V < [BST–PHASE] < 13.2 V, 4.5 V < BST < 30 V, 0 V < PHASE < 21 V, CTG = CBG = 1.0 nF, for min/max values unless otherwise noted.)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC Voltage Range</td>
<td></td>
<td>4.5</td>
<td>13.2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Boost Voltage Range</td>
<td>13.2 V wrt LX</td>
<td>4.5</td>
<td>30</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

**Supply Current**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quiescent Supply Current (NCP1589A)</td>
<td>VFB = 1.0 V, No Switching, VCC = 13.2 V</td>
<td>1.0</td>
<td>8.0</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Boost Quiescent Current</td>
<td>VFB = 1.0 V, No Switching</td>
<td>0.1</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Undervoltage Lockout**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>UVLO Threshold (VCC Rising)</td>
<td>VCC Rising</td>
<td>3.8</td>
<td>4.0</td>
<td>4.2</td>
<td>V</td>
</tr>
<tr>
<td>UVLO Threshold (VCC Falling)</td>
<td>VCC Falling</td>
<td>3.4</td>
<td>3.6</td>
<td>3.8</td>
<td>V</td>
</tr>
<tr>
<td>UVLO Hysteresis</td>
<td>VCC Rising or VCC Falling</td>
<td>0.4</td>
<td></td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

**Switching Regulator**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VFB Feedback Voltage</td>
<td>(FB Tied to Comp. Measure FB Pin.)</td>
<td>0.7936</td>
<td>0.8</td>
<td>0.8064</td>
<td>V</td>
</tr>
<tr>
<td>Oscillator Frequency (NCP1589A)</td>
<td></td>
<td>270</td>
<td>300</td>
<td>330</td>
<td>kHz</td>
</tr>
<tr>
<td>Oscillator Frequency (NCP1589B)</td>
<td></td>
<td>540</td>
<td>600</td>
<td>660</td>
<td>kHz</td>
</tr>
<tr>
<td>Ramp–Amplitude Voltage</td>
<td></td>
<td>1.1</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Minimum Duty Cycle</td>
<td></td>
<td>0</td>
<td></td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Maximum Duty Cycle</td>
<td></td>
<td>70</td>
<td>75</td>
<td>80</td>
<td>%</td>
</tr>
<tr>
<td>LG Minimum on Time</td>
<td></td>
<td>500</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
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</table>

**Error Amplifier**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Open Loop DC Gain (Note 1)</td>
<td></td>
<td>70</td>
<td>80</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Output Source Current</td>
<td>VFB &lt; 0.8 V</td>
<td>2.0</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Output Sink Current</td>
<td>VFB &gt; 0.8 V</td>
<td>2.0</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Input Offset Voltage (Note 1)</td>
<td></td>
<td>–2.0</td>
<td>0</td>
<td>2.0</td>
<td>mV</td>
</tr>
<tr>
<td>Input Bias Current</td>
<td></td>
<td>0.1</td>
<td>1.0</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>Unity Gain Bandwidth (Note 1)</td>
<td></td>
<td>15</td>
<td></td>
<td>Mhz</td>
<td></td>
</tr>
<tr>
<td>Disable Threshold</td>
<td></td>
<td>0.6</td>
<td>0.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Output Source Current During Disable</td>
<td></td>
<td>10</td>
<td>40</td>
<td></td>
<td>μA</td>
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**Gate Drivers**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Upper Gate Source</td>
<td>VCC = 5 V, VUG – VLX = 2.5 V</td>
<td>1.5</td>
<td></td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Upper Gate Sink</td>
<td></td>
<td>1.4</td>
<td></td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>Lower Gate Source</td>
<td></td>
<td>1.5</td>
<td></td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Lower Gate Sink</td>
<td>VCC = 12 V</td>
<td>1.0</td>
<td></td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>UG Falling to LG Rising Delay</td>
<td>VCC = 12 V, UG–LX &lt; 2.0 V, LG &gt; 2.0 V</td>
<td>12.4</td>
<td>18</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>LG Falling to UG Rising Delay</td>
<td>VCC = 12 V, LG &lt; 2.0 V, UG &gt; 2.0 V</td>
<td>12.4</td>
<td>18</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

**Soft–Start**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Soft–Start time</td>
<td></td>
<td>3.0</td>
<td>7.0</td>
<td></td>
<td>ms</td>
</tr>
</tbody>
</table>

**Power Good**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Voltage</td>
<td>Logic Low, Sinking 4 mA</td>
<td></td>
<td>0.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>OVP Threshold to PGOOD Output Low</td>
<td>Ramp VOS from 0.7 to 1.2. Monitor when PGOOD goes Low</td>
<td>0.88</td>
<td>1.0</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>OVP Threshold to Part Disable</td>
<td>Ramp VOS from 0.8 to 1.2. Monitor when outputs disable</td>
<td>1.0</td>
<td>1.2</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>UVP Threshold to PGOOD Output Low</td>
<td>Ramp VOS from 800 mV to 500 mV. Monitor when PGOOD goes Low</td>
<td>0.65</td>
<td>0.72</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>UVP Threshold to Part Disable</td>
<td>Ramp VOS from 800 mV to 500 mV. Monitor when outputs stop switching</td>
<td>0.5</td>
<td>0.6</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

**Overcurrent Protection**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>OC Current Source (Note 1)</td>
<td>Sourced from LG pin, before SS</td>
<td>9.0</td>
<td>10</td>
<td>11</td>
<td>μA</td>
</tr>
</tbody>
</table>

1. Guaranteed by design but not tested in production.
Figure 3. Oscillator Frequency ($F_{SW}$) vs. Temperature

Figure 4. Reference Voltage ($V_{ref}$) vs. Temperature

Figure 5. $I_C$ vs. Temperature

Figure 6. OCP Threshold at 55k vs. Temperature
APPLICATIONS INFORMATION

Over Current Protection (OCP)

The NCP1589A/B monitors the voltage drop across the low side mosfet and uses this information to determine if there is excessive output current. The voltage across the low side mosfet is measured from the LX pin, and is referenced to ground. The over current measurement is timed to occur at the end of the low side mosfet conduction period, just before the bottom mosfet is turned off.

If the voltage drop across the bottom mosfet exceeds the over current protection threshold, then an internal counter is incremented. If the voltage drop does not exceed the over current protection threshold, then the internal counter is reset. The NCP1589A/B will latch the over current protection fault condition only if the over current protection threshold is exceeded for four consecutive cycles.

When the NCP1589A/B latches an over current protection fault, both the high side and low side mosfets are turned off. To reset the over current protection fault, the power to the VCC pin must be cycled.

The over current threshold voltage can be externally, by varying the value of the ROCSET resistor. The ROCSET resistor is a resistor connected between the LG pin (low side mosfet gate) and ground.

During startup, after the VCC and BOOT pins reach the under voltage lockout threshold, the NCP1589A/B will source 10 μA of current out of the LG pin. This current will flow through the ROCSET resistor and produce a voltage that is sampled and then used as the over current protection threshold voltage. For example, if ROCSET is set to 10 kΩ, the 10 μA of current will yield a 100 mV threshold, and if the voltage drop across the low side mosfet exceeds 100 mV at the end of its conduction period, then an over current event will be detected.

If the ROCSET resistor is not present, then the over current protection threshold will max out at 640 mV. The valid range for ROCSET is 5 kΩ to 55 kΩ which yields a threshold voltage range of 50 mV to 550 mV.

Internal Soft-Start

To prevent excess inrush current during startup, the NCP1589A/B uses a calibrated current source with an internal soft start capacitor to ramp the reference voltage from 0 to 800 mV over a period of 4 ms. The softstart ramp generator will reset if the input power supply voltages reach the under voltage lockout threshold, or if the NCP1589A/B is disabled by having the COMP pin pulled low.

Startup into a Precharged Load

During a startup and soft start sequence the NCP1589A will detect a residual charge on the output capacitors and not forcefully discharge the capacitors before beginning the softstart sequence, instead, the softstart ramping of the output will begin at the voltage level of the residual charge. For example, if the NCP1589A/B is configured to provide a regulated output voltage of 2.5 V, the normal softstart sequence will ramp the output voltage from 0 to 2.5 V in 4.2 ms; however if the output capacitors already have a 1.2 V charge on them, the NCP1589A/B will not discharge the capacitors, instead the softstart sequence will begin at 1.2 V and then ramp the output to 2.5 V.

Power Good

The PGOOD pin is an open drain active high output pin that signals the condition of the VOS (Voltage Output Sense) pin. PGOOD is pulled low during soft start cycle, and if there is a latched over current, over voltage, or under voltage fault. If the voltage on the VOS pin is within ±10% of Vref (800 mV) then the PGOOD pin will not be pulled low. The PGOOD pin does not have an internal pull-up resistor.

Overvoltage Protection

If the voltage on the VOS pin exceeds the over voltage threshold the NCP1589A/B will latch an over voltage fault. During an over voltage fault the UG pin will be pulled low, and the LG pin will be high while the until the voltage on the VOS pin goes below \(V_{\text{ref}/2}\) (400 mV). The NCP1589A will continue drive the LG pin, LG will go high if VOS exceeds 1 V and then go low when VOS goes below 400 mV. The power to the NCP1589 must be cycled to reset the over voltage protection fault.

Under Voltage Protection

If the voltage on the VOS pin falls below the under voltage threshold after the soft start cycle completes, then the NCP1589A/B will latch an under voltage fault. During an under voltage fault, both the UG and LG pins will be pulled low. The power to the NCP1589 must be cycled to reset the under voltage protection fault.
Figure 7. Typical Startup Sequence
Feedback and Compensation
The NCP1589A/B allows the output voltage to be adjusted from 0.8 V to 5.0 V via an external resistor divider network. The controller will try to maintain 0.8 V at feedback pin. Thus, if a resistor divider circuit was placed across the feedback pin to VOUT, the controller will regulate the output voltage proportional to the resistor divider network in order to maintain 0.8 V at the FB pin. The same formula applies to the VOS pin and the controller will maintain 0.8 V at the VOS pin.

\[
R_4 = R_1 \times \left( \frac{V_{REF}}{V_{OUT} - V_{REF}} \right)
\]

The same formula can be applied to the feedback resistors at VOS.

\[
R_9 = R_{10} \times \left( \frac{V_{REF}}{V_{OUT} - V_{REF}} \right)
\]

Design Example
Voltage Mode Control Loop with TYPE III Compensation
Converter Parameters:
Input Voltage: \( V_{IN} = 5 \) V
Output Voltage: \( V_{OUT} = 1.65 \) V
Switching Frequency: 300 kHz
Total Output Capacitance: \( C_{OUT} = 3600 \) \( \mu F \)
Total ESR: ESR = 6 \( m\Omega \)
Output Inductance: \( L_{OUT} = 1 \) \( \mu H \)
Ramp Amplitude: \( V_{RAMP} = 1.1 \) V

\[a.. \text{Set a target for the close loop bandwidth at } 1/6^{th} \text{ of the switching frequency.} \]
\[F_{cross\_over} := 50 \text{ kHz} \]
b. Output Filter Double Pole Frequency

\[ F_{lc} = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{OUT} \cdot C_{OUT}}} \]

\[ F_{lc} = 2.653 \text{ kHz} \]

c. ESR Zero Frequency:

\[ F_{ESR} = \frac{1}{2 \cdot \pi \cdot C_{OUT} \cdot C_{ESR}} \]

\[ F_{ESR} = 7.368 \text{ kHz} \]

Step 1: Set a value for R1 between 2 kΩ and 5 kΩ

R1 := 4.12 kΩ

Step 2: Pick compensation DC gain (R2/R1) for desired close loop bandwidth.

\[ V_{RAMP} := 1.1 \text{ V} \]

\[ R2 := R1 \cdot \left( \frac{V_{RAMP}}{V_{IN}} \right) \cdot \left( \frac{F_{cross\_over}}{F_{lc}} \right) \]

R2 = 17.085 kΩ

Step 3: Place 1st zero at half the output filter double pole frequency.

\[ C2 := \frac{2 \cdot \sqrt{L_{OUT} \cdot C_{OUT}}}{R2} \]

\[ C2 = 7.024 \times 10^{-3} \text{ µF} \]

Step 4: Place 1st pole at ESR zero frequency.

\[ C1 := \frac{C2 \cdot R2 \cdot 2 \cdot \pi \cdot F_{ESR} - 1}{C2} \]

\[ C1 = 1.542 \times 10^{-3} \text{ µF} \]

Step 5: Place 2nd zero at the output filter double pole frequency.

\[ R3 := \frac{R1}{\frac{F_{SW}}{2 \cdot F_{lc}} - 1} \]

\[ R3 = 74.169 \text{ Ω} \]

Step 6: Place 2nd pole at half the switching frequency.

\[ C3 := \frac{1}{\left( \pi \cdot R3 \cdot F_{SW} \right)} \]

\[ C3 = 0.014 \text{ µF} \]

Step 7: R4 is sized to maintain the feedback voltage to V_{ref} = 0.8 V.

\[ R4 := \frac{V_{REF} \cdot R1}{V_{OUT} - V_{REF}} \]

\[ R4 = 3.878 \text{ kΩ} \]

The Component values for Type III Compensation are:

R1 = 4.12 kΩ
R2 = 17.085 kΩ
R3 = 74.169 Ω
R4 = 3.878 kΩ
C1 = 0.0015 µF
C2 = 0.007 µF
C3 = 0.014 µF

NOTE: Recommend to change values to industry standard component values.
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

DFN10, 3x3, 0.5P
CASE 485C
ISSUE F
DATE 16 DEC 2021

NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL b MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASH MAY NOT EXCEED 30 MICRONS ON TOP SURFACE OF TERMINAL.
6. FOR DEVICE DPN CONTAINING W OPTION, DETAIL A AND DETAIL B ALTERNATE CONSTRUCTIONS ARE NOT APPLICABLE. WETTABLE FLANK CONSTRUCTION IS DETAIL B AS SHOWN ON SIDE VIEW OF PACKAGE.

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WASHINGTON, DC
EXPOSED COPPER
PLATED SURFACE
PLATED COPPER
PACKING OUTLINE

NOTE: Microdot may be in either location

ALTERNATE A-1
ALTERNATE A-2

DESCRIPTION OF GENERIC MARKING DIAGRAM:
XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
* = Pb-Free Package
(NOTE: Microdot may be in either location)

*(This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "*", may or may not be present. Some products may not follow the Generic Marking.)

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DOCUMENT NUMBER: 98AON03161D
DESCRIPTION: DFN10, 3X3 MM, 0.5 MM PITCH
PAGE 1 OF 1