

# High Performance Active Clamp/Reset PWM Controller

## NCP1562A, NCP1562B

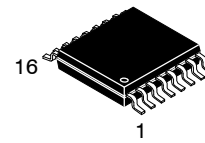
The NCP1562x is a family of voltage mode controllers designed for dc-dc converters requiring high-efficiency and low parts count. These controllers incorporate two in phase outputs with an overlap delay to prevent simultaneous conduction and facilitates soft switching. The main output is designed for driving a forward converter primary MOSFET. The secondary output is designed for driving an active clamp circuit MOSFET, a synchronous rectifier on the secondary side, or an asymmetric half bridge circuit.

The NCP1562 family reduces component count and system size by incorporating high accuracy on critical specifications such as maximum duty cycle limit, undervoltage detector and overcurrent threshold. Two distinctive features of the NCP1562 are soft-stop and a cycle skip current limit with a time threshold. Soft-stop circuitry powers down the converter in a controlled manner if a severe fault is detected. The cycle skip detector enables a soft-stop sequence if a continuous overcurrent condition is present.

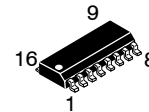
Additional features found in the NCP1562 include line feed-forward, frequency synchronization up to 1.0 MHz, cycle-by-cycle current limit with leading edge blanking (LEB), independent under and overvoltage detectors, adjustable output overlap delay, programmable maximum duty cycle, internal startup circuit and soft-start.

### Features

- Dual Control Outputs with Adjustable Overlap Delay
- >2.0 A Output Drive Capability
- Soft-Stop Powers Down Converter in a Controlled Manner
- Cycle-by-Cycle Current Limit
- Cycle Skip Initiated if Continuous Current Limit Condition Exists
- Voltage Mode Operation with Input Voltage Feedforward
- Fixed Frequency Operation up to 1.0 MHz
- Bidirectional Frequency Synchronization
- Independent Line Undervoltage and Overvoltage Detectors
- Accurate Programmable Maximum Duty Cycle Limit
- Programmable Maximum Volt-Second Product
- Programmable Soft-Start
- Internal 100 V Startup Circuit
- Precision 5.0 V Reference
- These are Pb-Free Devices
- ATX Power Supplies

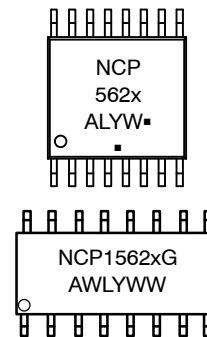


TSSOP-16  
DT SUFFIX  
CASE 948F



SOIC-16  
D SUFFIX  
CASE 751B

### MARKING DIAGRAMS



- x = Current Limit (A, B)
- A = Assembly Location
- WL, L = Wafer Lot
- Y = Year
- WW, W = Work Week
- G or ▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 24 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 24.

### Typical Applications

- Telecommunications Power Converters
- Low Output Voltage Converters using Control Driven Synchronous Rectifier
- Industrial Power Converters
- 42 V Automotive System



## NCP1562A, NCP1562B

### PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	$V_{in}$	Connect the input line voltage directly to this pin to enable the internal startup regulator. A constant current source supplies current from this pin to the capacitor connected to the $V_{AUX}$ pin, eliminating the need for a startup resistor. The charge current is typically 10 mA. Maximum input voltage is 100 V.
2	UVOV	Input supply voltage is scaled down and sampled by means of a resistor divider. The same pin is used for both undervoltage (UV) and overvoltage (OV) detection using a novel architecture (patent pending). The minimum and maximum input supply voltage thresholds are adjusted independently. A UV condition exists if the UVOV voltage is below 2.0 V and an OV condition exists if the UVOV voltage exceeds 3.0 V. The undervoltage threshold is trimmed during manufacturing to obtain $\pm 3\%$ accuracy allowing a tighter power stage design. Both the UV and OV detectors have a 100 mV hysteresis.
3	FF	An external R-C divider from the input line generates the Feedforward Ramp. This ramp is used by the PWM comparator to set the duty cycle, thus providing direct line regulation. An internal pulldown transistor discharges the external capacitor every cycle. Once discharged, the capacitor is effectively grounded until the next cycle begins.
4	CS	Overcurrent sense input. If the CS voltage exceeds 0.2 V (or 0.5 V in the NCP1562B) the converter operates in cycle-by-cycle current limit. Once a current limit pulse is detected, the cycle skip timer is enabled. Internal leading edge blanking pulse prevents nuisance triggering during normal operation. The leading edge blanking is disabled during soft-start and output overload conditions to improve the response to faults.
5	GND	Control circuit ground. All control and timing components that connect to GND should have the shortest loop possible to this pin to improve noise immunity.
6	$R_T C_T$	An external $R_T C_T$ divider from $V_{REF}$ sets the operating frequency and maximum duty cycle of OUT1. The maximum operating frequency is 1.0 MHz. A sawtooth Ramp between 2.0 V and 3.0 V is generated by sequentially charging and discharging $C_T$ . The peak and valley of the Ramp are accurately controlled to provide precise control of the duty cycle and frequency. The outputs are disabled during the $C_T$ discharge time.
7	SYNC	Proprietary bidirectional frequency synchronization architecture allows two NCP1562 devices to synchronize together. The lower frequency device becomes the slave. It can also synchronize to an external signal.
8	$V_{REF}$	Precision 5.0 V reference. Maximum output current is 5.0 mA. It is required to bypass the reference with a capacitor. The recommended capacitance range is between 0.047 $\mu$ F and 1.0 $\mu$ F.
9	$V_{EA}$	The error signal from an external error amplifier is fed to this input and compared to the Feedforward Ramp. A series diode and resistor offset the voltage on this pin before it is applied to the PWM Comparator inverting input. An internal pullup resistor allows direct connection to an optocoupler.
10	SS	A 10 $\mu$ A current source charges the external capacitor connected to this pin. Duty cycle is limited during startup by comparing the voltage on this pin to the Feedforward Ramp. Under steady state conditions, the SS voltage is approximately 3.8 V. Once a UV, OV, overtemperature or cycle skip fault is detected, the SS capacitor is discharged in a controlled manner with a 100 $\mu$ A current source. The duty cycle is then slowly reduced until reaching 0%.
11	$t_D$	An external resistor between this pin and GND sets the overlap time delay between OUT1 and OUT2 transitions.
12	CSKIP	The converter is disabled if a continuous overcurrent condition exists. The time to determine the fault and the time the converter is disabled are programmed by the capacitor ( $C_{CSKIP}$ ) connected to this pin. The cycle skip timer is enabled after a current limit fault is detected. Once enabled, $C_{CSKIP}$ is charged with a 100 $\mu$ A source. If the overcurrent fault is removed before entering the soft-stop mode, the capacitor is discharged with a 10 $\mu$ A source. Once $C_{CSKIP}$ reaches 3.0 V, the converter enters a soft-stop mode and $C_{CSKIP}$ is discharged with a 10 $\mu$ A source. The converter is re-enabled once $C_{CSKIP}$ reaches 0.5 V. If the condition resulting in overcurrent is cleared during this phase, $C_{CSKIP}$ discharges to 0 V. Otherwise, it starts charging from 0.5 V, setting up a hiccup mode operation.
13	OUT2	Secondary output of the PWM Controller. It can be used to drive an active clamp/reset switch, a synchronous rectifier topology, or both. OUT2 has an adjustable leading and trailing edge overlap delay against OUT1. OUT2 has source and sink resistances of 12 $\Omega$ (typ.). OUT2 is designed to handle up to 1.0 A.
14	PGND	Ground connection for OUT1 and OUT2. Tie to the power stage return with a short loop.

## NCP1562A, NCP1562B

### PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol	Description
15	OUT1	Main output of the PWM Controller. OUT1 has a source resistance of 4.0 $\Omega$ (typ.) and a sink resistance of 2.5 $\Omega$ (typ.). OUT1 is designed to handle up to 2.5 A. OUT1 trails OUT2 during a low to high transition and leads OUT2 during a high to low transition.
16	V <sub>AUX</sub>	Positive input supply. This pin connects to an external capacitor for energy storage. An internal current source supplies current from V <sub>in</sub> to this pin. Once the voltage on V <sub>AUX</sub> reaches approximately 10.3 V, the current source turns OFF and the outputs are enabled. It turns ON again once V <sub>AUX</sub> falls to 8.0 V. If the bias current consumption exceeds the startup current, V <sub>AUX</sub> will continue to discharge. Once V <sub>AUX</sub> reaches 7.0 V, the outputs are disabled allowing V <sub>AUX</sub> to charge. During normal operation, power is supplied to the IC via this pin by means of an auxiliary winding. The startup circuit is disabled once the voltage on the V <sub>AUX</sub> pin exceeds 10.3 V. If the V <sub>AUX</sub> voltage drops below 1.2 V (typ), the startup current is reduced to 200 $\mu$ A.

## NCP1562A, NCP1562B

### MAXIMUM RATINGS (Notes 1 and 2)

Symbol	Rating	Value	Unit
$V_{in}$	Line Voltage	100	V
$V_{AUX}, V_{outx}$	Auxiliary Supply, OUT1, OUT2	20	V
$V_{IO}$	All Other Inputs/Outputs Voltage	10	V
$I_{IO}$	All Other Inputs/Outputs Current	5.0	mA
$I_{REF}$	5.0 V Reference Output Current	10	mA
$V_{REF}$	5.0 V Reference Output Voltage	-0.3 to 6.0	V
$I_{out1}$	OUT1 Peak Output Current (D = 2%)	2.5	A
$I_{out2}$	OUT2 Peak Output Current (D = 2%)	1.0	A
$T_J$	Operating Junction Temperature	-40 to +125	°C
$T_{stg}$	Storage Temperature Range	-55 to +150	°C
$P_D$	Power Dissipation ( $T_A = 25\text{ °C}$ , 2.0 Oz Cu, 1.0 Sq Inch Printed Circuit Copper Clad) DT Suffix, Plastic Package Case 948F (TSSOP-16) D Suffix, Plastic Package Case 751B (SO-16)	0.75 0.95	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (2.0 Oz Cu Printed Circuit Copper Clad) DT Suffix, Plastic Package Case 948F (TSSOP-16) 0.36 Sq In 1.0 Sq In D Suffix, Plastic Package Case 751B (SO-16) 0.36 Sq In 1.0 Sq In	155 133 120 105	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- This device series contains ESD protection and exceeds the following tests:  
Pins 2-16: Human Body Model 2000 V per MIL-STD-883, Method 3015.  
Machine Model Method 160 V.  
Pin 1 is the HV startup of the device and is rated to the max rating of the part, or 100 V.
- This device contains Latchup protection and exceeds  $\pm 100$  mA per JEDEC Standard JESD78.

# NCP1562A, NCP1562B

**ELECTRICAL CHARACTERISTICS** ( $V_{in} = 48\text{ V}$ ,  $V_{AUX} = 12\text{ V}$ ,  $V_{UVOV} = 2.3\text{ V}$ ,  $V_{EA} = \text{open}$ ,  $V_{CSKIP} = 0\text{ V}$ ,  $V_{CS} = 0\text{ V}$ ,  $V_{SS} = \text{open}$ ,  $R_T = 13.3\text{ k}\Omega$ ,  $C_{AUX} = 10\text{ }\mu\text{F}$ ,  $C_T = 470\text{ pF}$ ,  $C_{out1} = C_{out2} = 100\text{ pF}$ ,  $C_{UVOV} = 0.01\text{ }\mu\text{F}$ ,  $C_{CSKIP} = 6800\text{ pF}$ ,  $R_D = 25\text{ k}\Omega$ ,  $R_{SYNC} = 5.0\text{ k}\Omega$ ,  $C_{REF} = 0.1\text{ }\mu\text{F}$ ,  $R_{FF} = 29.4\text{ k}\Omega$ ,  $C_{FF} = 470\text{ pF}$ . For typical values  $T_J = 25\text{ }^\circ\text{C}$ , for min/max values,  $T_J$  is  $-40\text{ }^\circ\text{C}$  to  $125\text{ }^\circ\text{C}$ , unless otherwise noted.)

Symbol	Characteristic	Min	Typ	Max	Unit
<b>STARTUP CONTROL AND <math>V_{AUX}</math> REGULATOR</b>					
$V_{inhibit}$ $V_{AUX(on)}$ $V_{AUX(off1)}$ $V_{AUX(off2)}$	$V_{AUX}$ Regulation ( $V_{UVOV} = 0\text{ V}$ ) Inhibit Threshold Voltage Startup Threshold/ $V_{AUX}$ Regulation Peak ( $V_{AUX}$ Increasing) Operating $V_{AUX}$ Valley Voltage Minimum Operating $V_{AUX}$ Valley Voltage after Turn-On ( $V_{UVOV} = 2.3\text{ V}$ , $V_{EA} = 0\text{ V}$ )	– 9.65 7.42 6.50	1.15 10.3 8.0 7.0	1.5 10.97 8.48 7.42	V
$V_{start(min)}$	Minimum Startup Voltage (Pin 1) $I_{AUX} = 1.0\text{ mA}$ , $V_{AUX} = V_{AUX(on)} - 0.2\text{ V}$	–	–	23.2	V
$I_{inhibit}$	Inhibit Bias Current $V_{AUX} = 0\text{ V}$	70	170	300	$\mu\text{A}$
$I_{start1}$ $I_{start2}$	Startup Circuit Output Current $V_{AUX} = V_{inhibit} + 0.2\text{ V}$ $V_{AUX} = V_{AUX(on)} - 0.2\text{ V}$	7.16 4.03	9.3 6.1	11.3 8.1	mA
$I_{start(off)}$	Startup Circuit Off-State Leakage Current ( $V_{in} = 200\text{ V}$ , $V_{UVOV} = 0\text{ V}$ ) $T_J = 25\text{ }^\circ\text{C}$ $T_J = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$	– –	25 –	50 100	$\mu\text{A}$
$V_{BR(DS)}$	Startup Circuit Breakdown Voltage (Note 3) $I_{start(off)} = 50\text{ }\mu\text{A}$ , $T_J = 125\text{ }^\circ\text{C}$	100	–	–	V
$I_{AUX1}$ $I_{AUX2}$ $I_{AUX3}$	Auxiliary Supply Current after $V_{AUX}$ Turn-On Outputs Disabled $V_{UVOV} = 0\text{ V}$ $V_{EA} = 0\text{ V}$ Outputs Enabled $V_{EA} = 4.0\text{ V}$	– – –	3.0 4.2 5.5	3.6 4.94 7.0	mA

### LINE UNDER/OVERVOLTAGE DETECTOR

$V_{UV}$	Undervoltage Threshold ( $V_{in}$ Increasing)	1.979	2.05	2.116	V
$V_{UV(H)}$	Undervoltage Hysteresis	0.074	0.093	0.118	V
$V_{UV(ratio)}$	Undervoltage Ratio ( $V_{UV(H)}/V_{UV}$ )	3.65	4.50	5.62	%
$V_{OV}$	Overvoltage Threshold ( $V_{in}$ Increasing)	2.80	2.95	3.10	V
$V_{OV(H)}$	Overvoltage Hysteresis	0.075	0.093	0.127	V
$I_{offset(UVOV)}$	Offset Current ( $V_{UVOV} = 2.8\text{ V}$ )	38	48	58	$\mu\text{A}$
$V_{offset(UVOV)}$	Offset Current Turn ON Threshold ( $\pm 5\%$ , $I_{offset(UVOV)} = 40\text{ }\mu\text{A}$ )	2.4	2.6	2.8	V

### LINE FEEDFORWARD

$V_{FF(peak)}$	Peak Voltage (Volt-Second Clamp)	2.8	3.0	3.2	V
$I_{FF(D)}$	Discharge Current ( $V_{FF} = 0.5\text{ V}$ , $V_{SS} = 0\text{ V}$ )	8.5	–	–	mA
$V_{offset(FF)}$	Offset Voltage ( $V_{FF} = 0\text{ V}$ , Ramp Down $V_{SS}$ )	0.118	0.185	0.268	V
$\Delta_{(FF-SS)}$	Feedforward Offset Minus Soft-Stop Reset Voltage	7	70	183	mV

3. Guaranteed by design only.

# NCP1562A, NCP1562B

**ELECTRICAL CHARACTERISTICS (continued)** ( $V_{in} = 48\text{ V}$ ,  $V_{AUX} = 12\text{ V}$ ,  $V_{UVOV} = 2.3\text{ V}$ ,  $V_{EA} = \text{open}$ ,  $V_{CSKIP} = 0\text{ V}$ ,  $V_{CS} = 0\text{ V}$ ,  $V_{SS} = \text{open}$ ,  $R_T = 13.3\text{ k}\Omega$ ,  $C_{AUX} = 10\text{ }\mu\text{F}$ ,  $C_T = 470\text{ pF}$ ,  $C_{out1} = C_{out2} = 100\text{ pF}$ ,  $C_{UVOV} = 0.01\text{ }\mu\text{F}$ ,  $C_{CSKIP} = 6800\text{ pF}$ ,  $R_D = 25\text{ k}\Omega$ ,  $R_{SYNC} = 5.0\text{ k}\Omega$ ,  $C_{REF} = 0.1\text{ }\mu\text{F}$ ,  $R_{FF} = 29.4\text{ k}\Omega$ ,  $C_{FF} = 470\text{ pF}$ . For typical values  $T_J = 25\text{ }^\circ\text{C}$ , for min/max values,  $T_J$  is  $-40\text{ }^\circ\text{C}$  to  $125\text{ }^\circ\text{C}$ , unless otherwise noted.)

Symbol	Characteristic	Min	Typ	Max	Unit
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## CURRENT LIMIT AND THERMAL SHUTDOWN

$V_{LIM}$	Cycle-by-Cycle Threshold Voltage ( $V_{out} = 10\text{ V}$ ) NCP1562A NCP1562B	191 472	203 495	217 512	mV
$t_{LIM}$	Propagation Delay to Output ( $V_{CS} = V_{LIM}$ to $1.0\text{ V}$ , LEB Disabled, $V_{out} = 10\text{ V}$ ) $T_J = 25\text{ }^\circ\text{C}$ $T_J = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$	– –	78 –	90 110	ns
$T_{SHDN}$	Thermal Shutdown Threshold (Junction Temperature Increasing, Note 4)	–	160	–	$^\circ\text{C}$
$T_H$	Thermal Shutdown Hysteresis (Temperature Decreasing, Note 4)	–	25	–	$^\circ\text{C}$

## LEADING EDGE BLANKING

$V_{LEB(\text{offset})}$	Offset Voltage	–	10	–	mV
$t_{LEB}$	Blanking Time	50	80	110	ns
$V_{LEB(\text{dis})}$	$V_{EA}$ Threshold the Disables LEB (Measured together with $t_{LEB}$ )	4.1	–	–	V

## CYCLE SKIP CURRENT LIMIT MODE

$I_{CSKIP(C)}$	Charge Current ( $V_{CSKIP} = 1.25\text{ V}$ )	70	90	111	$\mu\text{A}$
$I_{CSKIP(D)}$	Discharge Current ( $V_{CSKIP} = 1.25\text{ V}$ )	6.5	8.6	11	$\mu\text{A}$
$\text{Pulse}_{CSKIP}$	Number of Pulses to Exit Cycle Skip Mode	–	3	–	–
$V_{CSKIP(\text{peak})}$	Upper Threshold Voltage (Ramp up $V_{CSKIP}$ , $V_{CS} = 1.0\text{ V}$ )	2.83	3.03	3.24	V
$V_{CSKIP(\text{valley})}$	Lower Threshold Voltage (Ramp down $V_{CSKIP}$ )	0.39	0.465	0.52	V
$V_{CSKIP(H)}$	Threshold Voltage Hysteresis	–	2.5	–	V

## 5.0 V REFERENCE

$V_{REF}$	Output Voltage ( $I_{REF} = 0\text{ mA}$ )	4.9	5.0	5.1	V
$V_{REF(\text{Load})}$	Load Regulation ( $I_{REF} = 0$ to $5.0\text{ mA}$ )	–	16	50	mV
$V_{REF(\text{line})}$	Line Regulation ( $V_{AUX} = 7.5$ to $20\text{ V}$ , $I_{REF} = 0\text{ mA}$ )	–	10	50	mV
$I_{REF(D)}$	Discharge Current ( $V_{UVOV} = 0\text{ V}$ , $V_{REF} = 2.5\text{ V}$ )	3.8	–	–	mA

## OSCILLATOR

$f_{OSC}$	Frequency $T_J = 25\text{ }^\circ\text{C}$ $T_J = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$	222 211.2	246 –	272.2 277.2	kHz
$V_{RTCT(\text{peak})}$	Peak Voltage	–	2.95	–	V
$V_{RTCT(\text{valley})}$	Valley Voltage	–	2.1	–	V
$I_{RTCT}$	Discharge Current ( $V_{RTCT} = 2.3\text{ V}$ )	–	490	–	$\mu\text{A}$
$f_{MAX}$	Maximum Operating Frequency (Note 4)	1.0	–	–	MHz
D	Duty Cycle ( $R_D = 25\text{ k}\Omega$ )	58.5	62.0	64.7	%
$D_{MAX}$	Adjustable Maximum Duty Cycle (Note 4)	85	–	–	%

4. Guaranteed by design only.

# NCP1562A, NCP1562B

**ELECTRICAL CHARACTERISTICS (continued)** ( $V_{in} = 48\text{ V}$ ,  $V_{AUX} = 12\text{ V}$ ,  $V_{UVOV} = 2.3\text{ V}$ ,  $V_{EA} = \text{open}$ ,  $V_{CSKIP} = 0\text{ V}$ ,  $V_{CS} = 0\text{ V}$ ,  $V_{SS} = \text{open}$ ,  $R_T = 13.3\text{ k}\Omega$ ,  $C_{AUX} = 10\text{ }\mu\text{F}$ ,  $C_T = 470\text{ pF}$ ,  $C_{out1} = C_{out2} = 100\text{ pF}$ ,  $C_{UVOV} = 0.01\text{ }\mu\text{F}$ ,  $C_{CSKIP} = 6800\text{ pF}$ ,  $R_D = 25\text{ k}\Omega$ ,  $R_{SYNC} = 5.0\text{ k}\Omega$ ,  $C_{REF} = 0.1\text{ }\mu\text{F}$ ,  $R_{FF} = 29.4\text{ k}\Omega$ ,  $C_{FF} = 470\text{ pF}$ . For typical values  $T_J = 25\text{ }^\circ\text{C}$ , for min/max values,  $T_J$  is  $-40\text{ }^\circ\text{C}$  to  $125\text{ }^\circ\text{C}$ , unless otherwise noted.)

Symbol	Characteristic	Min	Typ	Max	Unit
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## SYNCHRONIZATION

$t_{O(SYNC)}$	Output Pulse Width	70	110	–	ns
$V_{H(SYNC)}$	Output Voltage High ( $R_{SYNC} = \infty$ )	–	4.3	–	V
$V_{SYNC}$	Sync Threshold Voltage (Note 5)	3.5	–	–	V
$t_{SYNC}$	Sync Input Pulse Width ( $V_{SYNC} = 3.5\text{ V}$ )	–	–	$t_{O(SYNC)min}$	ns
$f_{SYNC}$	Maximum Sync Frequency (Note 5)	–	–	1.0	MHz
$I_{SYNC(D)}$	Source Current (Note 5)	–	1.0	–	mA

## SOFT-START/STOP

$I_{SS(C)}$	Charge Current ( $V_{SS} = 1.6\text{ V}$ )	8.3	10.2	13.1	$\mu\text{A}$
$I_{SS(D)}$	Discharge Current ( $V_{UVOV} = 0\text{ V}$ , $V_{SS} = 1.6\text{ V}$ )	72	95	115	$\mu\text{A}$
$V_{reset(SS)}$	Soft-Stop Reset Voltage ( $V_{FF} = 0\text{ V}$ )	–	115	–	mV

## OUTPUTS

$t_{D(leading)}$ $t_{D(trailing)}$	Overlap Time Delay (Tested at 50% of Waveform) Leading Trailing	37 72	45 90	– –	ns
$V_{OL}$ $V_{OH}$	Output Voltage ( $I_{OUT} = 0\text{ mA}$ , Note 5) Low State High State	– 11.8	– –	0.25 –	V
$R_{SNK1}$ $R_{SRC1}$ $R_{SNK2}$ $R_{SRC2}$	Drive Resistance (FT ONLY) OUT1 Sink ( $V_{RTCT} = 4.0\text{ V}$ , $V_{out1} = 1.0\text{ V}$ ) $T_J = 25\text{ }^\circ\text{C}$ $T_J = -40\text{ }^\circ\text{C to } 125\text{ }^\circ\text{C}$ OUT1 Source ( $V_{RTCT} = 2.5\text{ V}$ , $V_{out1} = 11\text{ V}$ ) $T_J = 25\text{ }^\circ\text{C}$ $T_J = -40\text{ }^\circ\text{C to } 125\text{ }^\circ\text{C}$ OUT2 Sink ( $V_{RTCT} = 4.0\text{ V}$ , $V_{out2} = 1.0\text{ V}$ ) $T_J = 25\text{ }^\circ\text{C}$ $T_J = -40\text{ }^\circ\text{C to } 125\text{ }^\circ\text{C}$ OUT2 Source ( $V_{RTCT} = 2.5\text{ V}$ , $V_{out2} = 11\text{ V}$ ) $T_J = 25\text{ }^\circ\text{C}$ $T_J = -40\text{ }^\circ\text{C to } 125\text{ }^\circ\text{C}$	– – – – – – – –	2.8 – 4.7 – 11.4 – 11.6 –	3.6 5.03 5.75 7.45 12.7 20.0 13.5 20.0	$\Omega$
$t_{r1}$ $t_{r2}$	Rise Time (10% to 90%, $C_{out1} = 2200\text{ pF}$ , $C_{out2} = 220\text{ pF}$ ) OUT1 OUT2	– –	26 19	– –	ns
$t_{f1}$ $t_{f2}$	Fall Time (90% to 10%, $C_{out1} = 2200\text{ pF}$ , $C_{out2} = 220\text{ pF}$ ) OUT1 OUT2	– –	10 10	– –	ns

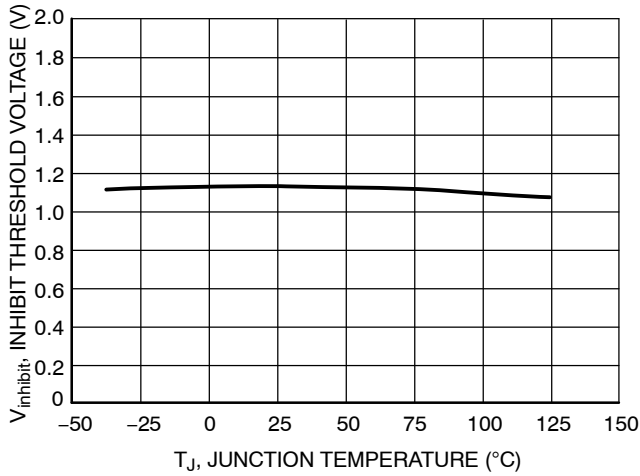
## PWM COMPARATOR

$R_{IN(VEA)}$	Input Resistance	11	25	58	$\text{k}\Omega$
$V_{EA(L)}$	Lower Input Threshold	0.48	0.83	1.04	V
$t_{PWM}$	Delay to Output (From $V_{OH}$ to $0.5 V_{OH}$ )	–	100	–	ns

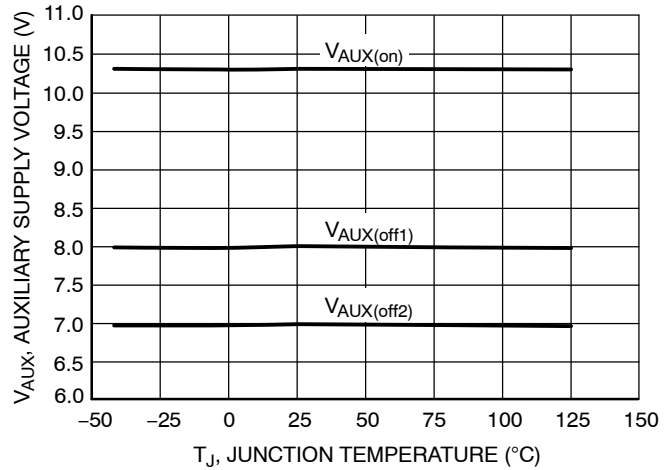
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Guaranteed by design only.

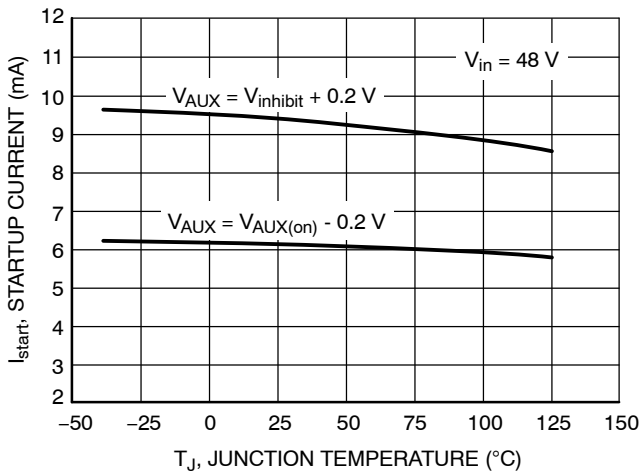
# NCP1562A, NCP1562B



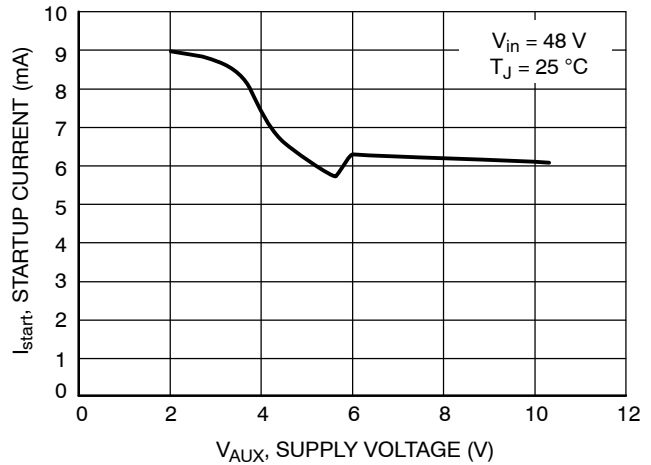
**Figure 2. Startup Circuit Inhibit Voltage Threshold vs. Junction Temperature**



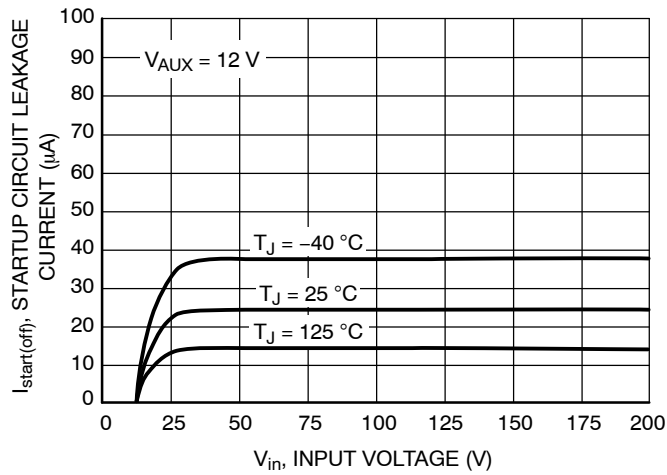
**Figure 3. Auxiliary Supply Voltage Thresholds vs. Junction Temperature**



**Figure 4. Startup Current vs. Junction Temperature**

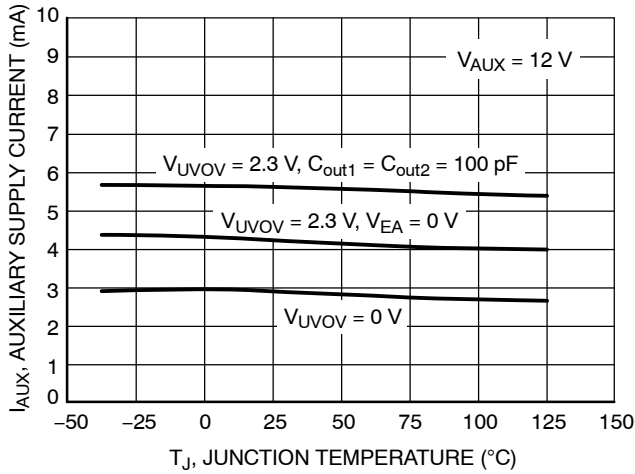


**Figure 5. Startup Current vs. Supply Voltage**

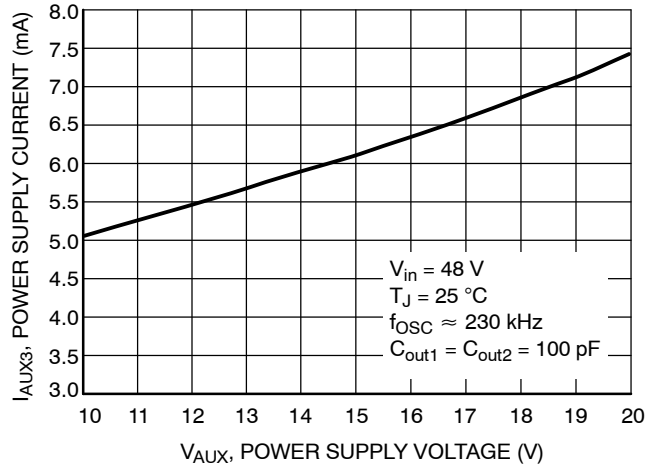


**Figure 6. Startup Circuit Leakage Current vs. Input Voltage**

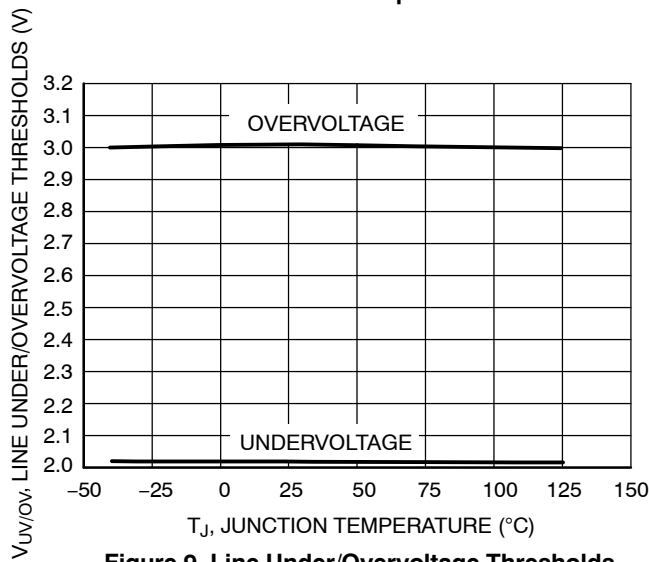
# NCP1562A, NCP1562B



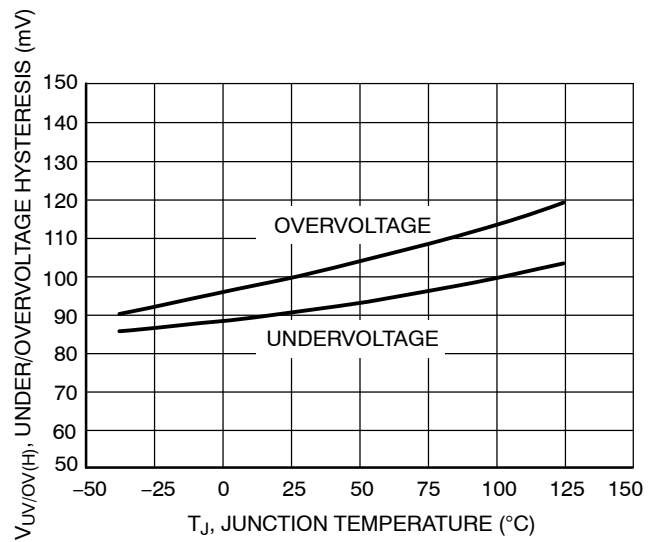
**Figure 7. Auxiliary Supply Current vs. Junction Temperature**



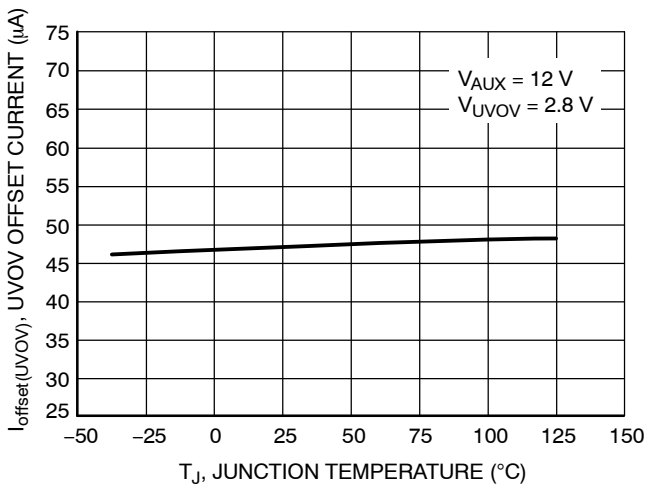
**Figure 8. Supply Current vs. Supply Voltage**



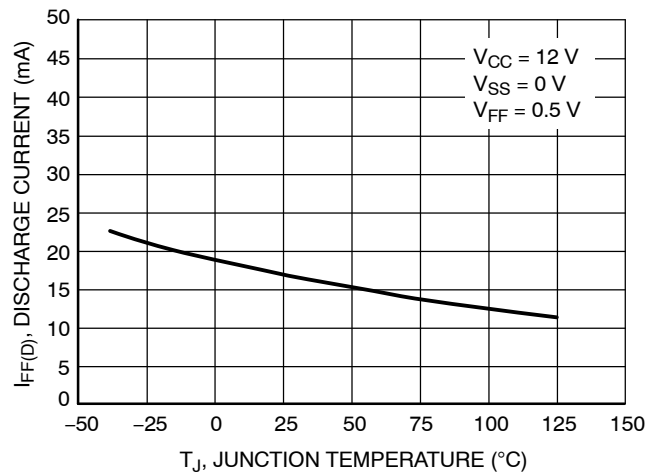
**Figure 9. Line Under/Overvoltage Thresholds vs. Junction Temperature**



**Figure 10. Line Under/Overvoltage Hysteresis vs. Junction Temperature**

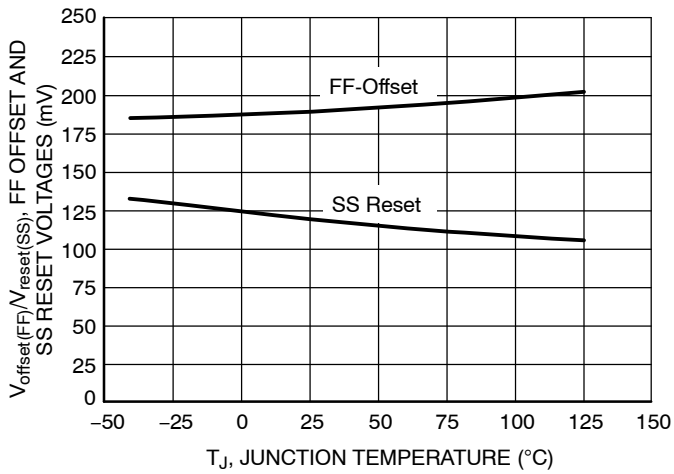


**Figure 11. UVOV Offset Current vs. Junction Temperature**

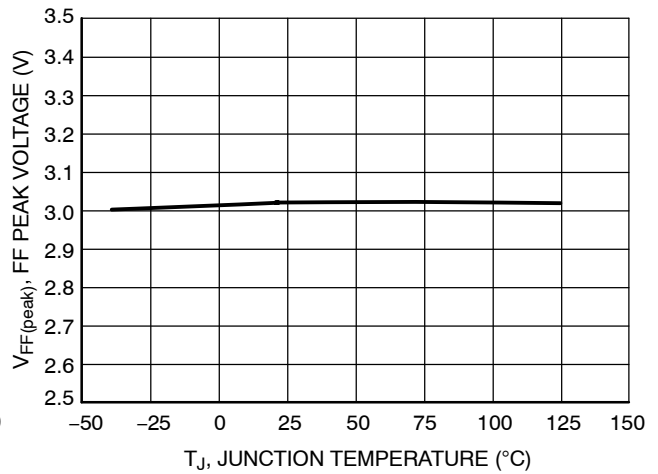


**Figure 12. FF Discharge Current vs. Junction Temperature**

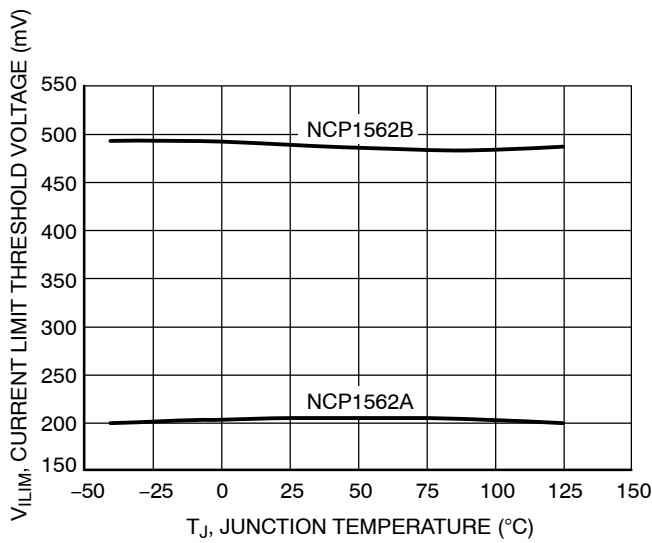
# NCP1562A, NCP1562B



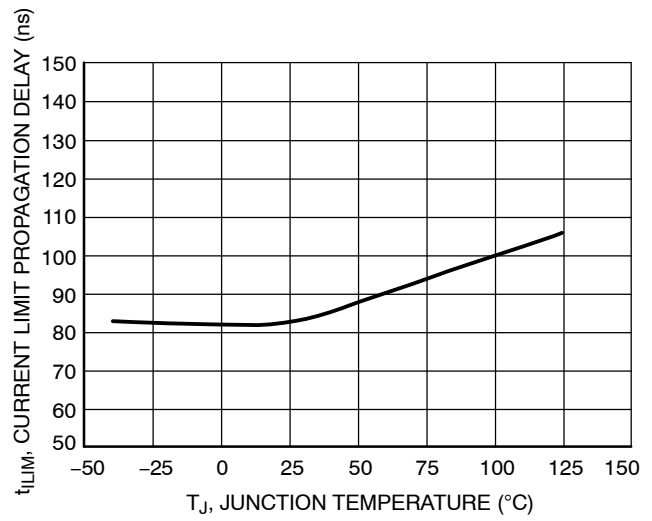
**Figure 13. FF Offset and SS Reset Voltages vs. Junction Temperature**



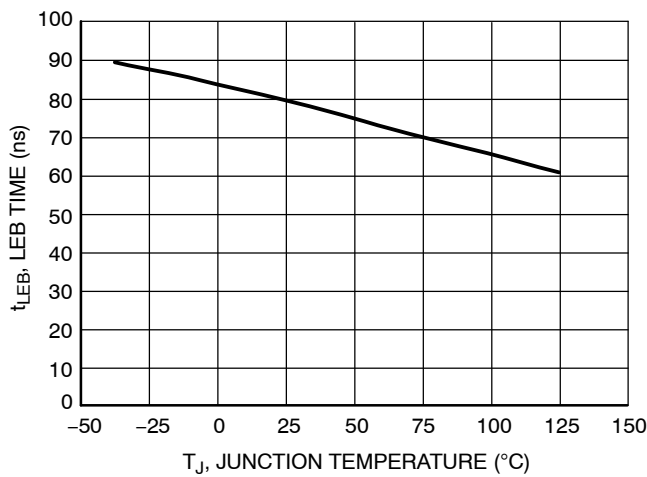
**Figure 14. Feedforward Peak Voltage vs. Junction Temperature**



**Figure 15. Current Limit Threshold Voltage vs. Junction Temperature**

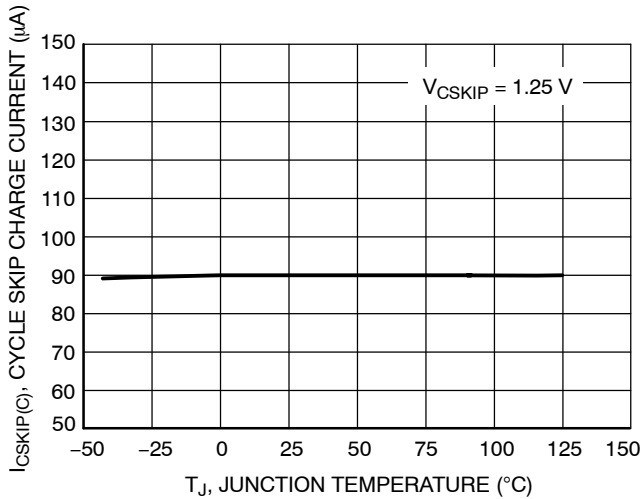


**Figure 16. Current Limit Propagation Delay vs. Junction Temperature**

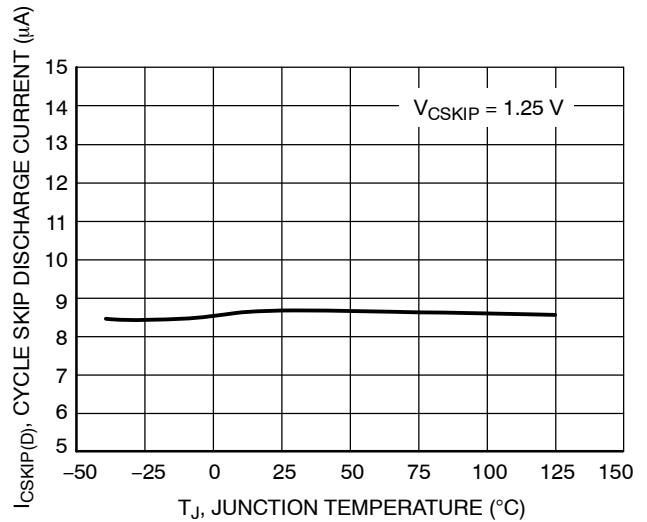


**Figure 17. Leading Edge Blanking Time vs. Junction Temperature**

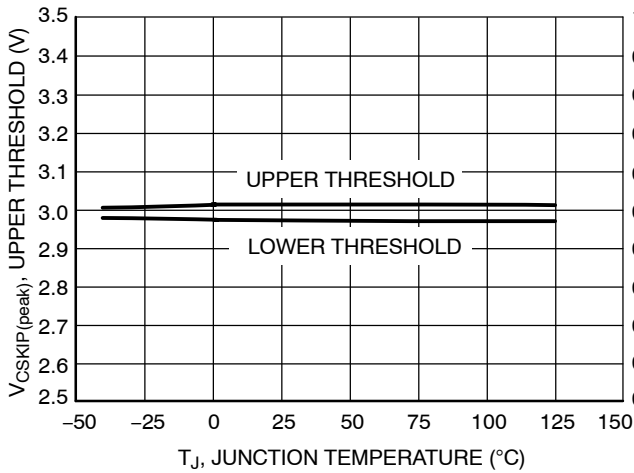
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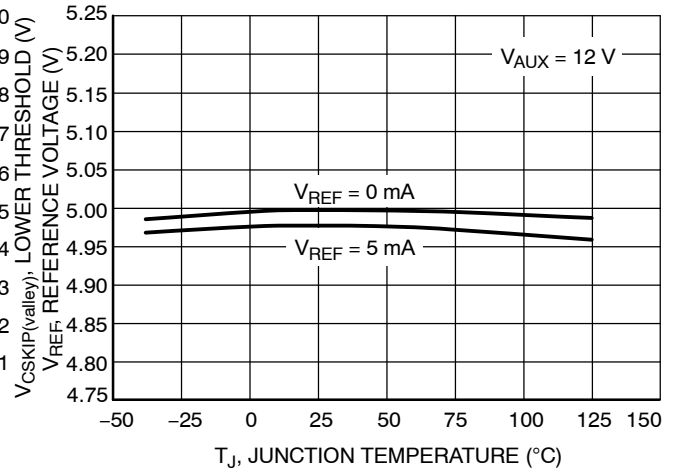
**Figure 18. Cycle Skip Charge Current vs. Junction Temperature**



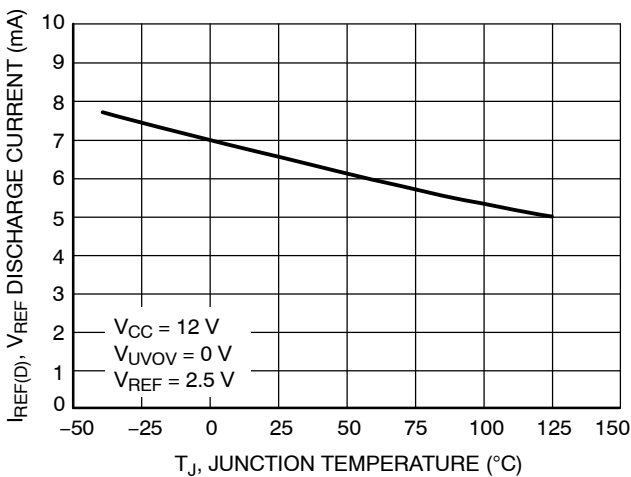
**Figure 19. Cycle Skip Discharge Current vs. Junction Temperature**



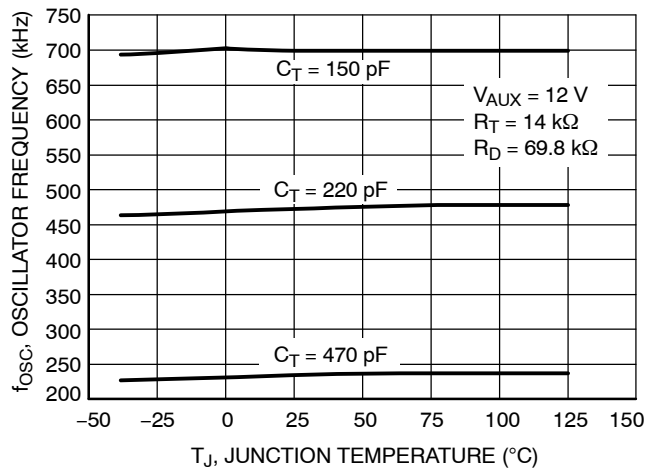
**Figure 20. Cycle Skip Voltage Thresholds vs. Junction Temperature**



**Figure 21. Reference Voltage vs. Junction Temperature**

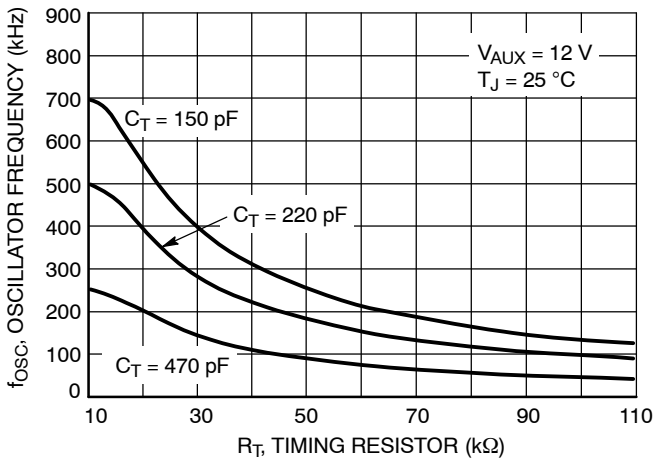


**Figure 22.  $V_{REF}$  Discharge Current vs. Junction Temperature**

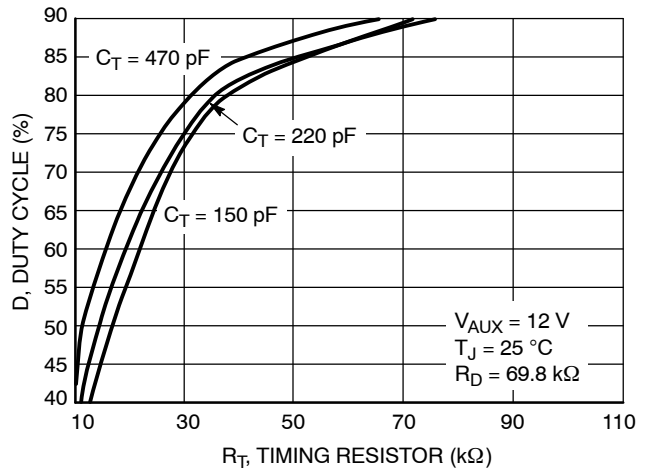


**Figure 23. Oscillator Frequency vs. Junction Temperature**

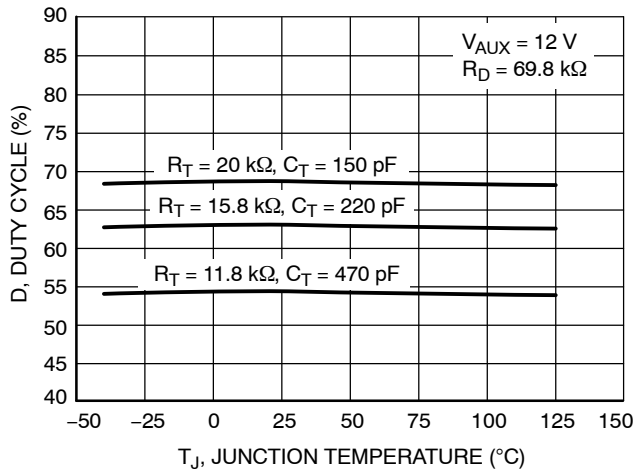
# NCP1562A, NCP1562B



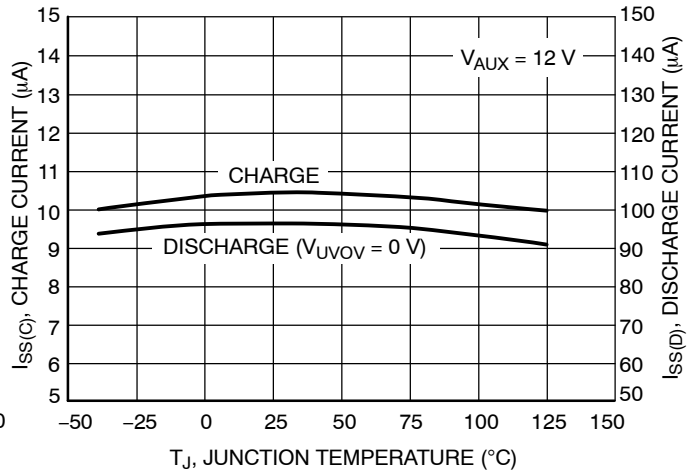
**Figure 24. Oscillator Frequency vs. Timing Resistor**



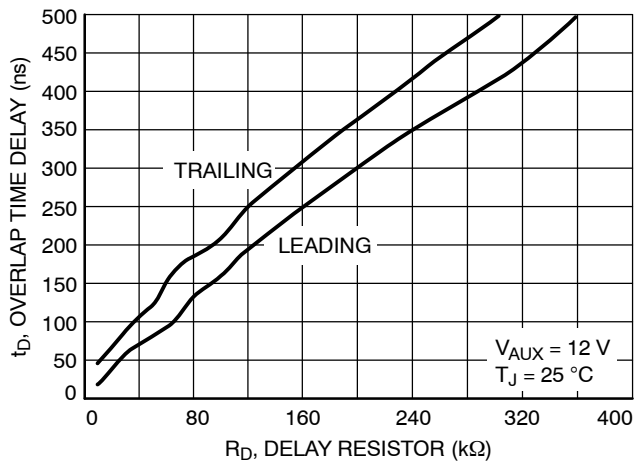
**Figure 25. Duty Cycle vs. Timing Resistor**



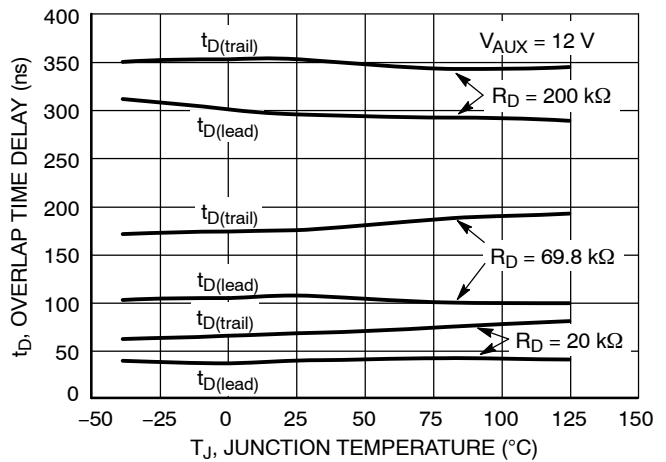
**Figure 26. Duty Cycle vs. Junction Temperature**



**Figure 27. Soft-Start/Stop Charge and Discharge Currents vs. Junction Temperature**

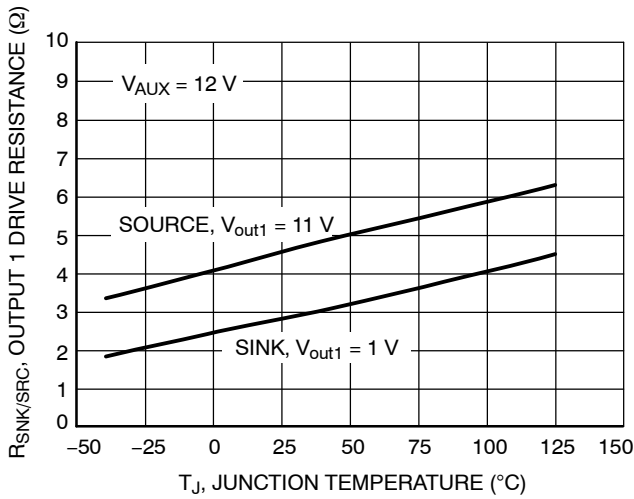


**Figure 28. Overlap Time Delay vs. Delay Resistor**

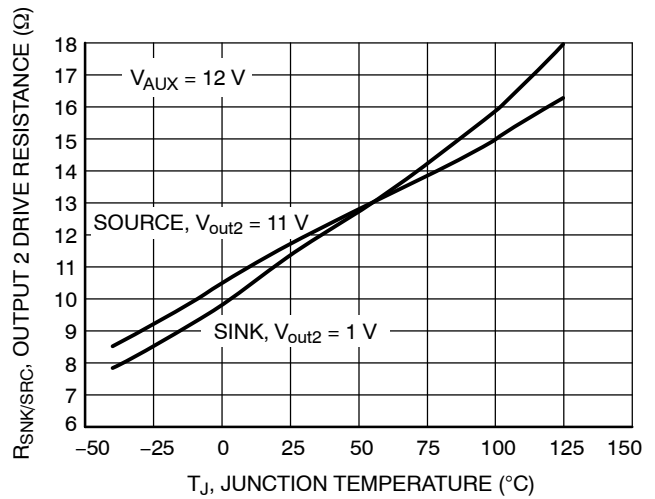


**Figure 29. Overlap Time Delay vs. Junction Temperature**

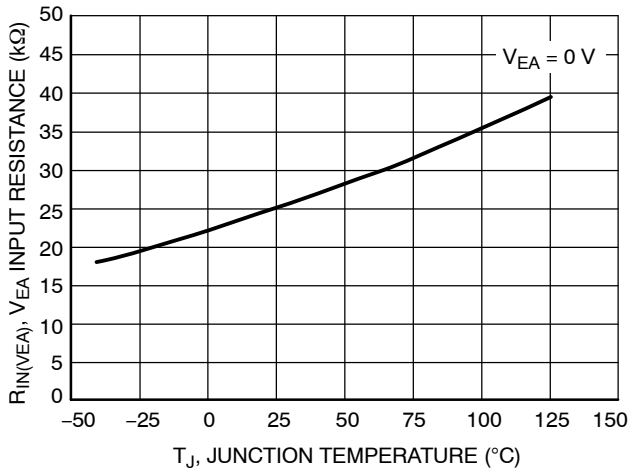
# NCP1562A, NCP1562B



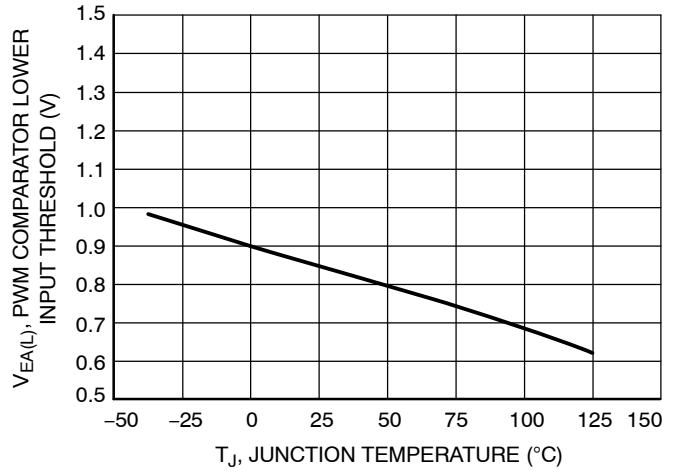
**Figure 30. Output 1 Drive Resistance vs. Junction Temperature**



**Figure 31. Output 2 Drive Resistance vs. Junction Temperature**



**Figure 32.  $V_{EA}$  Input Resistance vs. Junction Temperature**



**Figure 33. PWM Comparator Lower Input Threshold vs. Junction Temperature**

DETAILED OPERATING DESCRIPTION

The NCP1562x is a family of voltage mode controllers designed for dc-dc converters requiring high-efficiency and low parts count. These controllers incorporate two in phase outputs with an adjustable overlap delay. The main output is designed for driving a forward converter primary MOSFET. The secondary output is designed for driving an active clamp circuit MOSFET, a synchronous rectifier on the secondary side, or an asymmetric half bridge circuit.

Two distinctive features of the NCP1562 are the soft-stop and a cycle skip overcurrent detector with a time threshold. The soft-stop powers down the converter in a controlled manner after a fault is detected. The cycle skip timer disables the converter if a continuous overcurrent condition is present.

The NCP1562 reduces component count and system size by incorporating high accuracy on critical specifications such as programmable maximum duty cycle, undervoltage detector and overcurrent threshold. Additional features found in the NCP1562 include line feedforward, bidirectional frequency synchronization up to 1.0 MHz, cycle-by-cycle current limit with leading edge blanking (LEB), independent under and overvoltage detectors, internal startup circuit and soft-start.

SOFT-STOP AND SOFT-START

The NCP1562 incorporates a novel soft-stop and soft-start architecture that combines soft-start and soft-stop functions on a single pin.

Soft-stop reduces the duty cycle until it reaches 0% once a fault is detected. By slowly reducing the duty cycle during power down, the active clamp capacitor ( $C_{clamp}$ ) is discharged. This prevents oscillations between the power transformer and  $C_{clamp}$ , and ensures the converter turns off in a predictable state.

Soft-start slowly increases the duty cycle during power up allowing the controller to gradually reach steady state operation. Combined, both features reduce system stress and power surges.

The duty cycle is controlled by comparing the SS capacitor voltage ( $V_{SS}$ ) to the Feedforward (FF) Ramp. Soft-start or soft-stop is implemented by slowly charging or discharging the capacitor on the SS pin. OUT1 is disabled once the FF Ramp exceeds  $V_{SS}$ . The soft-start charge current is 10  $\mu A$  and the soft-stop discharge current is 100  $\mu A$ , guaranteeing a faster turn OFF time.

The converter enters a soft-stop sequence if an undervoltage, overvoltage, cycle skip or thermal shutdown condition is detected. Once the converter enters the soft-stop mode, it will stay in soft-stop mode until  $V_{SS}$  reaches 0.2 V even if the fault is removed prior to reaching 0.2 V.

The preset 1:10 charge:discharge ratio can be reduced by placing an external resistor between the  $V_{REF}$  and SS pins. The resistor should be sized such that the total charge

current does not exceed 100  $\mu A$ . Otherwise the converter will not be able to complete a soft-stop sequence.

Depending on the converter state, a soft-stop sequence is handled differently to ensure the fastest response time and prevent system malfunction. If a soft-stop sequence starts before  $V_{SS}$  exceeds the maximum voltage clamp of the FF Ramp (typ. 3.0 V) and the PWM Comparator ( $V_{EA}$ ) is not yet controlling the duty cycle, a controlled discharge of  $C_{SS}$  commences immediately, as shown in Figure 34. However, if  $V_{EA}$  is controlling the duty cycle,  $C_{SS}$  is discharged until soft-stop sets a duty cycle equal to the duty cycle set by  $V_{EA}$ . A controlled discharge commences afterwards, as shown in Figure 35. If  $V_{SS}$  exceeds the FF Ramp and the  $V_{EA}$  is not controlling the duty cycle,  $V_{SS}$  is forced to the peak voltage of the FF Ramp, before starting a controlled discharge of  $C_{SS}$ , as shown in Figure 36. The duty cycle set at the beginning of the soft-stop event never exceeds the duty cycle prior to the soft-stop event.

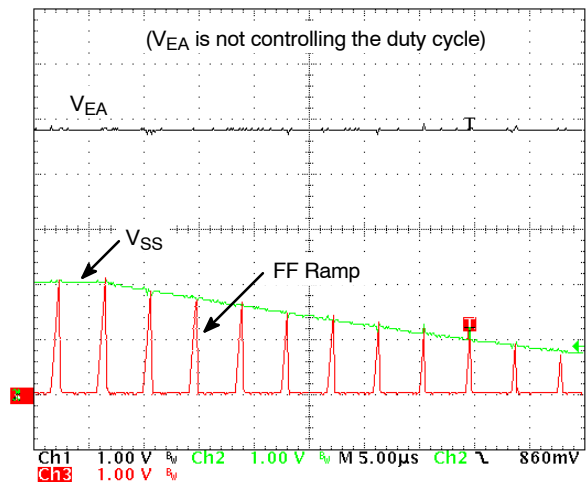


Figure 34. Soft-Stop Before Soft-Start is Complete and  $V_{EA}$  is Open.

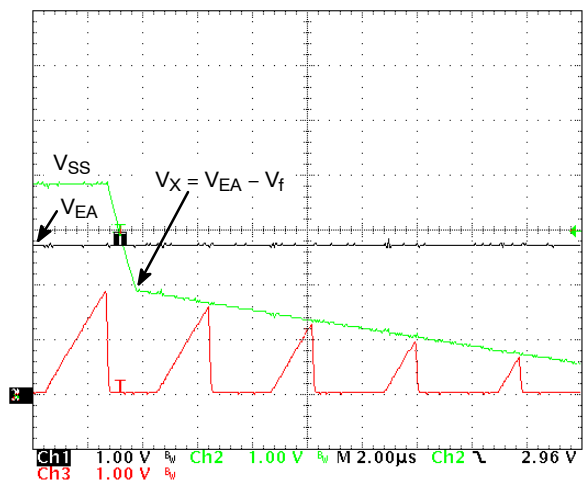
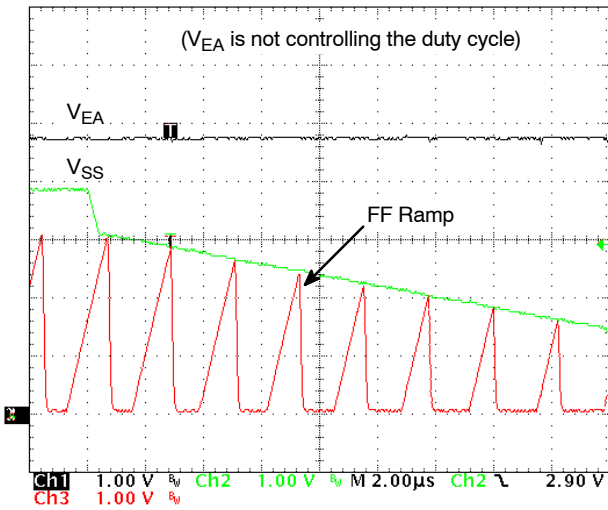


Figure 35. Soft-Stop Behavior when  $V_{EA}$  Controls the Duty Cycle.



**Figure 36. Soft-Stop Behavior After Soft-Start is Complete and  $V_{EA}$  is Open.**

If the voltage on the  $V_{AUX}$  pin reaches  $V_{AUX(off2)}$ ,  $C_{SS}$  is immediately discharged and the outputs are disabled.  $V_{SS}$  should not be pulled up or down externally.

**CURRENT LIMIT**

The NCP1562 has two overcurrent modes, cycle-by-cycle and cycle skip, providing the best protection during momentary and continuous overcurrent conditions.

**Cycle-by-Cycle**

In cycle-by-cycle, the conduction period ends once the voltage on the CS pin reaches the current limit voltage threshold ( $V_{ILIM}$ ). The NCP1562A has a  $V_{ILIM}$  of 0.2 V and the NCP1562B has a  $V_{ILIM}$  of 0.5 V.

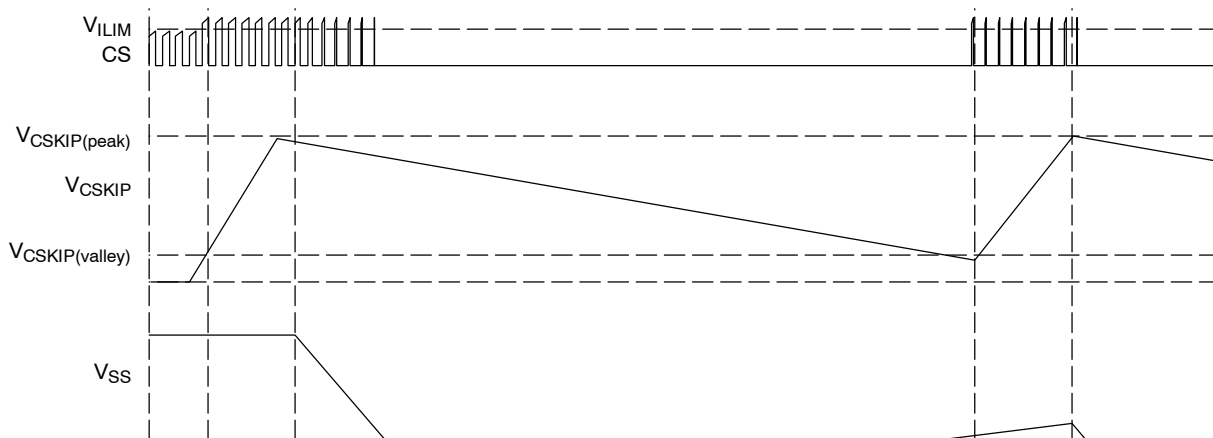
**Cycle Skip**

Traditionally, a voltage on the CS higher than  $V_{ILIM}$  has been used to trigger a cycle skip fault. Unfortunately, the fast response time of modern controllers makes it hard to reach a voltage on the CS pin higher than  $V_{ILIM}$ .

Instead of using a higher voltage threshold to detect a cycle skip fault, the NCP1562 uses a timer. It monitors the current limit comparator and if a continuous cycle-by-cycle current limit condition exists the converter is disabled. The time to disable the converter and the time the converter is disabled are programmed by the capacitor on the CSKIP pin,  $C_{CSKIP}$ .

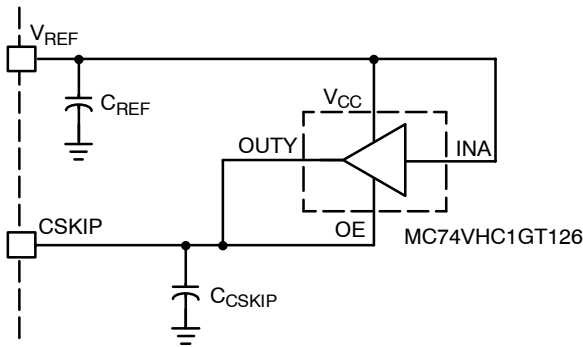
The cycle skip detection circuit charges  $C_{CSKIP}$  with a continuous 100  $\mu$ A current once cycle-by-cycle current limit fault is detected. If the current limit fault persists,  $C_{CSKIP}$  continues to charge until reaching the cycle skip upper threshold ( $V_{CSKIP(peak)}$ ) of 3.0 V. Once reached, the converter enters the soft-stop mode and  $C_{CSKIP}$  is discharged with a constant 10  $\mu$ A current. A new soft-start sequence commences once  $C_{CSKIP}$  reaches the lower cycle skip threshold ( $V_{CSKIP(valley)}$ ) of 0.5 V. If the overcurrent condition is still present, the capacitor starts charging on the next current limit event. Otherwise,  $C_{CSKIP}$  is discharged down to 0 V.

The cycle skip capacitor provides a means of remembering previous overcurrent conditions. If a continuous overcurrent condition is removed before reaching  $V_{CSKIP(peak)}$ ,  $C_{CSKIP}$  starts a controlled discharge. If the continuous overcurrent fault is once again detected before  $C_{CSKIP}$  is completely discharged,  $C_{CSKIP}$  charges from its existing voltage level, taking less time to reach  $V_{CSKIP(peak)}$ . Figure 37 shows operating waveforms during a continuous overcurrent condition. For optimal operation, the cycle skip discharge time should be longer than the soft-stop period.



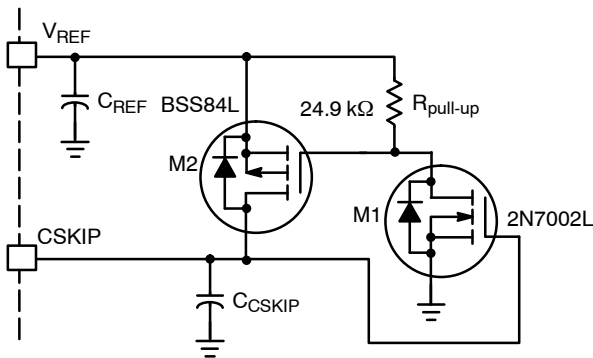
**Figure 37. Cycle Skip Waveforms**

In some instances it may be desired to latch (instead of auto re-start) the NCP1562 after a cycle skip event is detected. This can be easily achieved by adding an external latch. Figures 35 and 36 show an implementation of an integrated and a discrete latch, respectively. In general the circuits work by pulling CSKIP to  $V_{REF}$ , preventing it from reaching  $V_{CSKIP(valley)}$  once the CSKIP voltage reaches the turn on threshold of the latch. The external latch is cleared by bringing the UVOV voltage below  $V_{UV}$  and disabling  $V_{REF}$ .



**Figure 38. External Latch Implemented using onsemi's MiniGate™ Buffer**

The latch in Figure 38 consists of a TTL level tri-state output buffer from onsemi's MiniGate™ family. The enable (OE) and output (OUTY) terminals are connected to CSKIP and the  $V_{CC}$  and INA pins are connected to  $V_{REF}$ . The output of the buffer is in a high impedance mode when OE is low. Once a continuous current limit condition is detected, the CSKIP timer is enabled and CSKIP begins charging. Once the voltage on CSKIP reaches the enable threshold of the buffer, the output of the buffer is pulled to  $V_{REF}$ , latching the CSKIP timer. The OE threshold of the buffer is typically 1.5 V.



**Figure 39. External Latch Implemented using Discrete N and P-Channel MOSFETs**

A latch implemented using discrete N and P-channel MOSFETs is shown in Figure 39. The latch is enabled once the CSKIP voltage reaches the threshold of M1. Once M1 turns on, it pulls low the gate of M2. CSKIP is then pulled to  $V_{REF}$  by M2. It is important to size  $R_{pull-up}$  correctly. If  $R_{pull-up}$  is too big, it will not keep M2 off while  $V_{REF}$  charges. This will cause the controller to latch during initial power-up. In this particular implementation the turn on threshold of M1 is 2 V and  $R_{pull-up}$  is sized to 24.9 k $\Omega$ .

**Leading Edge Blanking**

The current sense signal is prone to leading edge spikes caused by the power switch transitions. The current signal is usually filtered using an RC low-pass filter to avoid premature triggering of the current limit circuit. However, the low pass filter will inevitably change the shape of the current pulse and also add cost and complexity. The NCP1562 uses LEB circuitry that blocks out the first 70 ns (typ) of each current pulse. This removes the leading edge spikes without altering the current waveform. The blanking period is disabled during soft-start as the blanking period may be longer than the startup duty cycle. It is also disabled if the output of the Saturation Comparator is low, indicating that the output is not yet in regulation. This occurs during power up or during an output overload condition.

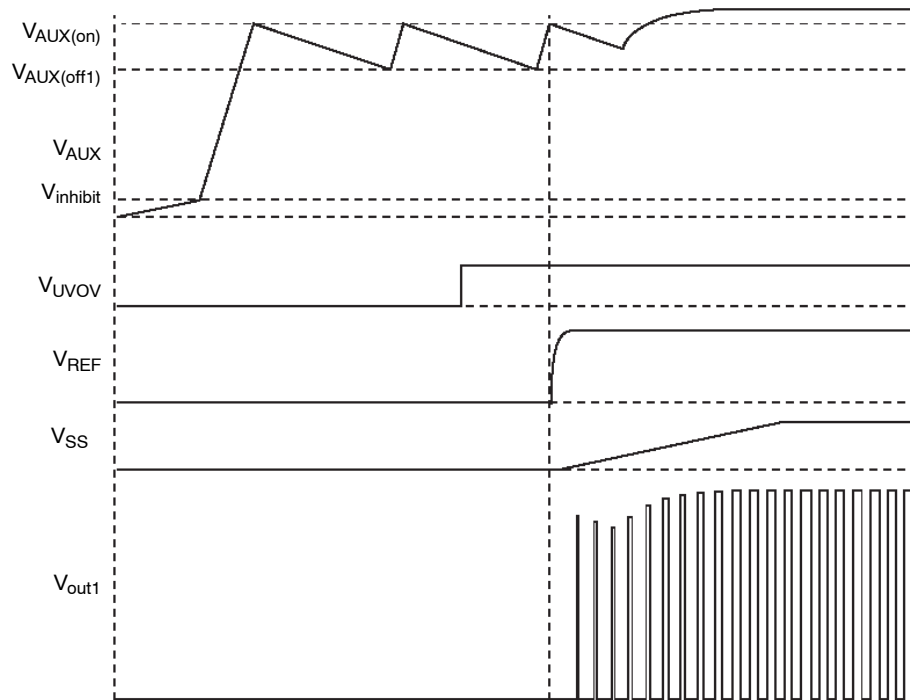
**Supply Voltage and Startup Circuit**

The NCP1562 internal startup regulator eliminates the need for external startup components. In addition, this regulator increases the efficiency of the supply as it uses no power when in the normal mode of operation, but instead uses power supplied by an auxiliary winding. The NCP1562 incorporates an optimized startup circuit that reduces the requirement of the supply capacitor, particularly important in size constrained applications.

The startup regulator consists of a constant current source that supplies current from the input line voltage ( $V_{in}$ ) to the supply capacitor on the  $V_{AUX}$  pin ( $C_{AUX}$ ). The startup current ( $I_{start}$ ) is typically 10 mA.

Once  $C_{AUX}$  is charged to 10.3 V ( $V_{AUX(on)}$ ), the startup regulator is disabled and the outputs are enabled if there are no UV, OV, cycle skip or thermal shutdown faults. The startup regulator remains disabled until the lower voltage threshold ( $V_{AUX(off1)}$ ) of 8.0 V is reached. Once reached, the startup circuit is enabled. If the bias current requirement out of  $C_{AUX}$  is greater than the startup current,  $V_{AUX}$  will discharge until reaching the lower voltage threshold ( $V_{AUX(off2)}$ ) of 7.0 V. Upon reaching  $V_{AUX(off2)}$ , the outputs are disabled. Once the outputs are disabled, the bias current of the IC is reduced, allowing  $V_{AUX}$  to charge back up. This mode of operation allows a dramatic reduction in the size of  $C_{AUX}$  as not all the power required for startup needs to be stored by  $C_{AUX}$ . This mode of operation is known as Dynamic Self Supply (DSS). Figure 40 shows the relationship between  $V_{AUX(on)}$ ,  $V_{AUX(off1)}$ ,  $V_{AUX(off2)}$  and UV. As shown in Figure 40, the outputs are not enabled until the UV fault is removed and  $V_{AUX}$  reaches  $V_{AUX(on)}$ .

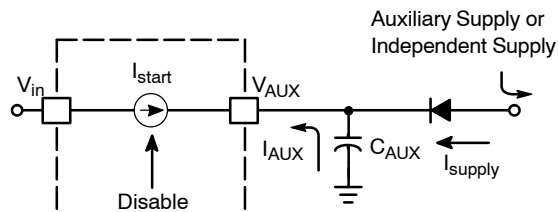
## NCP1562A, NCP1562B



**Figure 40. Startup Circuit Waveforms**

The startup regulator is disabled by biasing  $V_{AUX}$  above  $V_{AUX(on)}$ . This feature allows the NCP1562 to operate from an independent 12 V supply. If operating from an independent supply, the  $V_{in}$  and  $V_{AUX}$  pins should be connected together. The independent supply should maintain  $V_{AUX}$  above  $V_{AUX(on)}$ . Otherwise, the Output Latch will not be SET and the outputs will remain OFF after a fault condition is removed.

The startup circuit sources current into the  $V_{AUX}$  pin. It is recommended to place a diode between  $C_{AUX}$  and the auxiliary supply as shown in Figure 41. This allows the NCP1562 to charge  $C_{AUX}$  while preventing the startup regulator from sourcing current into the auxiliary supply.



**Figure 41. Recommended  $V_{AUX}$  Configuration**

$C_{AUX}$  provides power to the controller while operating in the self-bias or DSS mode. During the converter powerup,  $C_{AUX}$  must be sized such that a  $V_{AUX}$  voltage greater than  $V_{AUX(off2)}$  is maintained while the auxiliary supply voltage is building up. Otherwise,  $V_{AUX}$  will collapse and the controller will turn OFF. Also, the  $V_{AUX}$  discharge time (from 10.3 V to 7.0 V) must be greater than the soft-start charge period to assure the converter turns

ON. The IC bias current, gate charge load on the outputs, and the 5.0 V reference load must be considered to correctly size  $C_{AUX}$ . The current consumption due to external gate charge is calculated using Equation 1.

$$I_{AUX}(\text{gate charge}) = f \cdot Q_G \quad (\text{eq. 1})$$

where,  $f$  is the operating frequency and  $Q_G$  is the gate charge.

An internal supervisory circuit monitors  $V_{AUX}$  and prevents excessive power dissipation if the  $V_{AUX}$  pin is accidentally shorted. While  $V_{AUX}$  is below 1.2 V, the startup circuit is disabled and a current source ( $I_{inhibit}$ ) charges  $V_{AUX}$  with a minimum current of 50  $\mu\text{A}$ . Once  $V_{AUX}$  reaches 1.2 V the startup circuit is enabled. Therefore it is imperative that  $V_{AUX}$  is not loaded (driver, resistor divider, etc.) with more than 50  $\mu\text{A}$  while  $V_{AUX}$  is below 1.2 V. Otherwise,  $V_{AUX}$  will not charge. If a load greater than 50  $\mu\text{A}$  is present, a resistor can be placed between the  $V_{in}$  and  $V_{AUX}$  pins to help charge  $V_{AUX}$  to 1.2 V.

The startup circuit is rated at a maximum voltage of 100 V. If the device operates in the DSS mode, power dissipation should be controlled to avoid exceeding the maximum power dissipation of the controller. If dissipation on the controller is excessive, a resistor can be placed in series with the  $V_{in}$  pin. This will reduce power dissipation on the controller and transfer it to the series resistor.

### Line Under/Overvoltage Detector

The same pin is used for both line undervoltage (UV) and overvoltage (OV) detection using a novel architecture

(patent pending). This architecture allows both the UV and OV levels to be set independently. Both the UV and OV detectors have a 100 mV hysteresis.

The line voltage is sampled using a resistor divider as shown in Figure 42.

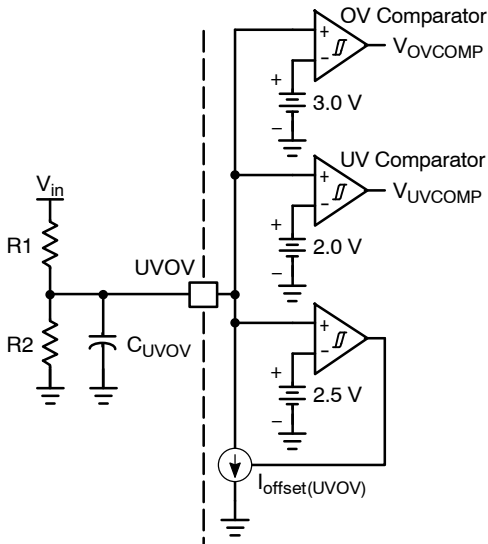


Figure 42. Line UVOV Detectors

A UV condition exists if the UVOV voltage is below  $V_{UV}$ , typically 2.0 V. The ratio of R1 and R2 determines the UV turn threshold. Once the UVOV voltage exceeds 2.5 V, an internal current source ( $I_{offset(UVOV)}$ ) sinks 50  $\mu$ A into the UVOV pin. This will clamp the UVOV voltage at 2.5 V while the current across R1 is less than  $I_{offset(UVOV)}$ . If the input voltage continues to increase, the 50  $\mu$ A source will be overridden and the voltage at the UVOV pin will increase. An OV condition exists if the UVOV voltage exceeds  $V_{OV}$ , typically 3.0 V. Figure 43 shows the relationship between UVOV and  $V_{in}$ .

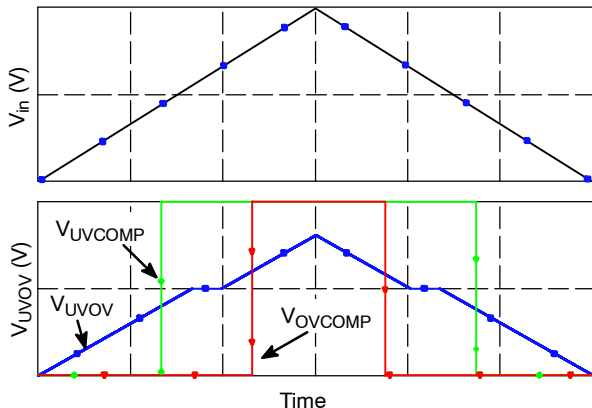


Figure 43. UVOV Detectors Typical Waveforms

While the internal current source is disabled, the UVOV voltage is solely determined by the ratio of R1 and R2. The input voltage at which the converter turns ON is given by

Equation 1. Once the internal current source is enabled, the absolute value of R1 together with the ratio of R1 and R2 determine the turn OFF threshold as shown in Equation 2.

$$V_{in(UV)} = V_{UV} \times \frac{(R1 + R2)}{R2} \quad (\text{eq. 1})$$

$$V_{in(OV)} = V_{OV} \frac{(R1 + R2)}{R2} + (\text{offset(UVOV)} \times R1) \quad (\text{eq. 2})$$

The undervoltage threshold is trimmed during manufacturing to obtain  $\pm 3\%$  accuracy allowing a tighter power stage design.

Once the line voltage is within the operating range, and  $V_{AUX}$  reaches  $V_{AUX(on)}$ , the outputs are enabled and a soft-start sequence commences. If a UV or OV fault is detected afterwards, the converter enters a soft-stop mode.

A small capacitor is required ( $>1000$  pF) from the UVOV pin to GND to prevent oscillation of the UVOV pin and filter line transients.

**Line Feedforward**

The NCP1562 incorporates line feedforward (FF) to limit the maximum volt-second product. It is the line voltage times the ON time. This limit prevent saturation of the transformer in forward and flyback topologies. Another advantage of feedforward is a controller frequency gain independent of line voltage. A constant gain facilitates frequency compensation of the converter.

Feedforward is implemented by generating a ramp proportional to  $V_{in}$  and comparing it to the error signal. The error signal solely controls the duty cycle while the input voltage is fixed. If the line voltage changes, the FF Ramp slope changes and duty cycle is immediately adjusted instead of waiting for the change to propagate around the feedback loop and be reflected back on the error signal.

The FF Ramp is generated with an R-C ( $R_{FF}C_{FF}$ ) divider from the input line as shown in Figure 44. The divider is selected such that the FF Ramp reaches 3.0 V in the desired maximum ON time. The FF Ramp terminates by effectively grounding  $C_{FF}$  during the converter OFF time. This can be triggered by the FF Ramp reaching 3.0 V, or any other condition that limits the duty cycle.

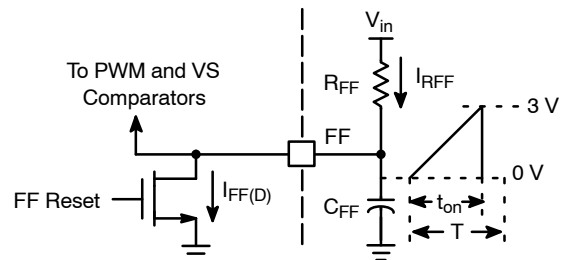


Figure 44. Feed Forward Ramp Generation

The FF pin is effectively grounded during power or during standby mode to prevent the FF pin from charging up to  $V_{in}$ .

The minimum value of  $R_{FF}$  is determined by the FF Ramp discharge current ( $I_{FF(D)}$ ). The current through  $R_{FF}$  ( $I_{RFF}$ ) should be at least ten times smaller than  $I_{FF(D)}$  for a sharp FF Ramp transition. Equations 3 and 4 are used to determine  $R_{FF}$  and  $C_{FF}$ .

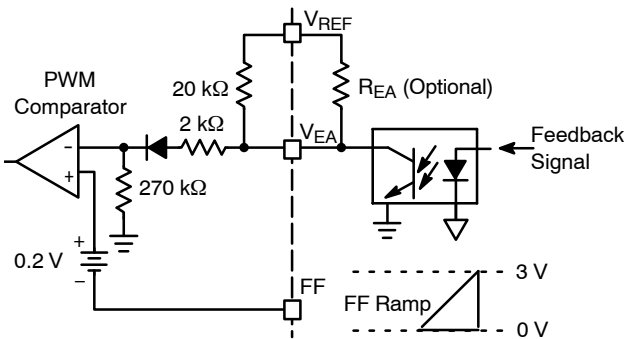
$$\frac{V_{in}}{0.1 \times I_{FF(D)}} \leq R_{FF} \quad (\text{eq. 3})$$

$$C_{FF} = \frac{D}{\ln\left(\frac{V_{in}}{V_{in}-3V}\right) \times f \times R_{FF}} \quad (\text{eq. 4})$$

where,  $f$  is the operating frequency. It is recommended to bias the FF circuit with enough current to provide good noise immunity.

**PWM Comparator**

In steady state operation, the PWM Comparator adjusts the duty cycle by comparing the error signal to the FF Ramp. The error signal is fed into the  $V_{EA}$  pin. The  $V_{EA}$  pin can be driven directly with an optocoupler without the need of an external pullup resistor as shown in Figure 45. In some instances, it may be required to have a pullup resistor smaller than the internal resistor ( $R4$ ) to adjust the gain of the isolation stage. This is easily accomplished by connecting an external resistor ( $R_{EA}$ ) in parallel with  $R4$ .  $R_{EA}$  is connected between the  $V_{REF}$  and  $V_{EA}$  pins. The effective pullup resistance is the parallel combination of  $R4$  and  $R_{EA}$ .



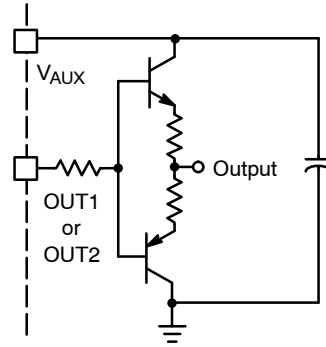
**Figure 45. Optocoupler Driving  $V_{EA}$  Input**

The drive of the  $V_{EA}$  pin is simplified by internally incorporating a series diode and resistor. The series diode provides a 0.7 V offset between the  $V_{EA}$  input and the PWM Comparator inverting input. It allows reaching zero duty cycle without the need of pulling the  $V_{EA}$  pin all the way to GND. The outputs are enabled if the  $V_{EA}$  voltage is approximately 0.5 V above the valley of the FF Ramp.

**Outputs**

The NCP1562 has two in-phase output drivers with an adjustable overlap delay ( $t_D$ ). The main output, OUT1, has a source resistance of 4.0  $\Omega$  (typ) and a sink resistance of 2.5  $\Omega$  (typ). The secondary output, OUT2, has a source and a sink resistance of 12  $\Omega$  (typ). OUT1 is rated at a maximum of 2.0 A and OUT2 is rated at a maximum of

1.0 A. If a higher drive capability is required, an external driver stage can be easily added as shown in Figure 46.



**Figure 46. Discrete Boost Drive Stage**

OUT1 drives the main MOSFET, and OUT2 drives a low side P-Channel active clamp MOSFET. A high side N-Channel active clamp MOSFET or a synchronous rectifier can also be driven by inverting OUT2. OUT2 is purposely sized smaller than OUT1 because the active clamp MOSFET only sees the magnetizing current. Therefore, a smaller active clamp MOSFET with less input capacitance can be used compared to the main switch.

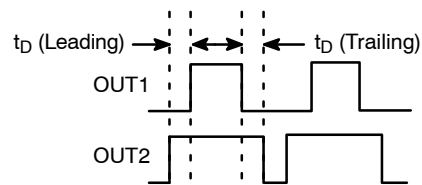
Once  $V_{AUX}$  reaches  $V_{AUX(on)}$  (typically 10.3 V), the internal startup circuit is disabled and the outputs are enabled if no faults are present. Otherwise, the outputs remain disabled until the fault is removed and  $V_{AUX}$  reaches  $V_{AUX(on)}$ . The outputs are disabled after a soft-stop sequence if  $V_{AUX}$  is below  $V_{AUX(on)}$  or if  $V_{AUX}$  reaches 7.0 V.

The outputs are biased directly from  $V_{AUX}$  and their high state voltage is approximately  $V_{AUX}$ . Therefore, the auxiliary supply voltage should not exceed the maximum gate voltage of the main or active clamp MOSFET.

The high current drive capability of the outputs will generate inductance-induced spikes if inductance is not reduced on the outputs. This can be done by reducing the connection length between the drivers and their loads and using wide connections.

**Overlap Delay**

The overlap delay prevents simultaneous conduction of the main and active clamp MOSFETs. The secondary output, OUT2, precedes OUT1 during a low to high transition and trails OUT1 during a high to low transition. Figure 47 shows the relationship between OUT1 and OUT2.



**Figure 47. Output Timing Diagram**

The output overlap delay is adjusted by connecting a resistor,  $R_D$ , from the  $t_D$  pin to ground. The overlap delay is proportional to  $R_D$ . A minimum delay of 20 ns is obtained by grounding the  $t_D$  pin.

The leading delay is purposely made longer than the trailing delay. This allows the user to optimize the delay for the turn on transition of the main switch and ensures the active clamp switch always exhibits zero volt switching.

**Analog and Power Ground (PGND)**

The NCP1562 has an analog ground, GND, and a power ground, PGND, terminal. GND is used for analog connections such as  $V_{REF}$ ,  $R_T C_T$ , feedforward among others. PGND is used for high current connections such as the internal output drivers. It is recommended to have independent analog and power ground planes and connect them at a single point, preferably at the ground terminal of the system. This will prevent high current flowing on PGND from injecting noise in GND. The PGND connection should be as short and wide as possible to reduce inductance-induced spikes.

**Oscillator**

The oscillator frequency and maximum duty cycle are set by an  $R_T C_T$  divider from  $V_{REF}$  as shown in Figure 48. A 500  $\mu$ A current source ( $I_{RTCT}$ ) discharges the timing capacitor ( $C_T$ ) upon reaching its peak threshold ( $V_{RTCT(peak)}$ ), typically 3.0 V. Once  $C_T$  reaches its valley

voltage ( $V_{RTCT(valley)}$ ), typically 2.0 V,  $I_{RTCT}$  turns OFF allowing  $C_T$  to charge back up through  $R_T$ . The resulting waveform on the RTCT pin has a sawtooth like shape.

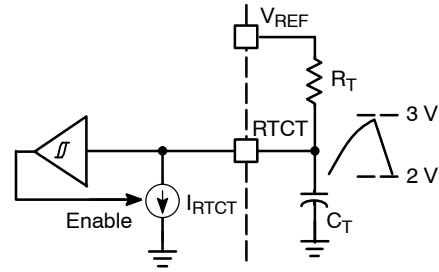


Figure 48. Oscillator Configuration

OUT2 is set high once  $V_{RTCT(valley)}$  is reached, followed by OUT1 delayed by the overlap delay. Once  $V_{RTCT(peak)}$  is reached, OUT1 goes low, followed by OUT2 delayed by  $t_D$ .

The duty cycle is the  $C_T$  charge time ( $t_{RTCT(C)}$ ) minus the overlap delay over the total charge and discharge ( $t_{RTCT(D)}$ ) times. The charge and discharge times are calculated using Equations 5 and 6. However, these equations are an approximation as they do not take into account the propagation delays of the internal comparator.

$$t_{RTCT(C)} = R_T C_T \times \ln\left(\frac{V_{RTCT(valley)} - V_{REF}}{V_{RTCT(peak)} - V_{REF}}\right) \quad (\text{eq. 5})$$

$$t_{RTCT(D)} = R_T C_T \times \ln\left(\frac{(I_{RTCT} \times R_T) + V_{RTCT(peak)} - V_{REF}}{(I_{RTCT} \times R_T) + V_{RTCT(valley)} - V_{REF}}\right) \quad (\text{eq. 6})$$

The duty cycle, D, is given by Equation 7.

$$D = \frac{t_{RTCT(C)} - t_D}{t_{RTCT(C)} + t_{RTCT(D)}} \quad (\text{eq. 7})$$

$$D = \frac{\ln\left(\frac{V_{RTCT(valley)} - V_{REF}}{V_{RTCT(peak)} - V_{REF}}\right) - \frac{t_D}{R_T C_T}}{\ln\left(\frac{V_{RTCT(valley)} - V_{REF}}{V_{RTCT(peak)} - V_{REF}}\right) \times \frac{(I_{RTCT} \times R_T) + V_{RTCT(peak)} - V_{REF}}{(I_{RTCT} \times R_T) + V_{RTCT(valley)} - V_{REF}}}$$

It can be observed that D is set by  $R_T$ ,  $C_T$  and  $t_D$ . This equation has two variables and can be solved iteratively. In general, the time delay is a small portion of the ON time and can be ignored as a first approximation.  $R_T$  is then selected

Substituting Equations 5, 6, and 7, and after a little algebraic manipulation and replacing values, it simplifies to:

to achieve a given duty cycle. Once the  $R_T$  is selected,  $C_T$  is chosen to obtain the desired operating frequency using Equation 9.

$$f = \frac{1}{R_T C_T \times \ln\left(\frac{V_{RTCT(valley)} - V_{REF}}{V_{RTCT(peak)} - V_{REF}}\right) \times \frac{(I_{RTCT} \times R_T) + V_{RTCT(peak)} - V_{REF}}{(I_{RTCT} \times R_T) + V_{RTCT(valley)} - V_{REF}}}$$

Figures 23 through 26 show the frequency and duty cycle variation vs  $R_T$  for several  $C_T$  values.  $R_T$  should not be less than 6.0 k $\Omega$ . Otherwise, the  $R_T C_T$  charge current will exceed the pulldown current and the oscillator will be in an undefined state.

**Synchronization**

A proprietary bidirectional frequency synchronization architecture allows multiple NCP1562 to synchronize in a master-slave configuration. It can synchronize to frequencies above or below the free running frequency.

The SYNC pin is in a high impedance mode during the charging of the RTCT Ramp. In this period the oscillator accepts an external SYNC pulse. If no pulse is detected upon reaching the peak of the RTCT Ramp, a 100 ns SYNC pulse is generated. The SYNC pulse is generated by internally pulling the SYNC pin to  $V_{REF}$ . The peak voltage of the SYNC pin is typically 4.3 V. Once the 100 ns timer expires, the pin goes back into a high impedance mode and an external resistor is required for pulldown as shown in Figure 49.

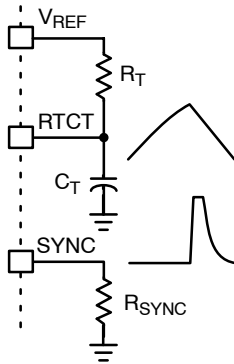


Figure 49. SYNC Pulse

The slew rate of the sync pin is determined by the pin capacitance and external pulldown resistor. The maximum source current of the SYNC pin is 1.0 mA. The resistor is sized to allow the SYNC pin to discharge before the start of the next cycle.

If an external pulse is received on the SYNC pin before the internal pulse is generated, the controller enters the slave mode of operation. Once operation in slave mode commences,  $C_T$  begins discharging and the  $R_T C_T$  Ramp upper threshold is increased to 4.0 V.

If a controller in slave mode does not receive a sync pulse before reaching the  $R_T C_T$  Ramp peak voltage (4.0 V), the upper threshold is reset back to 3.0 V and the converter reverts to operation in master mode. To guarantee the converter stays in slave mode, the minimum clock period of the master controller has to be less than the  $R_T C_T$  charge time from 2.0 V to 4.0 V.

Two NCP1562's are synchronized by connecting their SYNC pins together. The first device that generates a sync pulse during powerup becomes the master. A diode connected as shown in Figure 50 can be used to permanently set one controller as the master. The diode prevents the master from receiving the SYNC pulse of the slave controller.

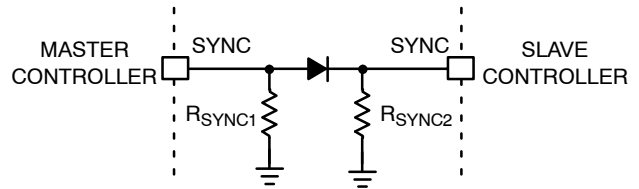


Figure 50. Master-Slave Configuration

**5.0 V Reference**

The NCP1562 has a precision 5.0 V reference output. It is a buffered version of the internal reference. The 5.0 V reference is biased directly from  $V_{AUX}$  and it can supply up to 5.0 mA. Load regulation is 50 mV and line regulation is 100 mV within the specified operating range.

It is required to bypass the reference with a capacitor. The capacitor is used for compensation of the internal regulator and high frequency noise filtering. The capacitor should be placed across the  $V_{REF}$  and GND pins. In most applications a 0.1  $\mu F$  will suffice. A bigger capacitor may be required to reduce the voltage ripple caused by the oscillator current. The recommended capacitor range is between 0.047  $\mu F$  and 1.0  $\mu F$ .

During powerup, the 5.0 V reference is enabled once  $V_{AUX}$  reaches  $V_{AUX(on)}$  and a UV fault is not present. Otherwise, the reference is enabled once the UV fault is removed and  $V_{AUX}$  reaches  $V_{AUX(on)}$ .

Once a UV fault is detected after the reference has been enabled, the reference is disabled after the soft-stop sequence is complete if the UV fault is still present. If the UV fault is removed before soft-stop is complete, the reference is not disabled.

**Application Information**

onsemi provides an electronic design tool, a demonstration board and an application note to facilitate design of the NCP1562 and reduce development cycle time. All the tools can be downloaded or ordered at [www.onsemi.com](http://www.onsemi.com).

The electronic design tool allows the user to easily determine most of the system parameters of an active clamp forward converter. The tool evaluates the power and active clamp stages as well as the frequency response of the system. The tool is used to design a converter for a 48 V telecom system. The converter delivers 100 W at 3.3 V. The circuit schematic is shown in Figure 51. The converter design is described in Application Note AND8273/D.



## NCP1562A, NCP1562B

### ORDERING INFORMATION

Device	Package	Current Limit	Shipping†
NCP1562ADBR2G	TSSOP-16 (Pb-Free)	200 mV	2500 Tape & Reel
NCP1562ADR2G	SO-16 (Pb-Free)	200 mV	2,500 Tape & Reel
NCP1562BDR2G	SO-16 (Pb-Free)	500 mV	2,500 Tape & Reel

### DISCONTINUED (Note 6)

NCP1562BDBR2G	TSSOP-16 (Pb-Free)	500 mV	2,500 Tape & Reel
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† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

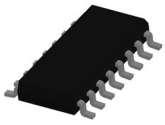
6. **DISCONTINUED:** This device is not available. Please contact your **onsemi** representative for information. The most current information on this device may be available on [www.onsemi.com](http://www.onsemi.com).

# NCP1562A, NCP1562B

## REVISION HISTORY

Revision	Description of Changes	Date
6	NCP1562BDBR2G OPN Marked as Discontinued + Rebranded the Data Sheet to <b>onsemi</b> format.	01/22/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

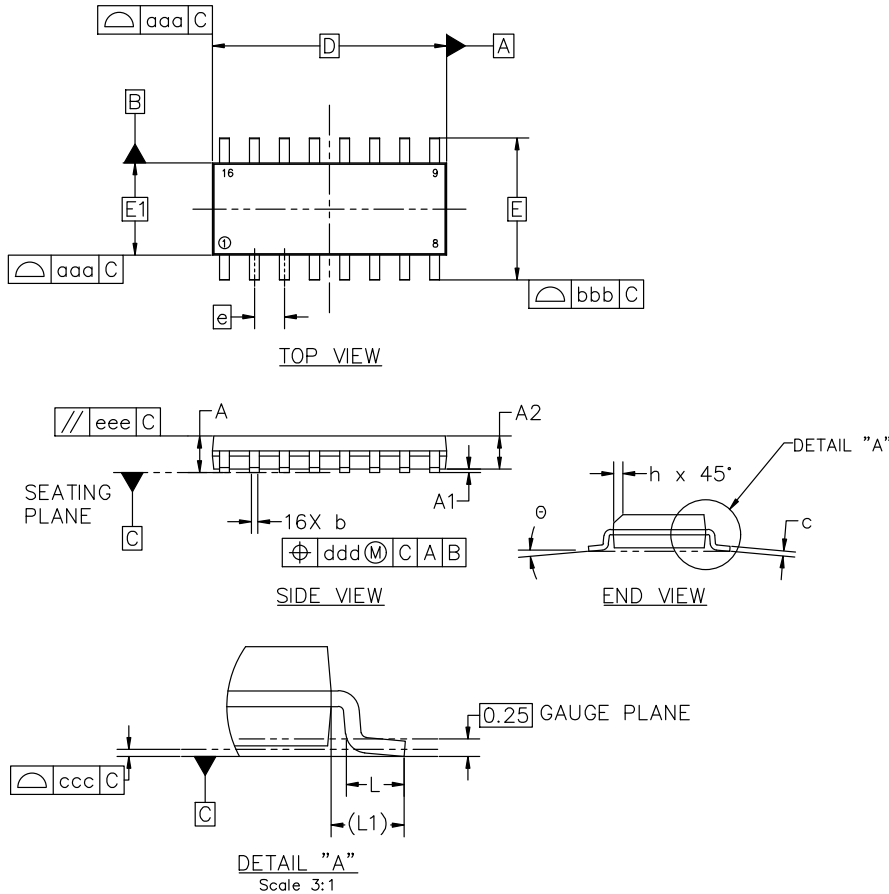


**SOIC-16 9.90x3.90x1.37 1.27P**  
**CASE 751B**  
**ISSUE M**

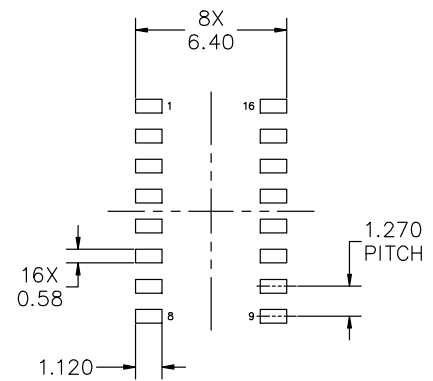
DATE 18 OCT 2024

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	---	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	---	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D

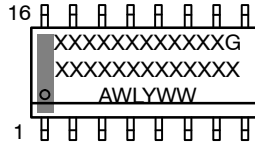
<b>DOCUMENT NUMBER:</b>	<b>98ASB42566B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SOIC-16 9.90X3.90X1.37 1.27P</b>	<b>PAGE 1 OF 2</b>

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**SOIC-16 9.90x3.90x1.37 1.27P**  
**CASE 751B**  
**ISSUE M**

DATE 18 OCT 2024

**GENERIC  
MARKING DIAGRAM\***



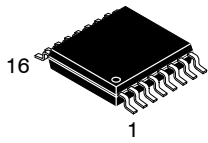
XXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

<p><b>STYLE 1:</b></p> <p>PIN 1. COLLECTOR  2. BASE  3. EMITTER  4. NO CONNECTION  5. EMITTER  6. BASE  7. COLLECTOR  8. COLLECTOR  9. BASE  10. EMITTER  11. NO CONNECTION  12. EMITTER  13. BASE  14. COLLECTOR  15. EMITTER  16. COLLECTOR</p>	<p><b>STYLE 2:</b></p> <p>PIN 1. CATHODE  2. ANODE  3. NO CONNECTION  4. CATHODE  5. CATHODE  6. NO CONNECTION  7. ANODE  8. CATHODE  9. CATHODE  10. ANODE  11. NO CONNECTION  12. CATHODE  13. CATHODE  14. NO CONNECTION  15. ANODE  16. CATHODE</p>	<p><b>STYLE 3:</b></p> <p>PIN 1. COLLECTOR, DYE #1  2. BASE, #1  3. EMITTER, #1  4. COLLECTOR, #1  5. COLLECTOR, #2  6. BASE, #2  7. EMITTER, #2  8. COLLECTOR, #2  9. COLLECTOR, #3  10. BASE, #3  11. EMITTER, #3  12. COLLECTOR, #3  13. COLLECTOR, #4  14. BASE, #4  15. EMITTER, #4  16. COLLECTOR, #4</p>	<p><b>STYLE 4:</b></p> <p>PIN 1. COLLECTOR, DYE #1  2. COLLECTOR, #1  3. COLLECTOR, #2  4. COLLECTOR, #2  5. COLLECTOR, #3  6. COLLECTOR, #3  7. COLLECTOR, #4  8. COLLECTOR, #4  9. BASE, #4  10. EMITTER, #4  11. BASE, #3  12. EMITTER, #3  13. BASE, #2  14. EMITTER, #2  15. BASE, #1  16. EMITTER, #1</p>
<p><b>STYLE 5:</b></p> <p>PIN 1. DRAIN, DYE #1  2. DRAIN, #1  3. DRAIN, #2  4. DRAIN, #2  5. DRAIN, #3  6. DRAIN, #3  7. DRAIN, #4  8. DRAIN, #4  9. GATE, #4  10. SOURCE, #4  11. GATE, #3  12. SOURCE, #3  13. GATE, #2  14. SOURCE, #2  15. GATE, #1  16. SOURCE, #1</p>	<p><b>STYLE 6:</b></p> <p>PIN 1. CATHODE  2. CATHODE  3. CATHODE  4. CATHODE  5. CATHODE  6. CATHODE  7. CATHODE  8. CATHODE  9. ANODE  10. ANODE  11. ANODE  12. ANODE  13. ANODE  14. ANODE  15. ANODE  16. ANODE</p>	<p><b>STYLE 7:</b></p> <p>PIN 1. SOURCE N-CH  2. COMMON DRAIN (OUTPUT)  3. COMMON DRAIN (OUTPUT)  4. GATE P-CH  5. COMMON DRAIN (OUTPUT)  6. COMMON DRAIN (OUTPUT)  7. COMMON DRAIN (OUTPUT)  8. SOURCE P-CH  9. SOURCE P-CH  10. COMMON DRAIN (OUTPUT)  11. COMMON DRAIN (OUTPUT)  12. COMMON DRAIN (OUTPUT)  13. GATE N-CH  14. COMMON DRAIN (OUTPUT)  15. COMMON DRAIN (OUTPUT)  16. SOURCE N-CH</p>	

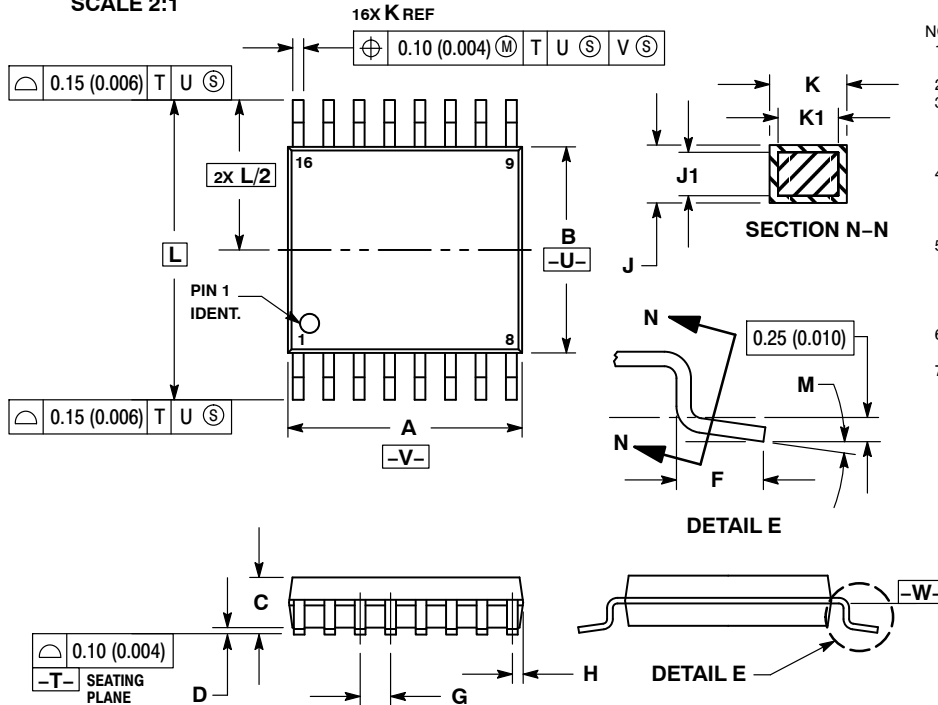
<b>DOCUMENT NUMBER:</b>	<b>98ASB42566B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SOIC-16 9.90X3.90X1.37 1.27P</b>	<b>PAGE 2 OF 2</b>

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TSSOP-16 WB  
CASE 948F  
ISSUE B

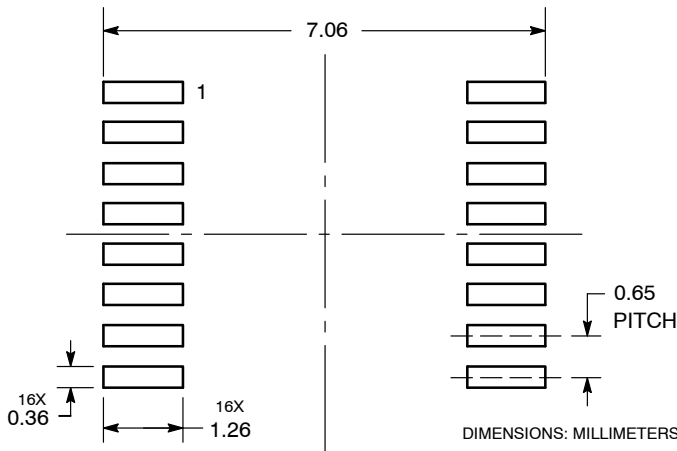
DATE 19 OCT 2006



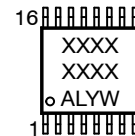
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

RECOMMENDED  
SOLDERING FOOTPRINT\*



GENERIC  
MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- G or ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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