

# Low Power Offline Constant Current PWM Current-Mode Controller with/without High Voltage Startup Current Source

## NCP1361, NCP1366

The NCP1361/66 offers a new solution targeting output power levels from a few watts up to 20 W in a universal-mains flyback application. Due to a novel method this new controller offers a primary-side constant current control, saving secondary-side components to perform current regulation.

The NCP1361/66 operates in valley-lockout quasi-resonant peak current mode control mode at nominal load to provide high efficiency. When the secondary-side power starts diminishing, the switching frequency naturally increases until a voltage-controlled oscillator (VCO) takes the lead, synchronizing the MOSFET turn-on in a drain-source voltage valley. The frequency is thus reduced by stepping into successive valleys until the number 4 is reached. Beyond this point, the frequency is linearly decreased in valley-switching mode until a minimum is hit. Valley lockout during the first four drain-source valleys prevents erratic discrete jumps and provides good efficiency in lighter load situations.

### Features

- ±10% Current Regulation
- 560 V Startup Current Source
- No Frequency Clamp, 80 or 110 kHz Maximum Switching Frequency Options
- Quasi-Resonant Operation with Valley Switching Operation
- Fixed Peak Current & Deep Frequency Foldback @ Light Load Operation
- External Constant Voltage Feedback Adjustment
- Cycle by Cycle Peak Current Limit
- Built-In Soft-Start
- Over & Under Output Voltage Protection
- Wide Operation  $V_{CC}$  Range (up to 28 V)
- Low Start-up Current (2.5  $\mu$ A typ.) with NCP1361
- Clamped Gate-drive Output for MOSFET
- $CS$  &  $V_s/ZCD$  pin Short and Open Protection
- Internal Temperature Shutdown
- Less than 30 mW No-Load Performance at High Line with NCP1366 Version
- These are Pb-Free Devices

### Typical Applications

- Low power ac-dc Adapters for Chargers
- Ac-dc USB chargers for Cell Phones, Tablets and Cameras

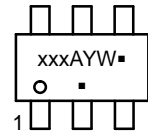
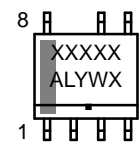


SOIC-7  
CASE 751U



TSOP-6  
CASE 318G

### MARKING DIAGRAMS



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information on page 25 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 25.

# NCP1361, NCP1366

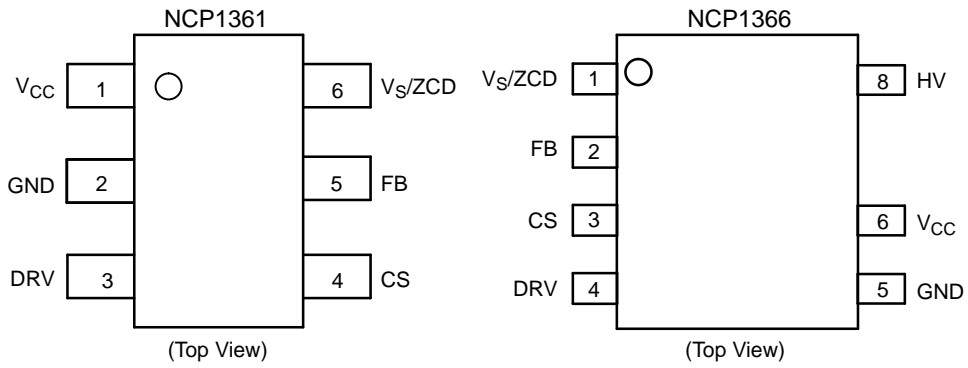


Figure 1. Pin Connections

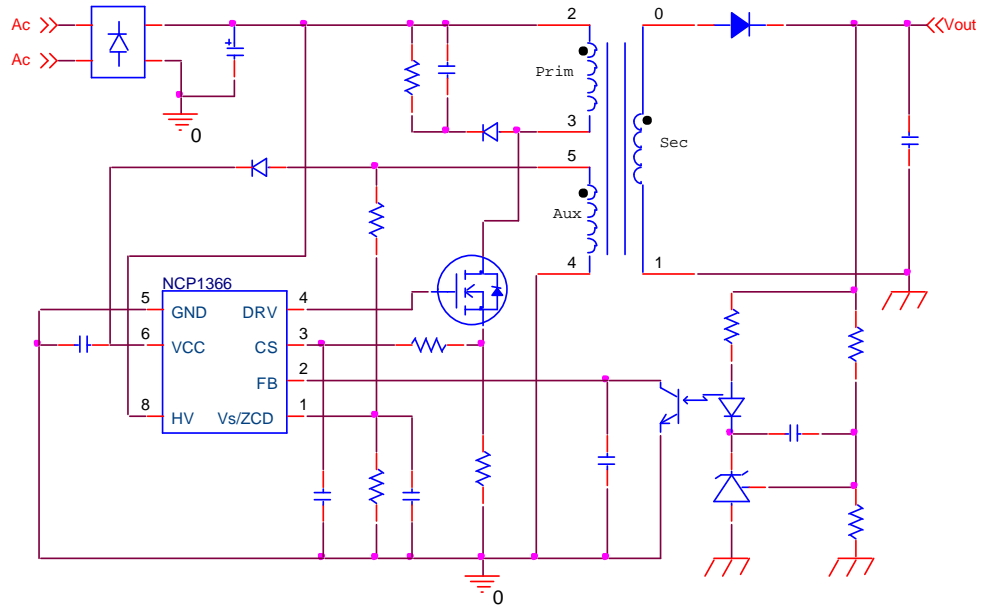


Figure 2. NCP1366 Typical Application Circuit

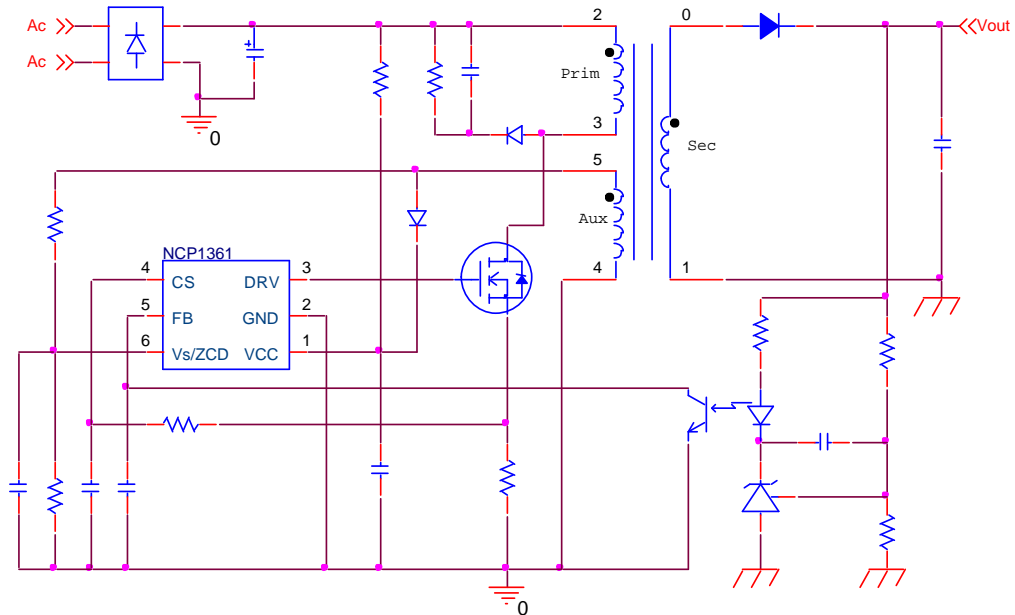


Figure 3. NCP1361 Typical Application Circuit

# NCP1361, NCP1366

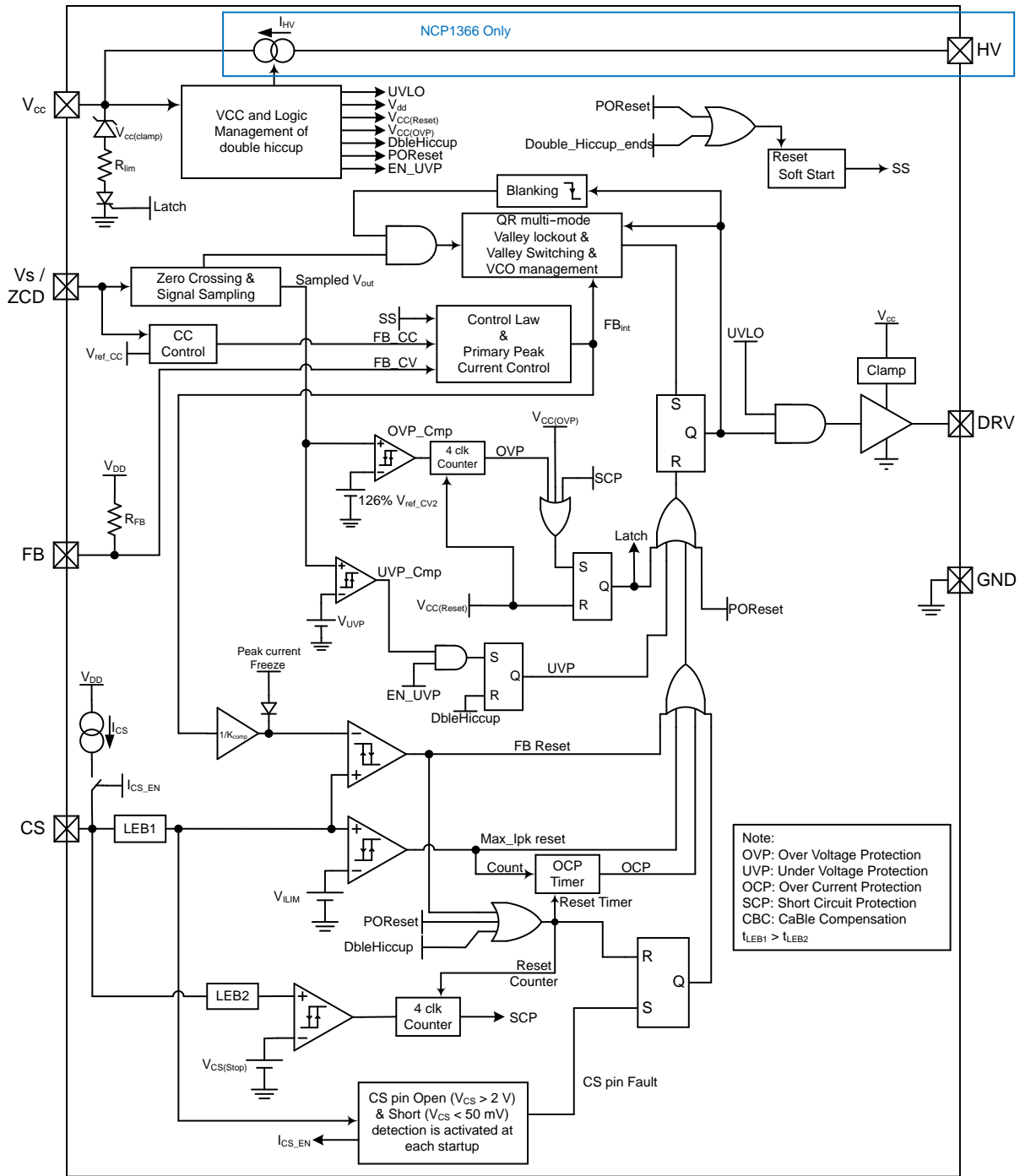


Figure 4. Functional Block Diagram: A Version

# NCP1361, NCP1366

## PIN FUNCTION DESCRIPTION

| Pin out<br>NCP1366 | Pin out<br>NCP1361 | Name      | Function   |
|--------------------|--------------------|-----------|--|
| 1                  | 6                  | $V_s/ZCD$ | Connected to the auxiliary winding; this pin senses the voltage output for the primary regulation and detects the core reset event for the Quasi-Resonant mode of operation. |
| 2                  | 5                  | FB        | This pin connects to an optocoupler collector and adjusts the peak current setpoint.   |
| 3                  | 4                  | CS        | This pin monitors the primary peak current.  |
| 4                  | 3                  | DRV       | Controller switch driver.  |
| 5                  | 2                  | GND       | Ground reference.  |
| 6                  | 1                  | $V_{CC}$  | This pin is connected to an external auxiliary voltage and supplies the controller.  |
| 7                  | -                  | NC        | Not Connected for creepage distance between high and low Voltage pins  |
| 8                  | -                  | HV        | Connected the high-voltage rail, this pin injects a constant current into the $V_{CC}$ capacitor for starting-up the power supply.   |

## MAXIMUM RATINGS

| Symbol                           | Rating  | Value                                  | Unit           |
|----------------------------------|---|--|----------------|
| $V_{CC(MAX)}$                    | Maximum Power Supply voltage, $V_{CC}$ pin, continuous voltage  | -0.3 to 28                             | V              |
| $\Delta V_{CC}/\Delta t$         | Maximum slew rate on $V_{CC}$ pin during startup phase  | +0.4                                   | V/ $\mu$ s     |
| $V_{DRV(MAX)}$<br>$I_{DRV(MAX)}$ | Maximum driver pin voltage, DRV pin, continuous voltage<br>Maximum current for DRV pin  | -0.3, $V_{DRV}$ (Note 1)<br>-300, +500 | V<br>mA        |
| $V_{MAX}$<br>$I_{MAX}$           | Maximum voltage on low power pins (except pins DRV and $V_{CC}$ )<br>Current range for low power pins (except pins DRV and $V_{CC}$ ) | -0.3, 5.5<br>-2, +5                    | V<br>mA        |
| $V_{HV}$                         | High Voltage pin voltage  | -0.3 to 560                            | V              |
| $R_{\theta J-A}$                 | Thermal Resistance Junction-to-Air  | 200                                    | $^{\circ}$ C/W |
| $T_{J(MAX)}$                     | Maximum Junction Temperature  | 150                                    | $^{\circ}$ C   |
|                                  | Operating Temperature Range   | -40 to +125                            | $^{\circ}$ C   |
|                                  | Storage Temperature Range   | -60 to +150                            | $^{\circ}$ C   |
|                                  | Human Body Model ESD Capability per JEDEC JESD22-A114F  | 2                                      | kV             |
|                                  | Machine Model ESD Capability (All pins except DRV) per JEDEC JESD22-A115C   | 200                                    | V              |
|                                  | Charged-Device Model ESD Capability per JEDEC JESD22-C101E  | 500                                    | V              |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- $V_{DRV}$  is the DRV clamp voltage  $V_{DRV(high)}$  when  $V_{CC}$  is higher than  $V_{DRV(high)}$ .  $V_{DRV}$  is  $V_{CC}$  otherwise
- This device contains latch-up protection and exceeds 100 mA per JEDEC Standard JESD78.

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| Characteristics | Conditions | Symbol | Min | Typ | Max | Unit |
|-----------------|------------|--------|-----|-----|-----|------|
|-----------------|------------|--------|-----|-----|-----|------|

## HIGH VOLTAGE STARTUP SECTION (NCP1366 only)

|   |   |               |    |     |     |               |
|---|---|---------------|----|-----|-----|---------------|
| Startup current sourced by $V_{CC}$ pin | $V_{HV} = 100\text{ V}$   | $I_{HV}$      | 70 | 100 | 150 | $\mu\text{A}$ |
| Leakage current at HV                   | $V_{HV} = 400\text{ V}$ , all options except NCP1366AABAY and NCP1366BABAY<br>All other options | $I_{HV\_LKG}$ | -  | 0.1 | 1.0 | $\mu\text{A}$ |
| Minimum Start-up HV voltage             | $I_{HV} = 95\%$ of $I_{HV}@V_{HV} = 100\text{ V}$ ,<br>$V_{CC} = V_{CC(on)} - 0.2\text{ V}$     | $V_{HV(min)}$ | -  | 22  | 25  | V             |

## SUPPLY SECTION AND $V_{CC}$ MANAGEMENT

|   |   |                 |     |     |      |                  |
|---|---|-----------------|-----|-----|------|------------------|
| $V_{CC}$ level at which driving pulses are authorized   | $V_{CC}$ increasing   | $V_{CC(on)}$    | 16  | 18  | 20   | V                |
| $V_{CC}$ level at which driving pulses are stopped  | $V_{CC}$ decreasing   | $V_{CC(off)}$   | 6.0 | 6.5 | 7.0  | V                |
| Internal Latch / Logic Reset Level<br>$V_{CC}$ clamp level  |   | $V_{CC(reset)}$ | -   | 5.6 | -    | V                |
| $V_{CC}$ clamp level (A & C version)  | Activated after Latch protection @ $I_{CC} = 100\ \mu\text{A}$  | $V_{CC(Clamp)}$ | -   | 4.2 | -    | V                |
| Minimal current into $V_{CC}$ pin that keeps the controller Latched (NCP1366, A & C fault mode version) |   | $I_{CC(Clamp)}$ | -   | -   | 20   | $\mu\text{A}$    |
| Minimal current into $V_{CC}$ pin that keeps the controller Latched (NCP1361, A & C fault mode version) |   | $I_{CC(Clamp)}$ | -   | -   | 6    | $\mu\text{A}$    |
| Current-limit resistor in series with the latch SCR   |   | $R_{lim}$       | -   | 7   | -    | $\text{k}\Omega$ |
| Over Voltage Protection   | Over Voltage threshold  | $V_{CC(OVP)}$   | 24  | 26  | 28   | V                |
| Start-up supply current, controller disabled or latched (Only valid with NCP1361)                       | $V_{CC} < V_{CC(on)}$ & $V_{CC}$ increasing from 0 V  | $I_{CC1}$       | -   | 2.5 | 5.0  | $\mu\text{A}$    |
| Internal IC consumption, steady state   | $F_{sw} = 65\text{ kHz}$ , $C_{DRV} = 1\text{ nF}$  | $I_{CC2}$       | -   | 1.7 | 2.5  | mA               |
| Internal IC consumption, frequency foldback mode  | VCO mode, $F_{sw} = 1\text{ kHz}$ , $C_{DRV} = 1\text{ nF}$   | $I_{CC3}$       | -   | 0.8 | 1.2  | mA               |
| Internal IC consumption when STBY mode is activated   | VCO mode, $F_{sw} = f_{VCO(min)}$ ,<br>$V_{Comp} = \text{GND}$ , $C_{DRV} = 1\text{ nF}$<br>$f_{VCO(min)} = 200\text{ Hz}$<br>$f_{VCO(min)} = 600\text{ Hz}$<br>$f_{VCO(min)} = 1.2\text{ kHz}$ | $I_{CC4}$       | -   | 470 | 520  | $\mu\text{A}$    |
|   |   |                 | -   | 500 | TBD* |                  |
|   |   |                 | -   | 530 | TBD* |                  |

## CURRENT COMPARATOR

|   |  |            |      |      |      |    |
|---|--|------------|------|------|------|----|
| Current Sense Voltage Threshold               | $V_{Comp} = V_{Comp(max)}$ , $V_{CS}$ increasing   | $V_{LIM}$  | 0.76 | 0.80 | 0.84 | V  |
| Cycle by Cycle Leading Edge Blanking Duration | options NCP1366AABAY,<br>NCP1366BABAY, NCP1361AABAY,<br>NCP1361BABAY and NCP1361EABAY<br>All other options | $t_{LEB1}$ | 250  | 300  | 360  | ns |
|   |  |            | 240  | 300  | 360  |    |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. The timer can be reset if there are 4 DRV cycles without overload or short circuit conditions

4. Guaranteed by Design.

\* Characterization upon request

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| Characteristics   | Conditions   | Symbol         | Min  | Typ               | Max  | Unit |
|---|--|----------------|------|-------------------|------|------|
| <b>CURRENT COMPARATOR</b>   |  |                |      |                   |      |      |
| Cycle by Cycle Current Sense Propagation Delay                            | $V_{CS} > (V_{ILIM} + 100\text{ mV})$ to DRV turn-off  | $t_{ILIM}$     | -    | 50                | 100  | ns   |
| Timer Delay Before Latching in Overload Condition                         | When CS pin $\geq \times V_{ILIM}$<br>(Note 3)   | $T_{OCP}$      | 50   | 70                | 90   | ms   |
| Threshold for Immediate Fault Protection Activation                       |  | $V_{CS(stop)}$ | 1.08 | 1.2               | 1.32 | V    |
| Leading Edge Blanking Duration for $V_{CS(stop)}$                         |  | $t_{LEB2}$     | -    | 120               | -    | ns   |
| Maximum peak current level at which VCO takes over or frozen peak current | $V_{Comp} < 1.9\text{ V}$ , $V_{CS}$ increasing<br>option X (~15% $V_{ILIM}$ )<br>option Y (~20% $V_{ILIM}$ )<br>option Z (~25% $V_{ILIM}$ ) | $V_{CS(VCO)}$  | -    | 120<br>160<br>200 | -    | mV   |

## REGULATION BLOCK

|  |  |                 |                   |                                       |                   |                   |
|--|--|-----------------|-------------------|---------------------------------------|-------------------|-------------------|
| Internal Voltage reference for Constant Current regulation | $T_J = 25^\circ\text{C}$<br>$-40^\circ\text{C} < T_J < 125^\circ\text{C}$  | $V_{ref\_CC}$   | 0.98<br>0.97      | 1.00<br>1.00                          | 1.02<br>1.03      | V                 |
| Pullup Resistor  |  | $R_{FB}$        | -                 | 20                                    | -                 | k $\Omega$        |
| Valley Thresholds  |  |                 |                   |                                       |                   | V                 |
| Transition from 1 <sup>st</sup> to 2 <sup>nd</sup> valley  | $V_{Comp}$ decreasing  | $V_{H2D}$       | -                 | 2.50                                  | -                 |                   |
| Transition from 2 <sup>nd</sup> to 3 <sup>rd</sup> valley  | $V_{Comp}$ decreasing  | $V_{H3D}$       | -                 | 2.30                                  | -                 |                   |
| Transition from 3 <sup>rd</sup> to 4 <sup>th</sup> valley  | $V_{Comp}$ decreasing  | $V_{H4D}$       | -                 | 2.10                                  | -                 |                   |
| Transition from 4 <sup>th</sup> valley to VCO              | $V_{Comp}$ decreasing  | $V_{HVCO D}$    | -                 | 1.90                                  | -                 |                   |
| Transition from VCO to 4 <sup>th</sup> valley              | $V_{Comp}$ increasing  | $V_{HVCO I}$    | -                 | 2.50                                  | -                 |                   |
| Transition from 4 <sup>th</sup> to 3 <sup>rd</sup> valley  | $V_{Comp}$ increasing  | $V_{H4I}$       | -                 | 2.70                                  | -                 |                   |
| Transition from 3 <sup>rd</sup> to 2 <sup>nd</sup> valley  | $V_{Comp}$ increasing  | $V_{H3I}$       | -                 | 2.90                                  | -                 |                   |
| Transition from 2 <sup>nd</sup> to 1 <sup>st</sup> valley  | $V_{Comp}$ increasing  | $V_{H2I}$       | -                 | 3.10                                  | -                 |                   |
| Minimal difference between any two valleys                 | $V_{Comp}$ increasing or $V_{Comp}$ decreasing   | $\Delta V_H$    | 176               | -                                     | -                 | mV                |
| Internal Dead Time generation for VCO mode                 | Entering in VCO when $V_{Comp}$ is decreasing and crosses $V_{HVCO D}$   | $T_{DT(start)}$ | -                 | 2                                     | -                 | $\mu\text{s}$     |
| Internal Dead Time generation for VCO mode                 | Leaving VCO mode when $V_{Comp}$ is increasing and crosses $V_{HVCO I}$  | $T_{DT(ends)}$  | -                 | 1                                     | -                 | $\mu\text{s}$     |
| Internal Dead Time generation for VCO mode                 | When in VCO mode<br>$V_{Comp} = 1.8\text{ V}$<br>$V_{Comp} = 1.3\text{ V}$<br>$V_{Comp} = 0.8\text{ V}$<br>$V_{Comp} < 0.4\text{ V}$ - 200 Hz option (Note 4)<br>$V_{Comp} < 0.4\text{ V}$ - 600 Hz option (Note 4)<br>$V_{Comp} < 0.4\text{ V}$ - 1.2 kHz option (Note 4) | $T_{DT}$        | -                 | 6<br>25<br>220<br>5000<br>1667<br>833 | -                 | $\mu\text{s}$     |
| Minimum Operating Frequency in VCO Mode                    | $V_{Comp} = \text{GND}$  | $f_{VCO(MIN)}$  | 150<br>450<br>0.9 | 200<br>600<br>1.2                     | 250<br>750<br>1.5 | Hz<br>Hz<br>kHz   |
| Maximum Operating Frequency                                |  | $f_{MAX}$       | -                 | No Clamp<br>80<br>110                 | -                 | N/A<br>kHz<br>kHz |

## DEMAGNETIZATION INPUT - ZERO VOLTAGE DETECTION CIRCUIT and VOLTAGE SENSE

|                             |                      |                |    |    |    |    |
|-----------------------------|----------------------|----------------|----|----|----|----|
| $V_{ZCD}$ threshold voltage | $V_{ZCD}$ decreasing | $V_{ZCD(TH)}$  | 25 | 45 | 65 | mV |
| $V_{ZCD}$ Hysteresis        | $V_{ZCD}$ increasing | $V_{ZCD(HYS)}$ | 15 | 30 | 45 | mV |

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| Characteristics | Conditions | Symbol | Min | Typ | Max | Unit |
|-----------------|------------|--------|-----|-----|-----|------|
|-----------------|------------|--------|-----|-----|-----|------|

## DEMAGNETIZATION INPUT - ZERO VOLTAGE DETECTION CIRCUIT and VOLTAGE SENSE

|   |   |                          |           |           |           |               |
|---|---|--------------------------|-----------|-----------|-----------|---------------|
| Threshold voltage for output short circuit or aux. winding short circuit detection        | After $t_{BLANK\_ZCD}$ if $V_{ZCD} < V_{ZCD(short)}$<br>→ Latched | $V_{ZCD(short)}$         | 30        | 50        | 70        | mV            |
| Propagation Delay from valley detection to DRV high                                       | $V_{ZCD}$ decreasing from 4 V to 0 V                              | $t_{DEM}$                | -         | -         | 170       | ns            |
| Delay after on-time that the $V_g/ZCD$ is still pulled to ground                          | (Note 4)  | $t_{short\_ZCD}$         | -         | 0.7       | -         | $\mu\text{s}$ |
| Blanking delay after on-time ( $V_g/ZCD$ pin is disconnected from the internal circuitry) |   | $t_{blank\_ZCD}$         | 1.2       | 1.5       | 1.8       | $\mu\text{s}$ |
| Timeout after last demagnetization transition   | Timeout while in Soft-start<br>Timeout after soft-start complete  | $t_{outSS}$<br>$t_{out}$ | 36<br>4.5 | 44<br>5.5 | 52<br>6.5 | $\mu\text{s}$ |
| Input leakage current   | $V_{CC} > V_{CC(on)}$ $V_{ZCD} = 4\text{ V}$ , DRV is low         | $I_{ZCD}$                | -         | -         | 0.1       | $\mu\text{A}$ |

## DRIVE OUTPUT - GATE DRIVE

|  |  |                        |        |         |        |          |
|--|--|------------------------|--------|---------|--------|----------|
| Drive resistance<br>DRV Sink<br>DRV Source |  | $R_{SNK}$<br>$R_{SRC}$ | -<br>- | 7<br>12 | -<br>- | $\Omega$ |
| Rise time                                  | $C_{DRV} = 1\text{ nF}$ , from 10% to 90%  | $t_r$                  | -      | 45      | 80     | ns       |
| Fall time                                  | $C_{DRV} = 1\text{ nF}$ , from 90% to 10%  | $t_f$                  | -      | 30      | 60     | ns       |
| DRV Low voltage                            | $V_{CC} = V_{CC(off)} + 0.2\text{ V}$ ,<br>$C_{DRV} = 220\text{ pF}$ , $R_{DRV} = 33\text{ k}\Omega$ | $V_{DRV(low)}$         | 6.0    | -       | -      | V        |
| DRV High voltage                           | $V_{CC} = V_{CC(OVP)} - 0.2\text{ V}$ , $C_{DRV} = 220\text{ pF}$ ,<br>$R_{DRV} = 33\text{ k}\Omega$ | $V_{DRV(high)}$        | -      | -       | 13.0   | V        |

## SOFT START

|                                    |   |          |   |   |   |    |
|------------------------------------|---|----------|---|---|---|----|
| Internal Fixed Soft Start Duration | Current Sense peak current rising from 0.2 V to 0.8 V | $t_{SS}$ | 3 | 4 | 5 | ms |
|------------------------------------|---|----------|---|---|---|----|

## FAULT PROTECTION

|  |  |                    |      |      |      |                  |
|--|--|--------------------|------|------|------|------------------|
| Thermal Shutdown   | Device switching ( $F_{sw} \sim 65\text{ kHz}$ ) (Note 4)  | $T_{SHTDN}$        | -    | 150  | -    | $^\circ\text{C}$ |
| Thermal Shutdown Hysteresis  | Device switching ( $F_{sw} \sim 65\text{ kHz}$ ) (Note 4)  | $T_{SHTDN(HYS)}$   | -    | 40   | -    | $^\circ\text{C}$ |
| Number of Drive cycle before latch confirmation  | $V_{Comp} = V_{Comp(max)}$ ,<br>$V_{CS} > V_{CS(stop)}$<br>Or Internal sampled $V_{out} > V_{OVP}$ | $T_{latch\_count}$ | -    | 4    | -    | -                |
| Fault level detection for OVP → Latched or Double Hiccup autorecovery (depends on fault version)   | Internal sampled $V_{out}$ increasing<br>$V_{OVP} = V_{ref\_CV2} + 26\%$<br>Version E              | $V_{OVP}$          | 2.95 | 3.15 | 3.35 | V                |
|  |  |                    | 3.4  | 3.6  | 3.8  |                  |
| Fault level detection for UVP → Latched or Double Hiccup autorecovery (depends on fault version) (UVP detection is disabled during $T_{EN\_UVP}$ ) | Internal sampled $V_{out}$ decreasing<br>Fault Mode Option A, B & C<br>Fault Mode Option Version E | $V_{UVP}$          | 1.4  | 1.5  | 1.6  | V                |
|  |  |                    | 0.70 | 0.75 | 0.80 |                  |
| Blanking time for UVP detection  | Starting at the beginning of the Soft start  | $T_{EN\_UVP}$      | -    | 37   | -    | ms               |
| Pull-up Current Source on CS pin for Open or Short circuit detection   | When $V_{CS} > V_{CS\_min}$  | $I_{CS}$           | -    | 55   | -    | $\mu\text{A}$    |

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| Characteristics              | Conditions  | Symbol          | Min | Typ | Max | Unit          |
|------------------------------|-------------|-----------------|-----|-----|-----|---------------|
| <b>FAULT PROTECTION</b>      |             |                 |     |     |     |               |
| CS pin Open detection        | CS pin open | $V_{CS(open)}$  | 0.8 | -   | -   | V             |
| CS pin Short detection       |             | $V_{CS\_min}$   | -   | 50  | 70  | mV            |
| CS pin Short detection timer | (Note 4)    | $T_{CS\_short}$ | -   | 3   | -   | $\mu\text{s}$ |

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## FAULT MODE STATES TABLE (WHATEVER THE VERSION)

| Event   | Timer Protection | Next Device Status  | Release to Normal Operation Mode   |
|---|------------------|---|--|
| Overcurrent<br>$V_{CS} > V_{ILIM}$                                  | OCP timer        | Double Hiccup   | <ul style="list-style-type: none"> <li>Resume to normal operation: if 4 pulses from FB Reset &amp; then Reset timer</li> <li>Resume operation after Double Hiccup</li> </ul> |
| Winding short<br>$V_{CS} > V_{CS(stop)}$                            | Immediate        | 4 consecutive pulses with $V_{CS} > V_{CS(stop)}$ before Latching | $V_{CC}$ is decreasing to $V_{CC(clamp)}$ and waiting for unplug from line $V_{CC} < V_{CC(reset)}$  |
| CS pin Fault:<br>Short & Open                                       | Immediate        | Double Hiccup   | Resume operation after Double Hiccup   |
| Low supply<br>$V_{CC} < V_{CC(off)}$                                | 10 $\mu$ s timer | Double Hiccup   | Resume operation after Double Hiccup   |
| Internal TSD  | 10 $\mu$ s timer | Double Hiccup   | Resume operation after Double Hiccup & $T < (T_{SHTDN} - T_{SHTDN(Hyst)})$   |
| ZCD short<br>$V_{ZCD} < V_{ZCD(short)}$ after $t_{BLANK\_ZCD}$ time | Immediate        | Double Hiccup   | Resume operation after Double Hiccup ( $V_{CC(on)} < V_{CC} < V_{CC(reset)}$ )   |

## FAULT MODE STATES TABLE (ACCORDING TO THE CONTROLLER VERSIONS)

| Event  | A Version     | B Version     | C Version     | E Version     |
|--|---------------|---------------|---------------|---------------|
| $V_{CC\_OVP}$<br>$V_{CC} > V_{CC(OVP)} = 26\text{ V}$  | Latched_Timer | Auto Recovery | Latched_Timer | Auto Recovery |
| $V_{OVP}$<br>$V_{OUT} > 126\% \cdot V_{REF\_CV2} = 3.15\text{ V}/3.6\text{ V [E]}$                           | Latched_4clk  | Auto Recovery | Latched_4clk  | Auto Recovery |
| $V_{UVP}$<br>$V_{OUT} < 60\% V_{REF\_CV2}, = 1.5\text{ V}/0.75\text{ V [E]}$<br>when VOUT is decreasing only | Auto Recovery | Auto Recovery | Latched_Timer | Auto Recovery |

## FAULT TYPE MODE DEFINITION

| Fault Mode    | Timer Protection | Next Device Status  | Release to Normal Operation Mode  |
|---------------|------------------|---|---|
| Latched_Timer | 10 $\mu$ s timer | Latched   | $V_{CC}$ is decreasing to $V_{CC(clamp)}$ and waiting for unplug from line $V_{CC} < V_{CC(reset)}$ |
| Latched_4clk  | Immediate        | 4 consecutive pulses with $V_{CS} > 126\% V_{ref\_CV2}$ before Latching | $V_{CC}$ is decreasing to $V_{CC(clamp)}$ and waiting for unplug from line $V_{CC} < V_{CC(reset)}$ |
| Autorecovery  | Immediate        | Resume operation after Double Hiccup                                    | Resume operation after Double Hiccup ( $V_{CC(on)} < V_{CC} < V_{CC(reset)}$ )                      |

# NCP1361, NCP1366

## CHARACTERIZATION CURVES

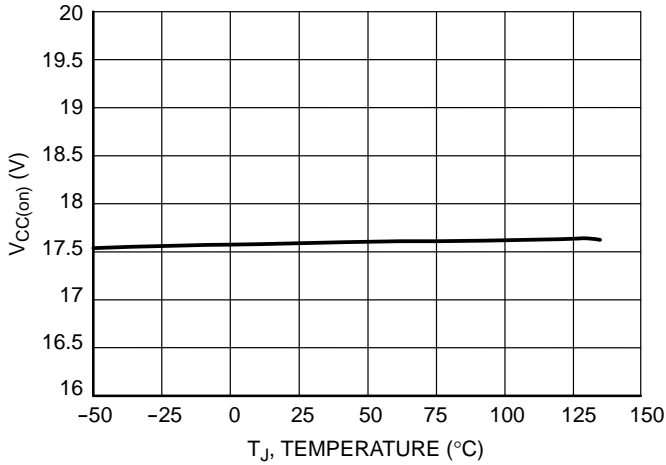


Figure 5. V<sub>CC</sub> Startup Threshold versus Temperature

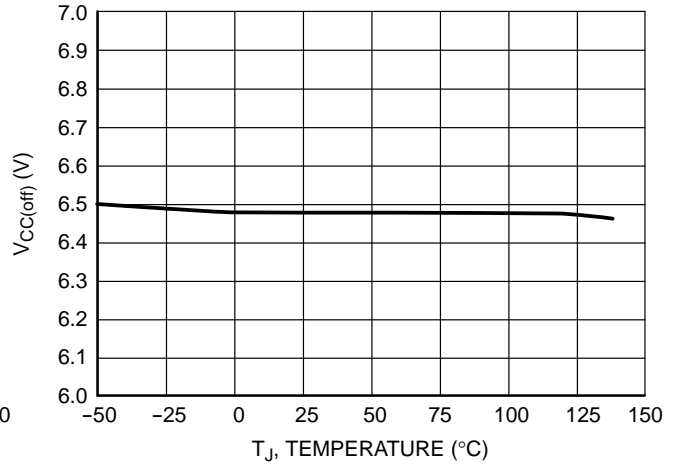


Figure 6. V<sub>CC</sub> Minimum Operating versus Temperature

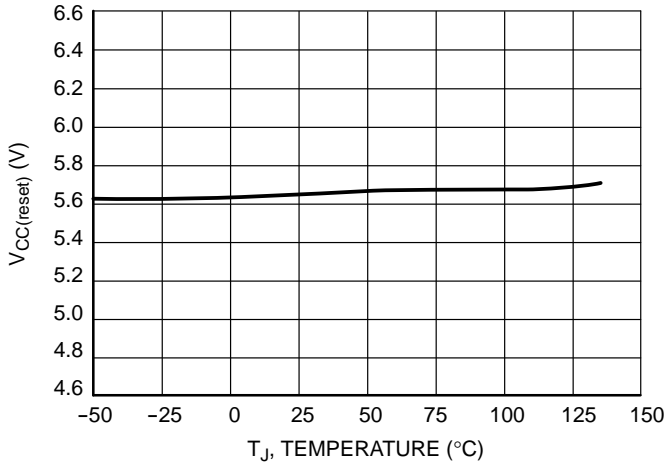


Figure 7. V<sub>CC(reset)</sub> versus Temperature

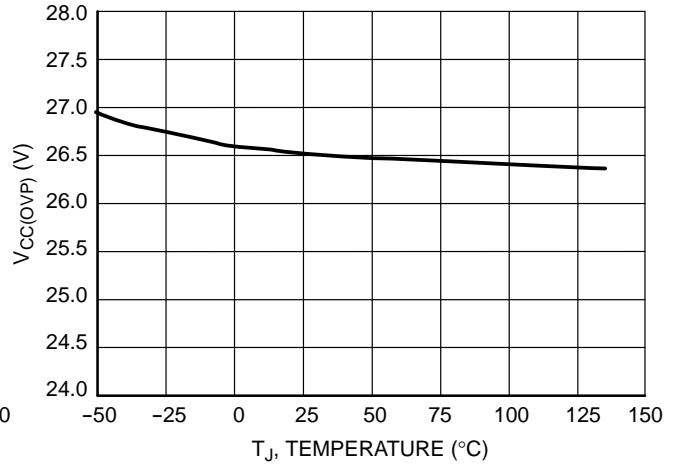


Figure 8. V<sub>CC(OVP)</sub> versus Temperature

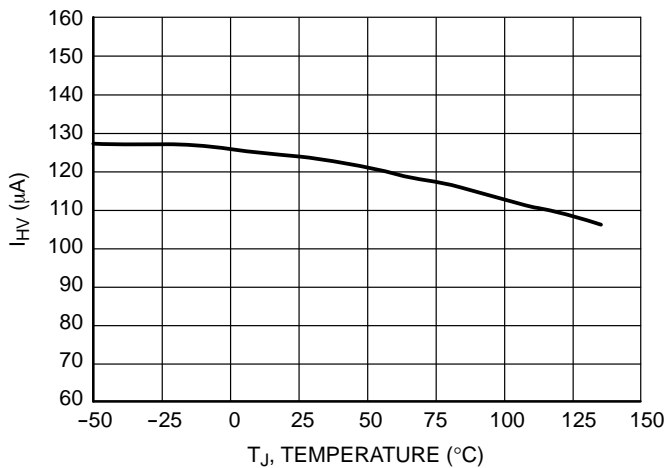


Figure 9. Startup Current Source versus Temperature

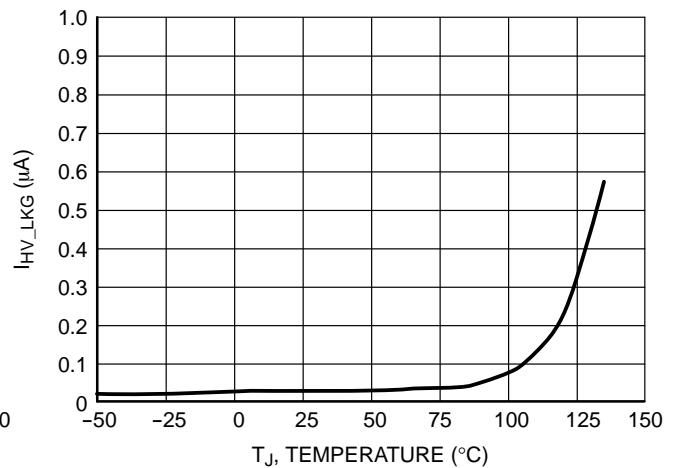
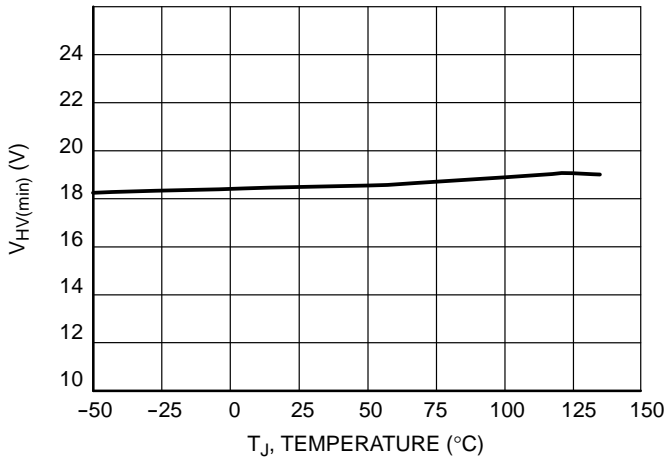


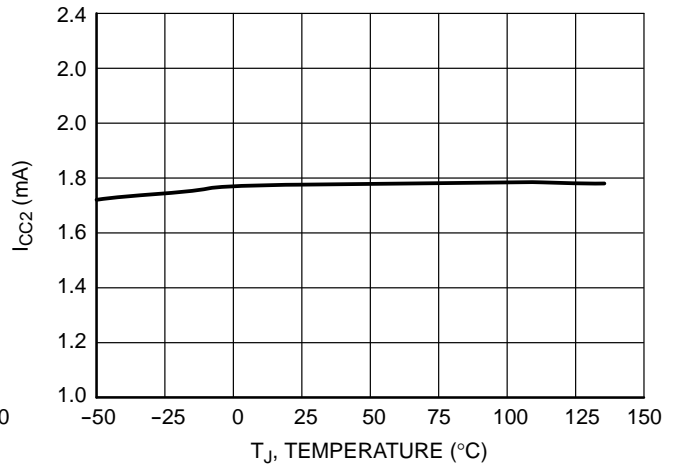
Figure 10. HV Pin Leakage versus Temperature

# NCP1361, NCP1366

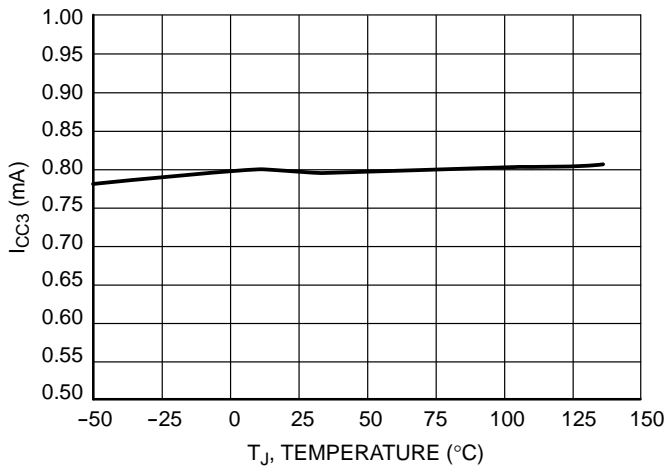
## CHARACTERIZATION CURVES



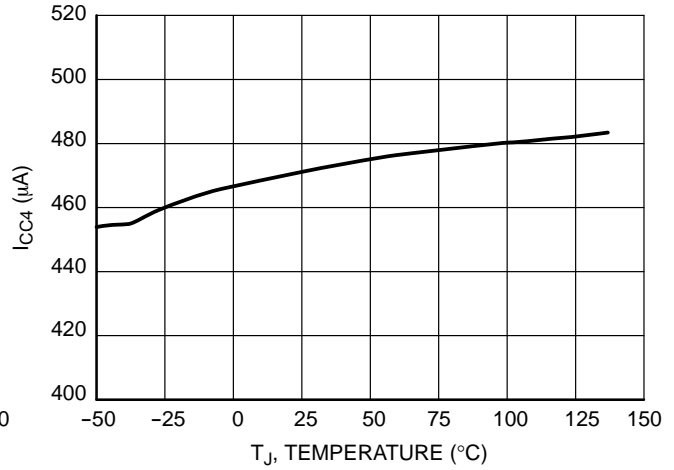
**Figure 11. Minimum Voltage for HV Startup Current Source versus Temperature**



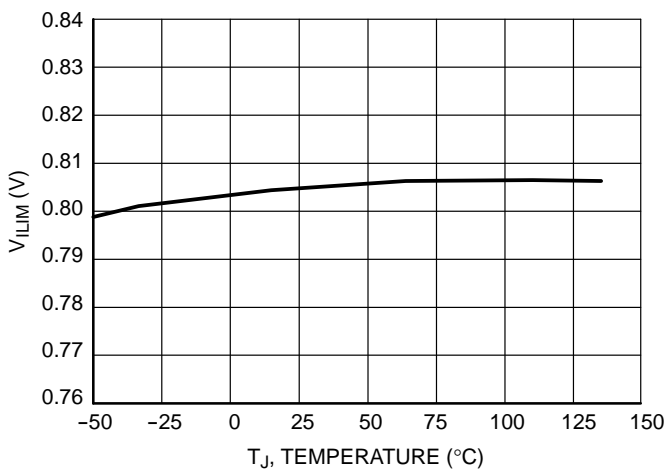
**Figure 12. I<sub>CC2</sub> versus Temperature**



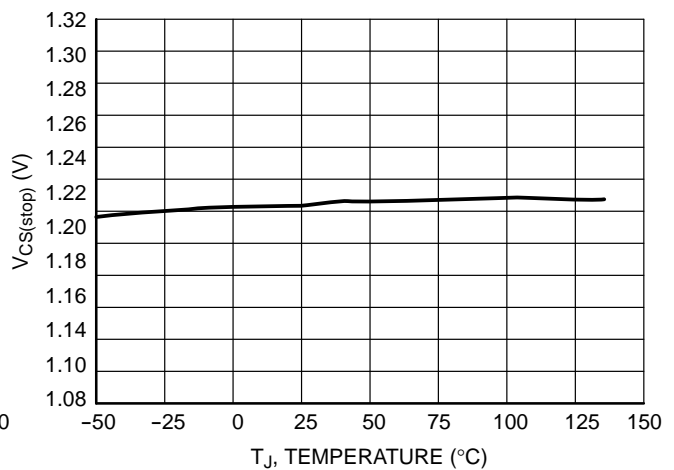
**Figure 13. I<sub>CC3</sub> versus Temperature**



**Figure 14. Standby Current Consumption (200 Hz option) versus Temperature**



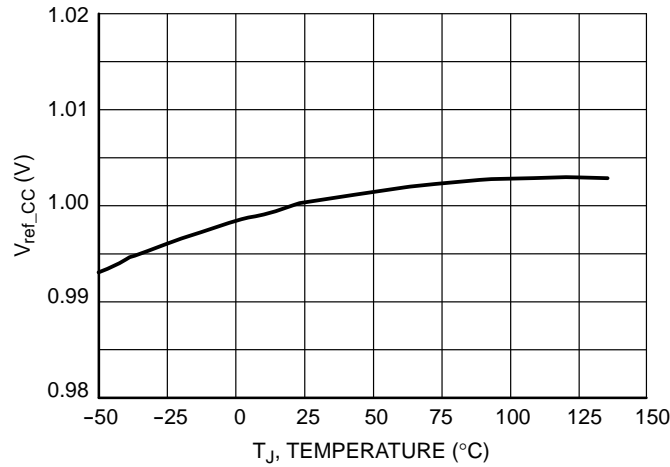
**Figure 15. Max Peak Current Limit versus Temperature**



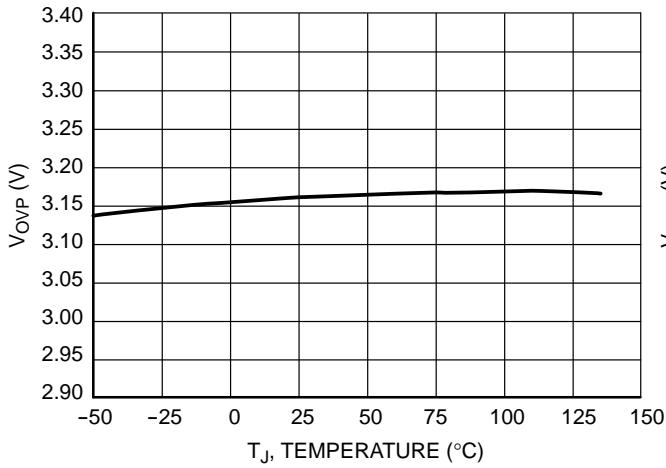
**Figure 16. Second Peak Current Limit for Fault Protection versus Temperature**

# NCP1361, NCP1366

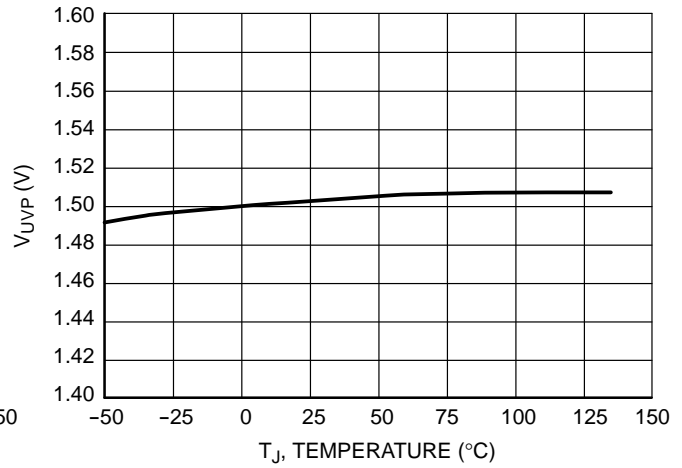
## CHARACTERIZATION CURVES



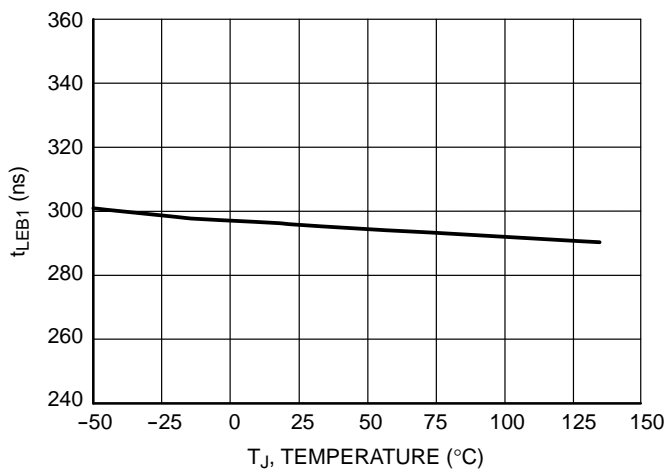
**Figure 17. Internal Voltage Reference for Constant Current Regulation versus Temperature**



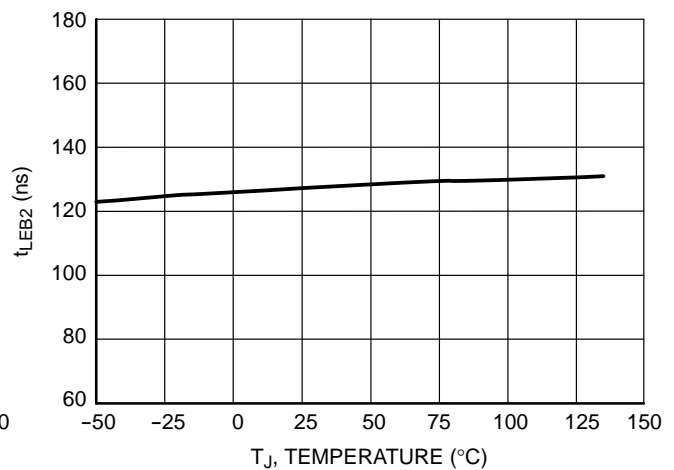
**Figure 18. Output Over Voltage Level versus Temperature (Fault Mode Options A, B & C)**



**Figure 19. Output Under Voltage Level versus Temperature (Fault Mode Options A & B)**



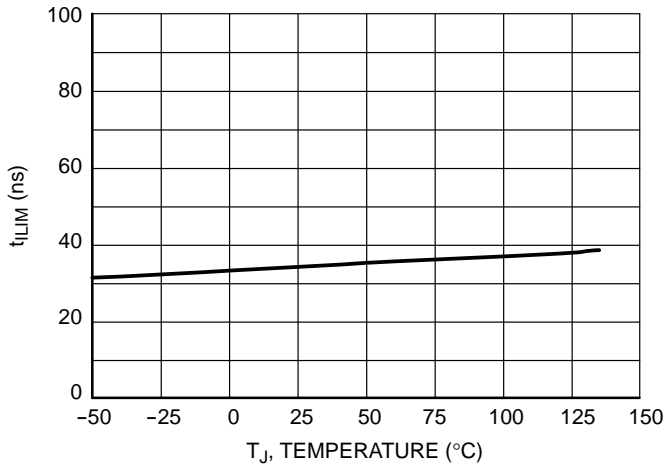
**Figure 20. Cycle-by-Cycle Leading Edge Blanking Duration versus Temperature**



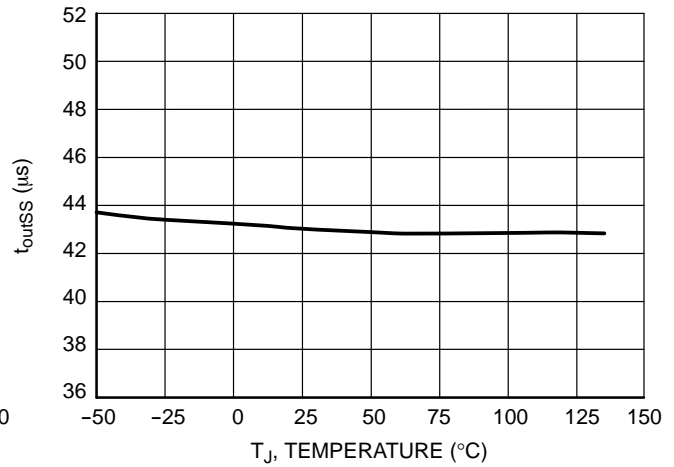
**Figure 21. Leading Edge Blanking Duration for V<sub>CS(stop)</sub> Level versus Temperature**

# NCP1361, NCP1366

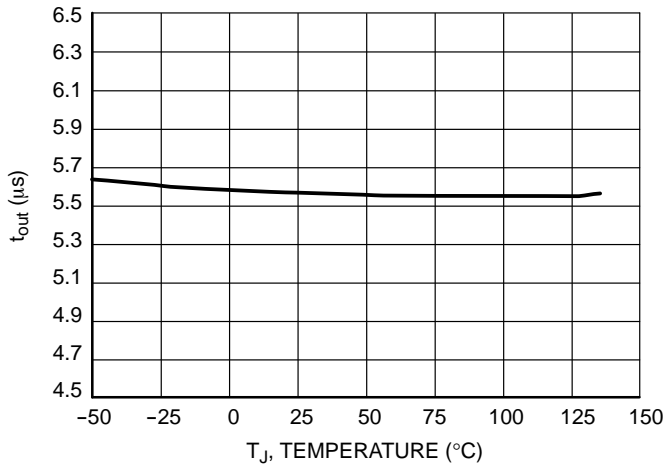
## CHARACTERIZATION CURVES



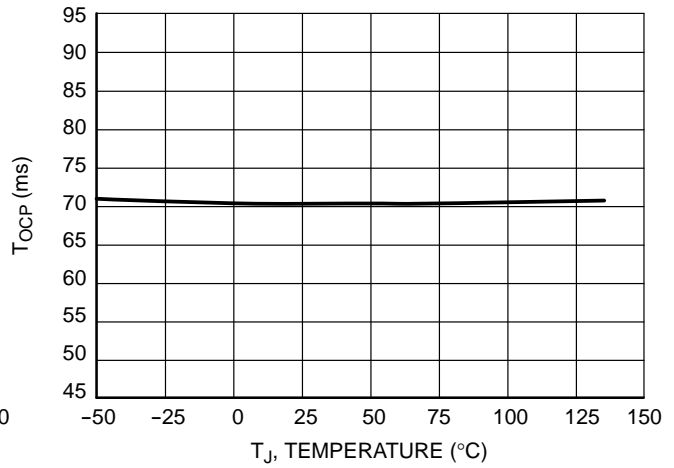
**Figure 22. Cycle-by-Cycle Current Sense Propagation Delay versus Temperature**



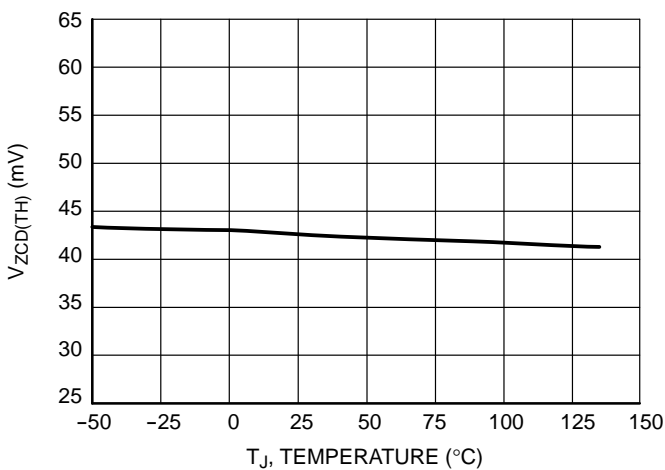
**Figure 23. Timeout After Last Demagnetization Transition in Soft-Start versus Temperature**



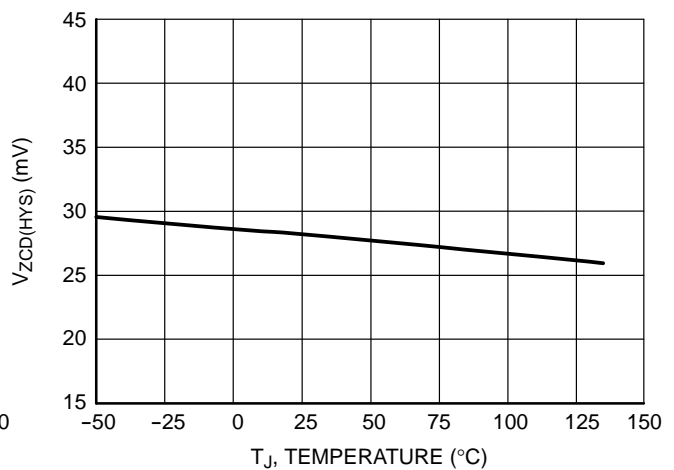
**Figure 24. Timeout After Last Demagnetization Transition versus Temperature**



**Figure 25. Timer Delay Before Latching in Overload Condition versus Temperature**



**Figure 26. Zero Voltage Detection Threshold Voltage versus Temperature**



**Figure 27. Zero Voltage Detection Hysteresis versus Temperature**

# NCP1361, NCP1366

## CHARACTERIZATION CURVES

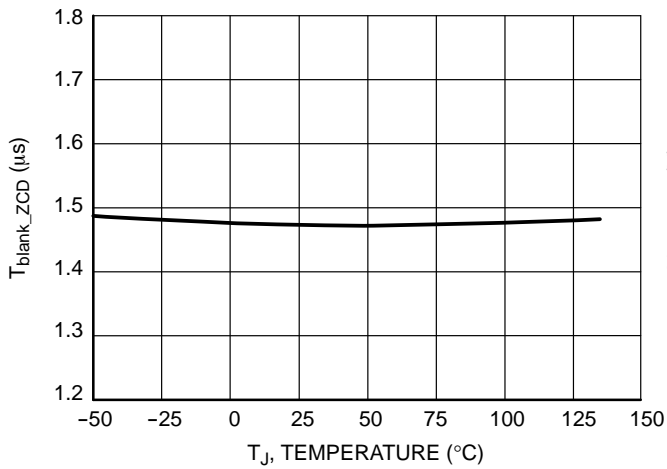


Figure 28. Blanking Delay for ZCD Detection versus Temperature

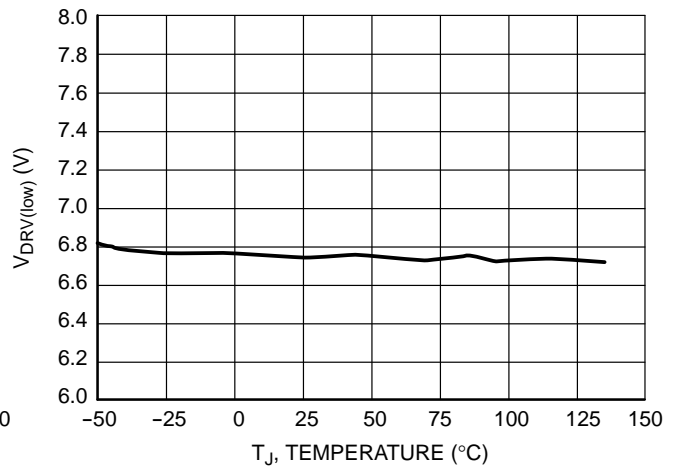


Figure 29. V<sub>DRV(low)</sub> versus Temperature

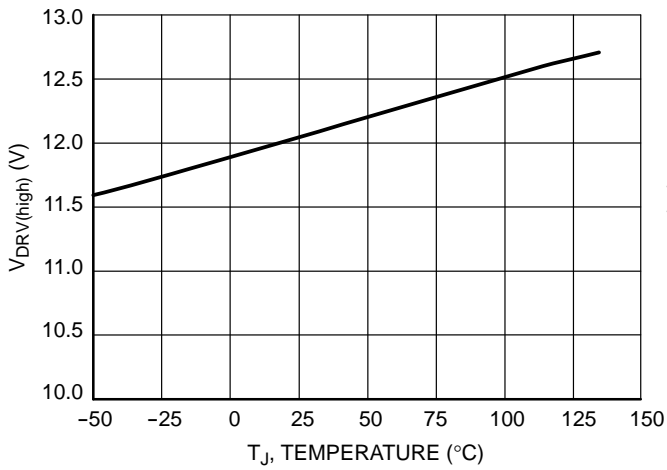


Figure 30. V<sub>DRV(high)</sub> versus Temperature

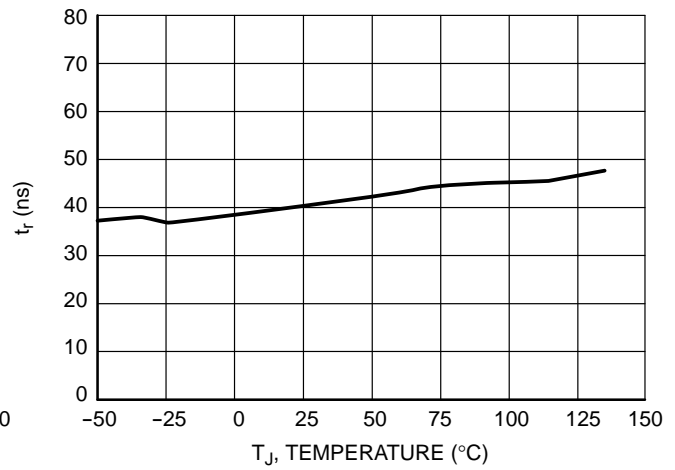


Figure 31. Gate Drive Rise Time versus Temperature

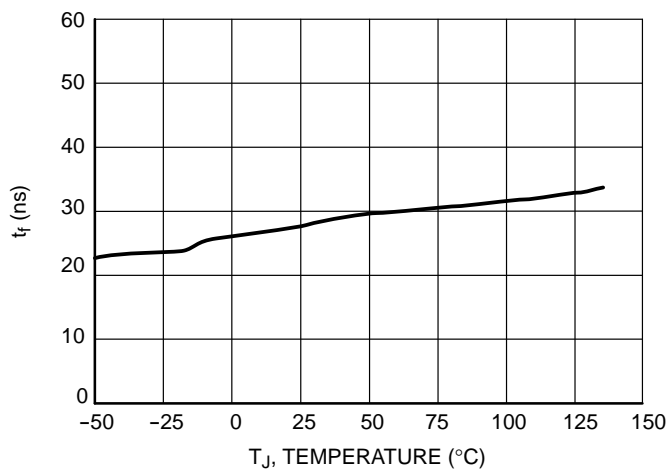
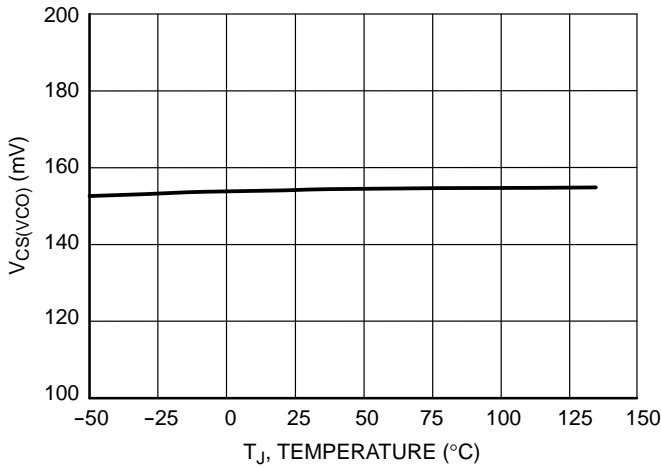


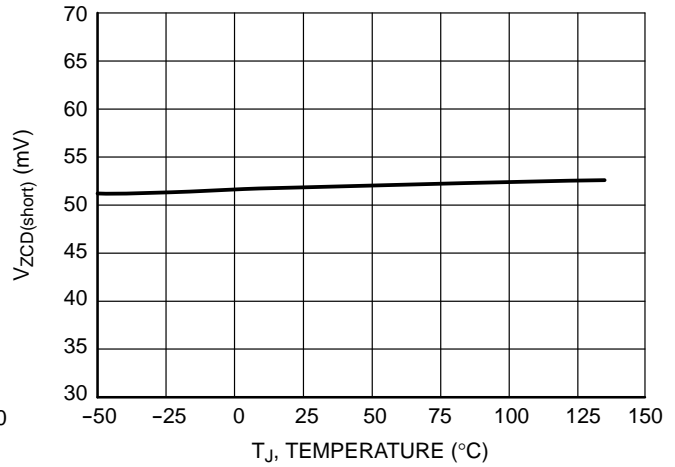
Figure 32. Gate Drive Fall Time versus Temperature

# NCP1361, NCP1366

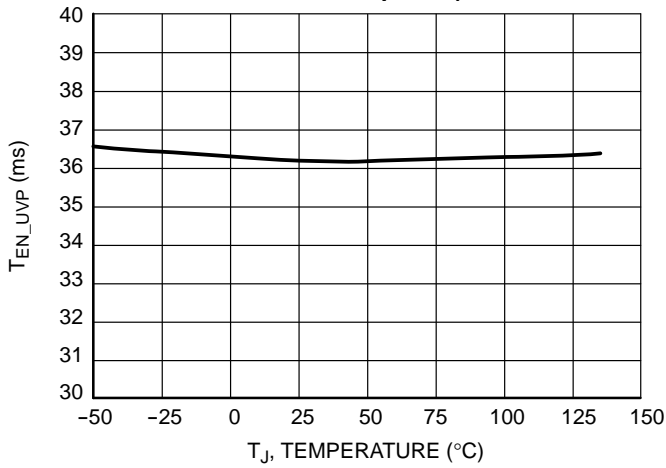
## CHARACTERIZATION CURVES



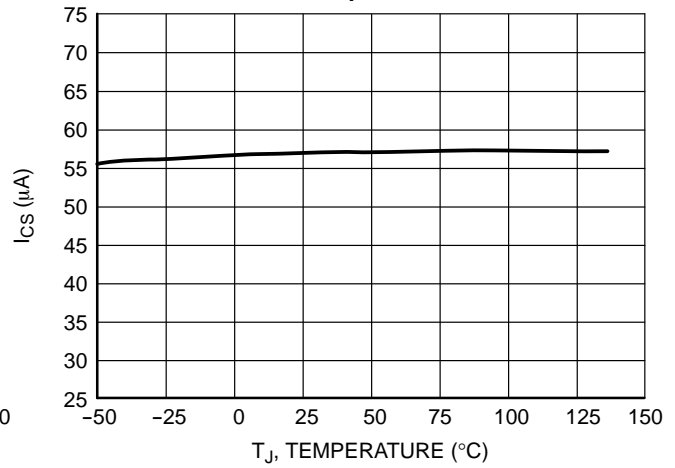
**Figure 33. Minimum or Frozen Peak Current on CS Pin versus Temperature (Frozen Peak Current optionY)**



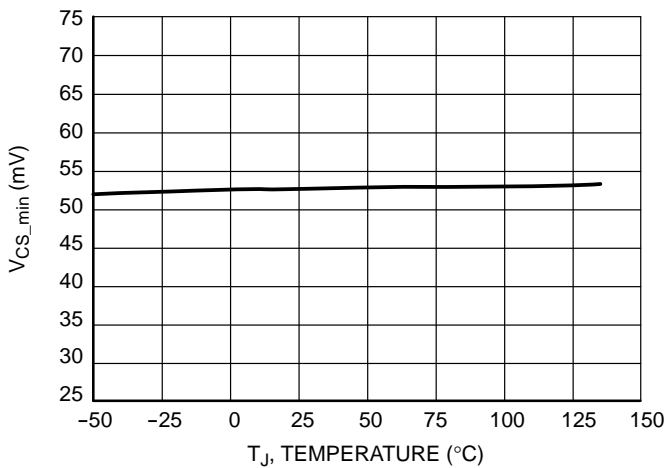
**Figure 34. Threshold Level for Detecting Output or Aux. Winding Short versus Temperature**



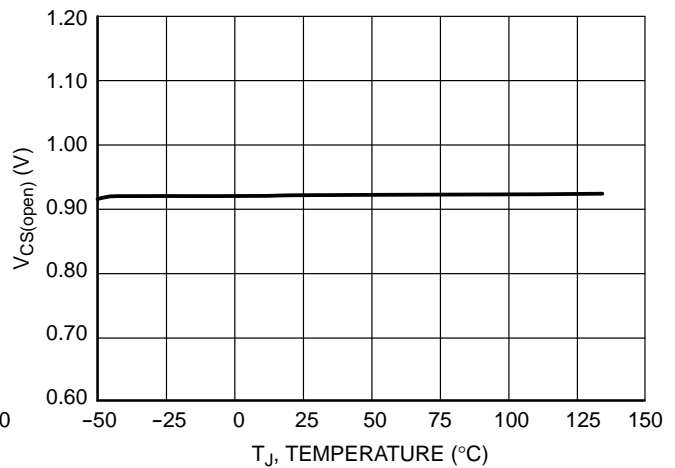
**Figure 35. Startup Blanking Time for UVP Detection versus Temperature**



**Figure 36. Pull-up Current Source for Detecting Open or Short on CS Pin versus Temperature**



**Figure 37. CS Pin Short Detection Threshold versus Temperature**



**Figure 38. CS Pin Open Detection Threshold versus Temperature**

APPLICATION INFORMATION

The NCP1366/61 is a flyback power supply controller providing a means to implement primary side constant-current regulation. This technique does not need a secondary side feedback circuitry, associated bias current and an opto-coupler. NCP1366/61 implements a current-mode architecture operating in quasi-resonant mode. The controller prevents valley-jumping instability and steadily locks out in a selected valley as the power demand goes down. As long as the controller is able to detect a valley, the new cycle or the following drive remains in a valley. Due to a dedicated valley detection circuitry operating at any line and load conditions, the power supply efficiency will always be optimized. In order to prevent any high switching frequency two frequency clamp options are available.

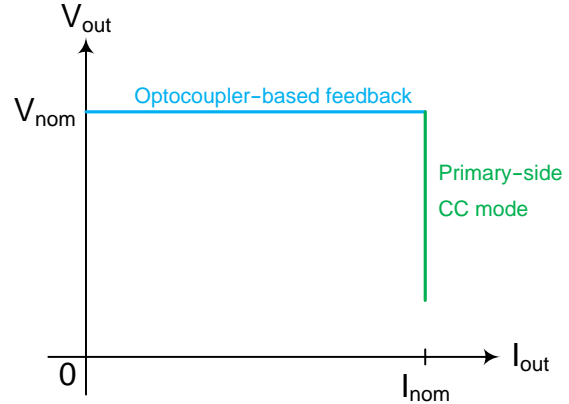


Figure 39. Constant-Voltage & Constant-Current Mode

• **Quasi-Resonance Current-mode operation:**

implementing quasi-resonance operation in peak current-mode control optimizes the efficiency by switching in the valley of the MOSFET drain-source voltage. Due to a proprietary circuitry, the controller locks-out in a selected valley and remains locked until the input voltage significantly changes. Only the four first valleys could be locked out. When the load current diminishes, valley switching mode of operation is kept but without valley lock-out. Valley-switching operation across the entire input/output conditions brings efficiency improvement and lets the designer build higher-density converters.

• **Frequency Clamp:** As the frequency is not fixed and dependent on the line, load and transformer specifications, it is important to prevent switching frequency runaway for applications requiring maximum switching frequencies up to 90 kHz or 130 kHz. Two frequency clamp options at 80 kHz or 110 kHz are available for this purpose. In case frequency clamp is not needed, a specific version of the 1361/66 exists in which the clamp is deactivated.

• **Primary Side Constant Current Regulation:** Battery charging applications request constant current regulation. NCP1361/66 controls and regulates the output current at a constant level regardless of the input and output voltage conditions. This function offers tight over power protection by estimating and limiting the maximum output current from the primary side, without any particular sensor.

• **Optocoupler-based feedback:** the voltage feedback loop is classically implemented with an optocoupler and a NCP431 voltage reference in the secondary side. By pulling the feedback pin low, the controller adjusts the peak current setpoint and regulates  $V_{out}$ .

- **Soft-Start:** 4 ms internal fixed soft start guarantees a peak current starting from zero to its nominal value with smooth transition in order to prevent any overstress on the power components at each startup.
- **Cycle-by-Cycle peak current limit:** If the max peak current reaches the  $V_{ILIM}$  level, the over current protection timer is enabled and starts counting. If the overload lasts  $T_{OCP}$  delay, then the fault is latched and the controller stops immediately driving the power MOSFET. The controller enters in a double hiccup mode before autorecovering with a new startup cycle.
- **$V_{CC}$  Over Voltage Protection:** If the  $V_{CC}$  voltage reaches the  $V_{CC(OVP)}$  threshold the controller enters in latch mode. Thus it stops driving pulse on  $DRV$  pin:
  - ♦ **A & C version - (Latched  $V_{CC(OVP)}$ ):**  $V_{CC}$  capacitor is internally discharged to the  $V_{CC(Clamp)}$  level with a very low power consumption: the controller is completely disabled. Resuming operation is possible by unplugging the line in order to releasing the internal  $V_{CC}$  thyristor with a  $V_{CC}$  current lower than the  $I_{CC(Clamp)}$ .
  - ♦ **B version - (Autorecovery):** it enters in double hiccup mode before resuming operation.
- **Winding Short-Circuit Protection:** An additional comparator senses the  $CS$  signal and stops the controller if  $V_{CS}$  reaches  $V_{ILIM}+50\%$  (after a reduced LEB:  $t_{LEB2}$ ). Short circuit protection is enabled only if 4 consecutive pulses reach  $SCP$  level. This small counter prevents any false triggering of short circuit protection during surge test for instance. This fault is latched and operations will be resumed like in a case of  $V_{CC}$  Over Voltage Protection.



- V<sub>out</sub> Over Voltage Protection:** if the internally-built output voltage becomes higher than  $V_{OVP}$  level ( $V_{ref\_CV1} + 26\%$ ) a fault is detected.
  - A & C version:** This fault is latched and operations are resumed like in the **V<sub>CC</sub> Over Voltage Protection** case.
  - B version:** the part enters in double hiccup mode before resuming operations.
- V<sub>out</sub> Under Voltage Protection:** After each circuit power on sequence,  $V_{out}$  UVP detection is enabled only after the startup timer  $T_{EN\_UVP}$ . This timer ensures that the power supply is able to fuel the output capacitor before checking the output voltage in on target. After this startup blanking time, UVP detection is enabled and monitors the Output voltage level. When the power supply is running in constant-current mode and when the output voltage falls below  $V_{UVP}$  level, the controller stops sending drive pulses and enters a double hiccup mode before resuming operations (A & B version), or latches off (C version).
- V<sub>s</sub>/ZCD Pin Short Protection:** at the beginning of each off-time period, the  $V_s/ZCD$  pin is tested to check whether it is shorted or left open. In case a fault is detected, the controller enters in a double hiccup mode before resuming operations.
- Temperature Shutdown:** if the junction temperature reaches the  $T_{SHTDN}$  level, the controller stop driving the

power mosfet until the junction temperature decreases by  $T_{SHTDN(HYS)}$ , then the operation is resumed after a double hiccup mode.

**Startup Operation**

The high-voltage startup current source is connected to the bulk capacitor via the  $HV$  pin, it charges the  $V_{CC}$  capacitor. During startup phase, it delivers 100  $\mu A$  to fuel the  $V_{CC}$  capacitor. When  $V_{CC}$  pin reaches  $V_{CC(on)}$  level, the NCP1361/66 is enabled. Before sending the first drive pulse to the power MOSFET, the  $CS$  pin has been tested for an open or shorted situation. If  $CS$  pin is properly wired, then the controller sends the first drive pulse to the power MOSFET. After sending these first pulses, the controller checks the correct  $V_s/ZCD$  pin wiring. Considering the  $V_s/ZCD$  pin properly wired, the controller engages a softstart sequence. The softstart sequence controls the max peak current from the minimal frozen primary peak current ( $V_{CS(VCO)} = 120\text{ mV}$ : 15% of  $V_{LLIM}$ ) to the nominal pulse width by smoothly increasing the level.

Figure 40 illustrates a standard connection of the  $HV$  pin to the bulk capacitor. If the controller is in a latched fault mode (ex  $V_{CC\_OVP}$  has been detected), the power supply will resume the operation after unplugging the converter from the ac line outlet. Due the extremely low controller consumption in latched mode, the release of the latch could be very long. The unplug duration for releasing the latch will be dependent on the bulk capacitor size.

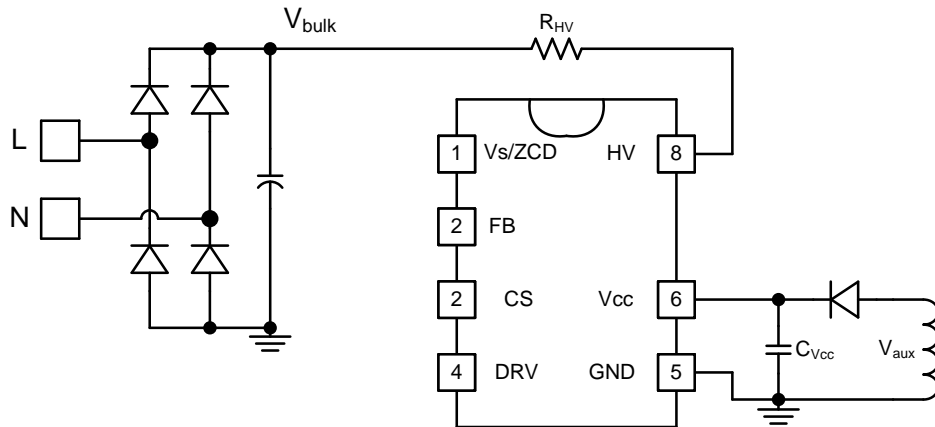


Figure 40. HV Startup Connection to the Bulk Capacitor (NCP1366)

The following calculation illustrates the time needed for releasing the latch state:

$$t_{unplug} > \frac{C_{bulk} V_{in\_ac} \sqrt{2}}{I_{HV}} \quad (\text{eq. 1})$$

For the following typical application with a 10  $\mu F$  bulk capacitor and a wide mains input range, in the worst case the power supply needs to be unplug at least for 38 seconds @ 265 V ac and 12 seconds @ 85 Vac. It is important to note that the previous recommendation is no longer valid with the B version, as all the faults are set to autorecovery mode only.

**Protecting the Controller Against Negative Spikes**

As with any controller built upon a CMOS technology, it is the designer's duty to avoid the presence of negative spikes on sensitive pins. Negative injection has the bad habit to forward-bias the controller substrate and can induce erratic behaviors. Sometimes, the injection can be so strong that internal parasitic SCRs are triggered and latch the controller. The  $HV$  pin can be the problem in certain circumstances. During the turn-off sequence, e.g. when the user unplugs the power supply, the controller is still fed by its  $V_{CC}$  capacitor and keeps activating the MOSFET ON and

OFF with a peak current limited by  $R_{sense}$ . Unfortunately, if the quality factor  $Q$  of the resonating network formed by  $L_p$  and  $C_{bulk}$  is high (e.g. the MOSFET  $R_{DS(on)} + R_{sense}$  are small), conditions are met to make the circuit resonate and a negative ringing can potentially appear at the  $HV$  pin.

Simple and inexpensive cures exist to prevent the internal parasitic SCR activation. One of them consist of inserting a resistor in series with the  $HV$  pin to keep the negative current at the lowest when the bulk swings negative (Figure 40).

Another option (Figure 41) consists of connecting the  $HV$  pin directly to the line or neutral input via a high-voltage diode. This configuration offers the benefits to release a latch state immediately after unplugging the power supply from the mains outlet. There is no delay for resetting the controller as there no capacitor keeps the  $HV$  bias.

$R_{HV}$  resistor value must be sized as follow in order to guarantee a correct behavior of the  $HV$  startup in the worst case conditions:

$$R_{HV} < \frac{V_{in,ac\_min} \sqrt{2} - V_{HV(min)\_max}}{I_{HV\_max}} \quad (eq. 2)$$

Where:

- $V_{in,ac\_min}$  is minimal input voltage, for example 85 V ac for universal input mains.
- $V_{HV(min)\_max}$  is the worst case of the minimal input voltage needed for the  $HV$  startup current source (25 V-max).
- $I_{HV\_max}$  is the maximum current delivered by the  $HV$  startup current source (150  $\mu$ A-max)

With this typical example

$$R_{HV} < \frac{85 \sqrt{2} - 25}{150 \mu} = 633 \text{ k}\Omega,$$

then any value below this one will be ok.

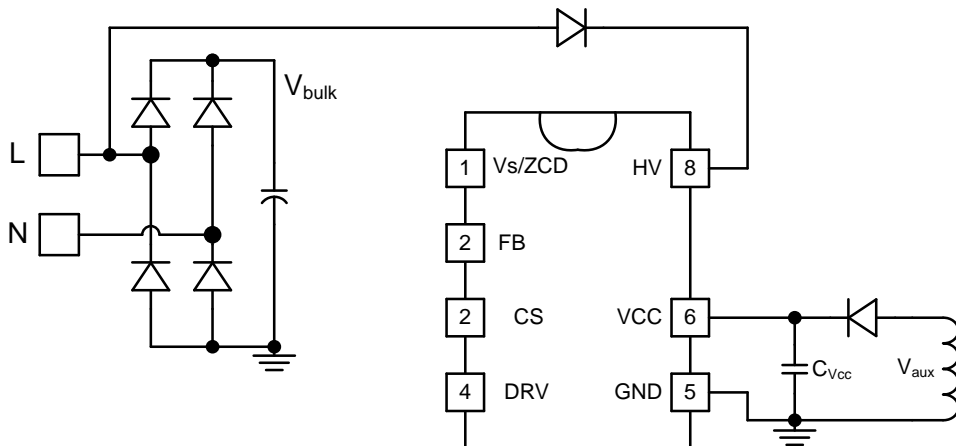


Figure 41. Recommended HV Startup Connection for Fast Release after a Latched Fault (NCP1366)

**Primary Side Regulation: Constant Current Operation**

Figure 42 portrays idealized primary and secondary transformer currents of a flyback converter operating in Discontinuous Conduction Mode (DCM).

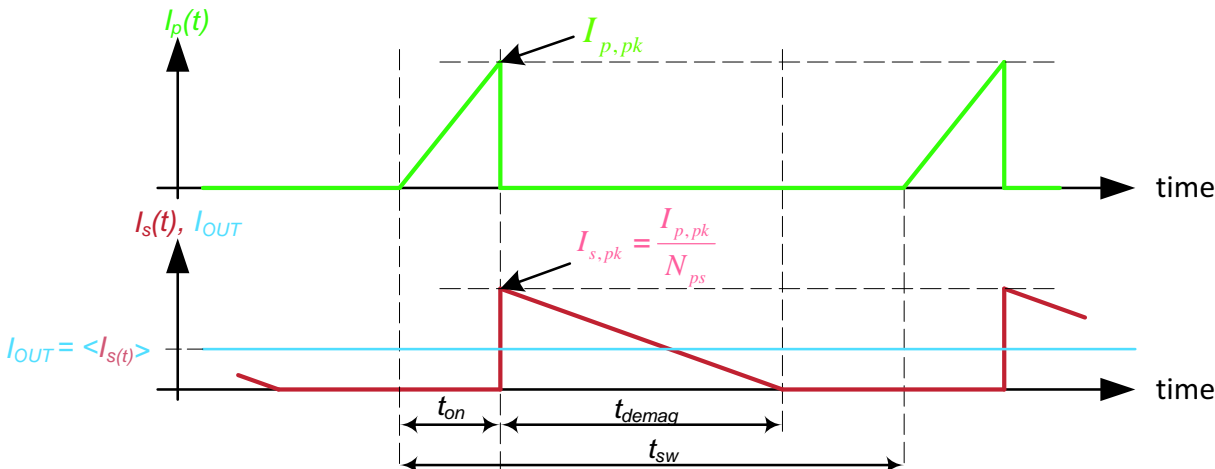


Figure 42. Primary and Secondary Transformer Current Waveforms

When the primary power MOSFET is turned on, the primary current is illustrated by the green curve of Figure 42. When the power MOSFET is turned off the primary side current drops to zero and the current into the secondary winding immediately rises to its peak value equal to the primary peak current divided by the primary to secondary turns ratio. This is an ideal situation in which the leakage inductance action is neglected.

The output current delivered to the load is equal to the average value of the secondary winding current, thus we can write:

$$I_{out} = \langle i_{sec}(t) \rangle = \frac{I_{p,pk} t_{demag}}{2N_{ps} t_{sw}} \quad (\text{eq. 3})$$

Where:

- $t_{sw}$  is the switching period
- $t_{demag}$  is the demagnetizing time of the transformer
- $N_{ps}$  is the secondary to primary turns ratio, where  $N_p$  and  $N_s$  are respectively the transformer primary and secondary turns:

$$N_{ps} = \frac{N_s}{N_p} \quad (\text{eq. 4})$$

- $I_{p,pk}$  is the magnetizing peak current sensed across the sense resistor on CS pin:

$$I_{p,pk} = \frac{V_{CS}}{R_{sense}} \quad (\text{eq. 5})$$

Internal constant current regulation block is building the constant current feedback information as follow:

$$V_{FB\_CC} = V_{ref\_CC} \frac{t_{sw}}{t_{demag}} \quad (\text{eq. 6})$$

As the controller monitors the primary peak current via the sense resistor and due to the internal current setpoint divider ( $K_{comp}$ ) between the CS pin and the internal feedback information, the output current could be written as follow:

$$I_{out} = \frac{V_{ref\_CC}}{8N_{ps}R_{sense}} \quad (\text{eq. 7})$$

The output current value is set by choosing the sense resistor value:

$$R_{sense} = \frac{V_{ref\_CC}}{8N_{ps}I_{out}} \quad (\text{eq. 8})$$

When the power MOSFET is released at the end of the on time, because of the transformer leakage inductance and the drain lumped capacitance some voltage ringing appears on the drain node. These voltage ringings are also visible on the auxiliary winding and could cheat the controller detection circuits. To avoid false detection operations, two protecting circuits have been implemented on the  $V_s/ZCD$  pin (see Figure 43):

1. An internal switch grounds the  $V_s/ZCD$  pin during  $t_{on} + t_{short\_ZCD}$  in order to protect the pin from negative voltage.
2. In order to prevent any misdetection from the zero crossing block an internal switch disconnects  $V_s/ZCD$  pin until  $t_{blank\_ZCD}$  time (1.5  $\mu$ s typ.) ends.

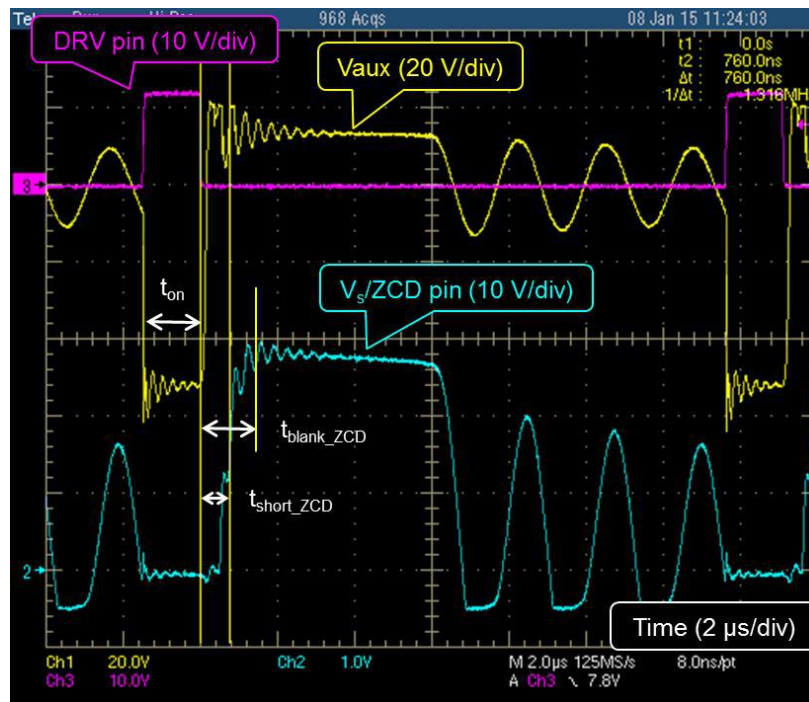


Figure 43.  $V_s/ZCD$  Pin Waveforms

**Constant-Current and Constant-Voltage Overall Regulation:**

As already presented in the two previous paragraphs, the controller integrates two different feedback loops: the first one deals with the constant-current regulation scheme while the second one builds the constant-voltage regulation with an opto-based voltage loop. One of the two feedback paths sets the primary peak current into the transformer. During startup phase, however, the peak current is controlled by the soft-start.

**Zero Current Detection**

The NCP1361/66 integrates a quasi-resonant (QR) flyback controller. The power switch turn-off of a QR converter is determined by the peak current whose value depends on the feedback loop. The switch restart event is determined by the transformer demagnetization end. The

demagnetization end is detected by monitoring the transformer auxiliary winding voltage. Turning on the power switch once the transformer is demagnetized (or reset) reduces turn-on switching losses. Once the transformer is demagnetized, the drain voltage starts ringing at a frequency determined by the transformer magnetizing inductance and the drain lumped capacitance, eventually settling at the input voltage value. A QR controller takes advantage of the drain voltage ringing and turns on the power switch at the drain voltage minimum or “valley” to reduce turn-on switching losses and electromagnetic interference (EMI).

As sketched by Figure 44, a valley is detected once the ZCD pin voltage falls below the QR flyback demagnetization threshold,  $V_{ZCD(TH)}$ , typically 45 mV. The controller will switch once the valley is detected or increment the valley counter depending on FB voltage.

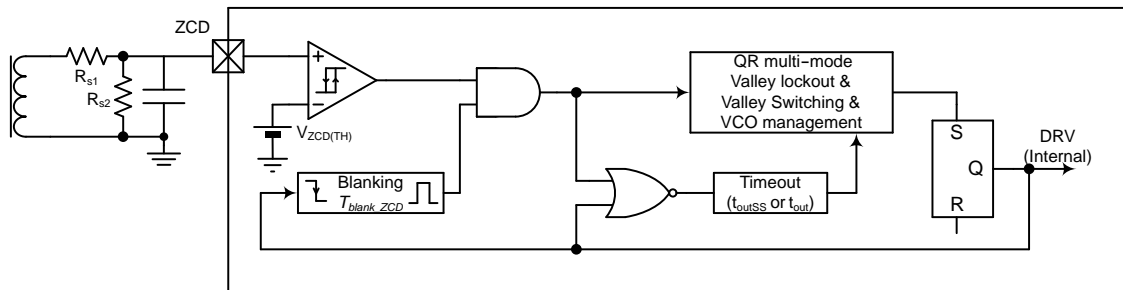


Figure 44. Valley Lockout Detection Circuitry internal Schematic

**Timeout**

The *ZCD* block actually detects falling edges of the auxiliary winding voltage applied to the *ZCD* pin. At start-up or during other transient phases, the *ZCD* comparator may be unable to detect such an event. Also, in the case of extremely damped oscillations, the system may not succeed in detecting all the valleys required by valley lockout operation (VLO, see next section). In this condition, the NCP1361/66 ensures continued operation by incorporating a maximum timeout period that resets itself when a demagnetization phase is properly detected. In case the ringing signal is too weak or heavily damped, the timeout signal supersedes the *ZCD* signal for the valley counter. Figure 44 shows the timeout period generator circuit schematic. The timeout duration,  $t_{out}$ , is set to 5.5  $\mu$ s (typ.).

During startup, the output voltage is still low, leading to long demagnetization phase, difficult to detect since the auxiliary winding voltage is small as well. In this condition, the  $t_{out}$  timeout is generally shorter than the inductor demagnetization period and if used to restart a switching cycle, it can cause continuous current mode (CCM) operation for a few cycles until the voltage on the *ZCD* pin is high enough for proper valleys detection. A longer timeout period,  $t_{outSS}$ , (typically 44  $\mu$ s) is therefore set during soft-start to prevent CCM operation.

In VLO operation, the timeout occurrences are counted instead of valleys when the drain-source voltage oscillations are too damped to be detected. For instance, assume the circuit must turn on at the third valley and the *ZCD* ringing only enables the detection of:

- Valleys #1 to #2: the circuit generates a *DRV* pulse  $t_{out}$  (steady-state timeout delay) after valley #2 detection.

- Valley #1: the timeout delay must run twice so that the circuit generates a *DRV* pulse 10  $\mu$ s ( $2 * t_{out}$  typ.) after valley #1 detection.

**Valley LockOut (VLO) and Frequency Foldback (FF)**

The operating frequency of a traditional Quasi-Resonant (QR) flyback controller is inversely proportional to the system load. In other words, a load reduction increases the operating frequency. A maximum frequency clamp can be useful to limit the operating frequency range. However, when associated with a valley-switching circuit, instabilities can arise because of the discrete frequency jumps. The controller tends to hesitate between two valleys and audible noise can be generated

To avoid this issue, the NCP1361/66 incorporates a proprietary valley lockout circuitry which prevents so-called valley jumping. Once a valley is selected, the controller stays locked in this valley until the input level or output power changes significantly. This technique extends QR operation over a wider output power range while maintaining good efficiency and naturally limiting the maximum operating frequency.

The operating valley (from 1<sup>st</sup> to 4<sup>th</sup> valley) is determined by the internal feedback level (*FB* node on Figure 4). As *FB* voltage level decreases or increases, the valley comparators toggle one after another to select the proper valley.

The decimal counter increases each time a valley is detected. The activation of an “n” valley comparator blanks the “n-1” or “n+1” valley comparator output depending if  $V_{FB}$  decreases or increases, respectively. Figure 45 shows a typical frequency characteristic obtained at low line in a 10 W charger.

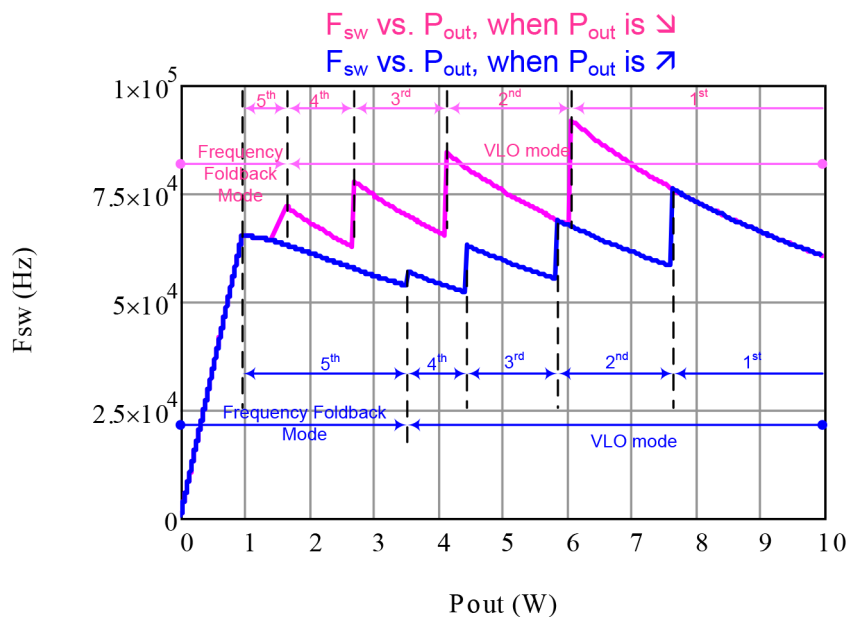


Figure 45. Typical Switching Frequency versus Output Power Relationship in a 10 W Adapter

## NCP1361, NCP1366

When an “n” valley is asserted by the valley selection circuitry, the controller locks in this valley until the  $FB$  voltage decreases to the lower threshold (“n+1” valley activates) or increases to the “n valley threshold” + 600 mV (“n-1” valley activates). The regulation loop adjusts the

peak current to deliver the necessary output power at the valley operating point. Each valley selection comparator features a 600 mV hysteresis that helps stabilize operation despite the  $FB$  voltage swing produced by the regulation loop.

**Table 1. VALLEY FB THRESHOLD ON CONSTANT VOLTAGE REGULATION**

| FB Falling                                |       | FB Rising                                 |       |
|---|-------|---|-------|
| 1 <sup>st</sup> to 2 <sup>nd</sup> valley | 2.5 V | FF mode to 4 <sup>th</sup>                | 2.5 V |
| 2 <sup>nd</sup> to 3 <sup>rd</sup> valley | 2.3 V | 4 <sup>th</sup> to 3 <sup>rd</sup> valley | 2.7 V |
| 3 <sup>rd</sup> to 4 <sup>th</sup> valley | 2.1 V | 3 <sup>rd</sup> to 2 <sup>nd</sup> valley | 2.9 V |
| 4 <sup>th</sup> to FF mode                | 1.9 V | 2 <sup>nd</sup> to 1 <sup>st</sup> valley | 3.1 V |

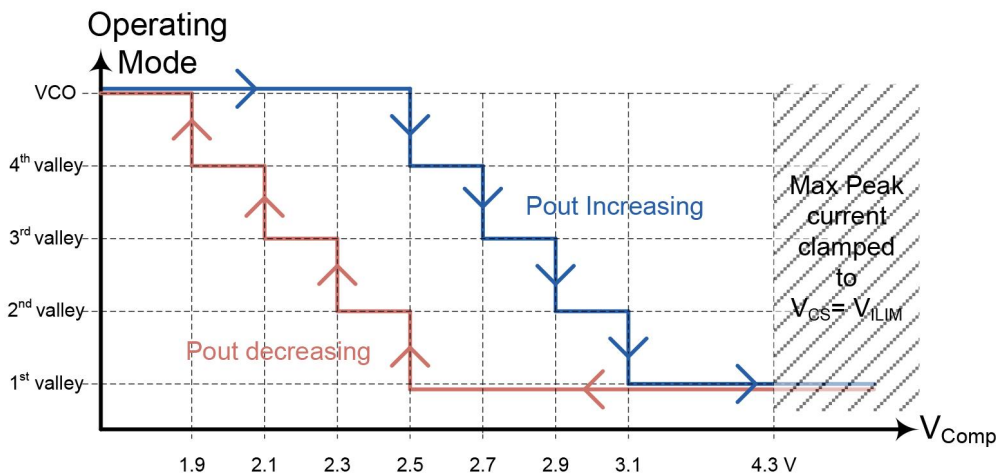
### Frequency Foldback (FF)

As the output current decreases ( $FB$  voltage decreases), the valleys are incremented from 1 to 4. In case the fourth valley is reached, the  $FB$  voltage further decreases below 1.9 V and the controller enters the frequency foldback mode (FF). The current setpoint being internally forced to remain above 0.12 V (setpoint corresponding to  $V_{Comp} = 1.9$  V), the controller regulates the power delivery by modulating the switching frequency. When an output current increase causes  $FB$  to exceed the 2.5 V FF upper threshold (600 mV hysteresis), the circuit recovers  $VLO$  operation.

In frequency foldback mode, the system reduces the switching frequency by adding some dead-time after the 4<sup>th</sup> valley is detected. However, in order to keep the high

efficiency benefit inherent to the QR operation, the controller turns on again with the next valley after the dead time has ended. As a result, the controller will still run in valley switching mode even when the FF is enabled. This dead-time increases when the  $FB$  voltage decays. There is no discontinuity when the system transitions from  $VLO$  to FF and the frequency smoothly reduces as  $FB$  goes below 1.9 V.

The dead-time is selected to generate a 2  $\mu$ s dead-time when  $V_{Comp}$  is decreasing and crossing  $V_{HVCOI}$  (1.9 V typ.). At this moment, it can linearly go down to the minimal frequency limit ( $f_{VCO(min)} = 200, 600$  or 1200 Hz version are available). The generated dead-time is 1  $\mu$ s when  $V_{Comp}$  is increasing and crossing  $V_{HVCOI}$  (2.5 V typ.).



**Figure 46. Valley Lockout Threshold**

### Current Setpoint

As explained in this operating description, the current setpoint is affected by several functions. Figure 47 summarizes these interactions. As shown by this figure, the current setpoint is the output of the control law divided by  $K_{comp}$  (4 typ.). This current setpoint is clamped by the soft-start slope as long as the peak current requested by the  $FB\_CV$  or  $FB\_CC$  level are higher. The softstart clamp is

starting from the frozen peak current ( $V_{CS(VCO)} = 120$  mV typ.) to  $V_{ILIM}$  (0.8 V typ.) within 4 ms ( $t_{ss}$ ).

However, this internal  $FB$  value is also limited by the following functions:

- A minimum setpoint is forced that equals  $V_{CS(VCO)}$  (0.12 V, typ.)
- In addition, a second  $OCF$  comparator ensures that in any case the current setpoint is limited to  $V_{ILIM}$ .



This ensures the MOSFET current setpoint remains limited to  $V_{ILIM}$  in a fault condition.

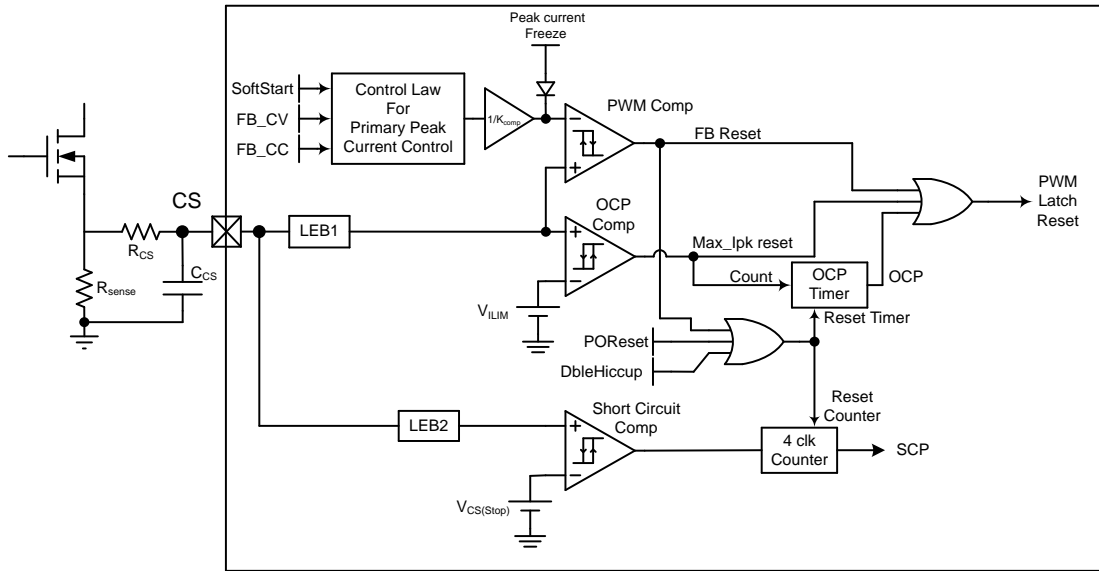


Figure 47. Current Setpoint

### A 2nd Over-Current Comparator for Abnormal Overcurrent Fault Detection

A severe fault like a winding short-circuit can cause the switch current to increase very rapidly during the on-time. The current sense signal significantly exceeds  $V_{ILIM}$ . But, because the current sense signal is blanked by the LEB circuit during the switch turn on, the power switch current can abnormally increase, possibly causing system damages. The NCP1361/66 protects against this dangerous mode by adding an additional comparator for abnormal overcurrent fault detection or short-circuit condition. The current sense signal is blanked with a shorter LEB duration,  $t_{LEB2}$ , typically 120 ns, before applying it to the short-circuit comparator. The voltage threshold of this extra comparator,  $V_{CS(stop)}$ , is typically 1.2 V, set 50% higher than  $V_{ILIM}$ . This is to avoid interference with normal operation. Four consecutive abnormal overcurrent faults cause the controller to enter in auto-recovery mode. The count to 4 provides noise immunity during surge testing. The counter is reset each time a  $DRV$  pulse occurs without activating the fault overcurrent comparator or after double hiccup sequence or if the power supply is unplugged with a new startup sequence after the initial power on reset.

### Standby Power Optimization

Assuming the no-load standby power is a critical parameter, the NCP1361/66 is optimized to reach an ultra low standby power. When the controller enters standby mode, a part of the internal circuitry has been disabled in order to minimize its supply current. When the STBY mode is enabled, the consumption is only 200  $\mu A$  ( $I_{CC4}$ ) with the 200 Hz minimal frequency option.

### Fault mode and Protection

- ◆  $CS$  pin: at each startup, a 55  $\mu A$  ( $I_{CS}$ ) current source pulls up the  $CS$  pin to disable the controller if the pin is left open or grounded. Then the controller enters in a double hiccup mode.
- ◆  $V_S/ZCD$  pin: after sending the first drive pulse the controller checks the correct wiring of  $V_S/ZCD$  pin: after the  $ZCD$  blanking time, if there is an open or short conditions, the controller enters in double hiccup mode.

**Thermal Shutdown:** An internal thermal shutdown circuit monitors the junction temperature of the IC. The controller is disabled if the junction temperature exceeds the thermal shutdown threshold ( $T_{SHDN}$ ), typically 150°C. A continuous  $V_{CC}$  hiccup is initiated after a thermal shutdown fault is detected. The controller restarts at the next  $V_{CC(on)}$  once the IC temperature drops below  $T_{SHDN}$  reduced by the thermal shutdown hysteresis ( $T_{SHDN(HYS)}$ ), typically 40°C. The thermal shutdown is also cleared if  $V_{CC}$  drops below  $V_{CC(reset)}$ . A new power up sequences commences at the next  $V_{CC(on)}$  once all the faults are removed.

### Driver

The NCP1361/66 maximum supply voltage,  $V_{CC(max)}$ , is 28 V. Typical high-voltage MOSFETs have a maximum gate voltage rating of 20 V. The  $DRV$  pin incorporates an active voltage clamp which limits the gate voltage on the external mosfet. The  $DRV$  voltage clamp,  $V_{DRV(high)}$  is set to 13 V maximum.

# NCP1361, NCP1366

**TABLE OF AVAILABLE OPTIONS**

| Function                                       | Options  |
|--|--|
| Fault Mode                                     | $V_{CC\_OVP}$ Latched / Full Autorecovery / $V_{out\_UVP}$ latched |
| Minimum operating frequency in VCO             | 200 Hz / 600 Hz / 1.2 kHz / 23 kHz                                 |
| Frequency Clamp or Maximum operating frequency | No Clamp / 80 kHz / 110 kHz  |

**ORDERING TABLE OPTION**

| OPN #<br>NCP136_----- | HV Startup |    | Fault Mode                                 |                      |                 |   | Min Operating F <sub>sw</sub> (STBY) |           |            |           |            | Frequency Clamp |           |            | Frozen Peak Current V <sub>CS(VCO)</sub> |           |           |
|-----------------------|------------|----|--|----------------------|-----------------|---|--------------------------------------|-----------|------------|-----------|------------|-----------------|-----------|------------|--|-----------|-----------|
|                       | 6          | 1  | A  | B                    | C               | E   | A                                    | B         | C          | D         | E          | A               | B         | C          | X  | Y         | Z         |
|                       | Yes        | No | $V_{CC\_OVP}$<br>$V_{OUT\_OVP}$<br>Latched | Full<br>Autorecovery | Full<br>Latched | Full<br>Autorecovery<br>$V_{OVP} = 3.6\text{ V}$<br>$V_{UVP} = 0.75\text{ V}$ | 200<br>Hz                            | 600<br>Hz | 1.2<br>kHz | 23<br>kHz | No<br>Min. | No              | 80<br>kHz | 110<br>kHz | 120<br>mV                                | 160<br>mV | 200<br>mV |
| NCP1366AABAY          | X          |    | X  |                      |                 |   | X                                    |           |            |           |            |                 | X         |            |  | X         |           |
| NCP1366BABAY          | X          |    |  | X                    |                 |   | X                                    |           |            |           |            |                 | X         |            |  | X         |           |
| NCP1366CABAY          | X          |    |  |                      | X               |   | X                                    |           |            |           |            |                 | X         |            |  | X         |           |
| NCP1366EABAY          | X          |    |  |                      |                 | X   | X                                    |           |            |           |            |                 | X         |            |  | X         |           |
| NCP1361AABAY          |            | X  | X  |                      |                 |   | X                                    |           |            |           |            |                 | X         |            |  | X         |           |
| NCP1361BABAY          |            | X  |  | X                    |                 |   | X                                    |           |            |           |            |                 | X         |            |  | X         |           |
| NCP1361CABAY          |            | X  |  |                      | X               |   | X                                    |           |            |           |            |                 | X         |            |  | X         |           |
| NCP1361EABAY          |            | X  |  |                      |                 | X   | X                                    |           |            |           |            |                 | X         |            |  | X         |           |



## NCP1361, NCP1366

### ORDERING INFORMATION

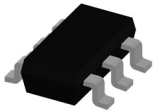
| Device            | Marking | Package             | Shipping†          |
|-------------------|---------|---------------------|--------------------|
| NCP1366AABAYDR2G  | 1366A1  | SOIC-7<br>(Pb-Free) | 2500 / Tape & Reel |
| NCP1366BABAYDR2G  | 1366B1  | SOIC-7<br>(Pb-Free) | 2500 / Tape & Reel |
| NCP1361EABAYSNT1G | ACU     | TSOP-6<br>(Pb-Free) | 3000 / Tape & Reel |

### DISCONTINUED (Note 5)

|                   |        |                     |                    |
|-------------------|--------|---------------------|--------------------|
| NCP1366EABAYDR2G  | 1366E1 | SOIC-7<br>(Pb-Free) | 2500 / Tape & Reel |
| NCP1361AABAYSNT1G | ADE    | TSOP-6<br>(Pb-Free) | 3000 / Tape & Reel |
| NCP1361BABAYSNT1G | ADF    | TSOP-6<br>(Pb-Free) | 3000 / Tape & Reel |

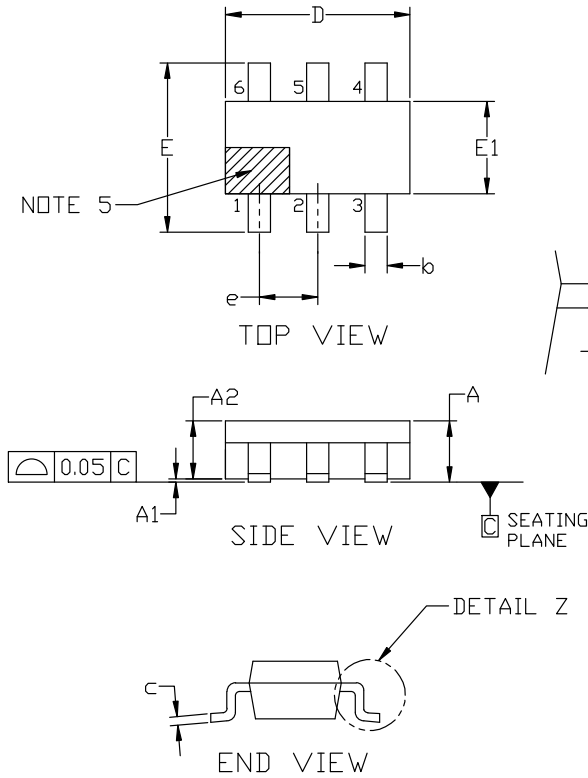
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

5. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on [www.onsemi.com](http://www.onsemi.com).



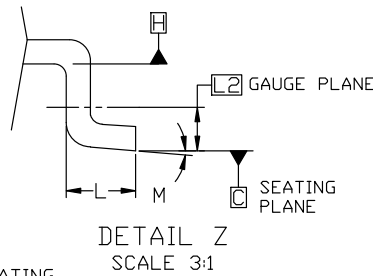
**TSOP-6 3.00x1.50x0.90, 0.95P**  
**CASE 318G**  
**ISSUE W**

DATE 26 FEB 2024

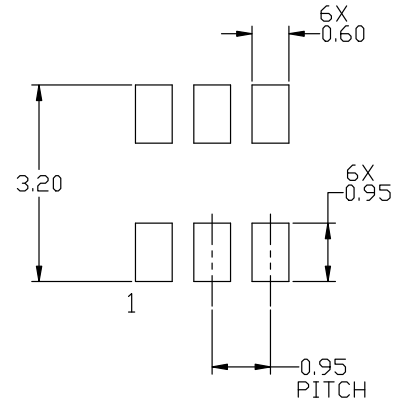


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE



| MILLIMETERS |          |      |      |
|-------------|----------|------|------|
| DIM         | MIN      | NOM  | MAX  |
| A           | 0.90     | 1.00 | 1.10 |
| A1          | 0.01     | 0.06 | 0.10 |
| A2          | 0.80     | 0.90 | 1.00 |
| b           | 0.25     | 0.38 | 0.50 |
| c           | 0.10     | 0.18 | 0.26 |
| D           | 2.90     | 3.00 | 3.10 |
| E           | 2.50     | 2.75 | 3.00 |
| E1          | 1.30     | 1.50 | 1.70 |
| e           | 0.85     | 0.95 | 1.05 |
| L           | 0.20     | 0.40 | 0.60 |
| L2          | 0.25 BSC |      |      |
| M           | 0°       | ---  | 10°  |



RECOMMENDED MOUNTING FOOTPRINT

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

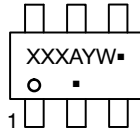
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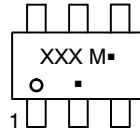
**TSOP-6 3.00x1.50x0.90, 0.95P**  
**CASE 318G**  
**ISSUE W**

DATE 26 FEB 2024

**GENERIC  
MARKING DIAGRAM\***



**IC**



**STANDARD**

|                            |                            |
|----------------------------|----------------------------|
| XXX = Specific Device Code | XXX = Specific Device Code |
| A = Assembly Location      | M = Date Code              |
| Y = Year                   | ▪ = Pb-Free Package        |
| W = Work Week              |                            |
| ▪ = Pb-Free Package        |                            |

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

- |  |  |   |   |   |  |
|--|--|---|---|---|--|
| <b>STYLE 1:</b><br>PIN 1. DRAIN<br>2. DRAIN<br>3. GATE<br>4. SOURCE<br>5. DRAIN<br>6. DRAIN              | <b>STYLE 2:</b><br>PIN 1. EMITTER 2<br>2. BASE 1<br>3. COLLECTOR 1<br>4. EMITTER 1<br>5. BASE 2<br>6. COLLECTOR 2    | <b>STYLE 3:</b><br>PIN 1. ENABLE<br>2. N/C<br>3. R BOOST<br>4. Vz<br>5. V in<br>6. V out                            | <b>STYLE 4:</b><br>PIN 1. N/C<br>2. V in<br>3. NOT USED<br>4. GROUND<br>5. ENABLE<br>6. LOAD                | <b>STYLE 5:</b><br>PIN 1. EMITTER 2<br>2. BASE 2<br>3. COLLECTOR 1<br>4. EMITTER 1<br>5. BASE 1<br>6. COLLECTOR 2 | <b>STYLE 6:</b><br>PIN 1. COLLECTOR<br>2. COLLECTOR<br>3. BASE<br>4. EMITTER<br>5. COLLECTOR<br>6. COLLECTOR |
| <b>STYLE 7:</b><br>PIN 1. COLLECTOR<br>2. COLLECTOR<br>3. BASE<br>4. N/C<br>5. COLLECTOR<br>6. EMITTER   | <b>STYLE 8:</b><br>PIN 1. Vbus<br>2. D(in)<br>3. D(in)+<br>4. D(out)+<br>5. D(out)<br>6. GND                         | <b>STYLE 9:</b><br>PIN 1. LOW VOLTAGE GATE<br>2. DRAIN<br>3. SOURCE<br>4. DRAIN<br>5. DRAIN<br>6. HIGH VOLTAGE GATE | <b>STYLE 10:</b><br>PIN 1. D(OUT)+<br>2. GND<br>3. D(OUT)-<br>4. D(IN)-<br>5. VBUS<br>6. D(IN)+             | <b>STYLE 11:</b><br>PIN 1. SOURCE 1<br>2. DRAIN 2<br>3. DRAIN 2<br>4. SOURCE 2<br>5. GATE 1<br>6. DRAIN 1/GATE 2  | <b>STYLE 12:</b><br>PIN 1. I/O<br>2. GROUND<br>3. I/O<br>4. I/O<br>5. VCC<br>6. I/O                          |
| <b>STYLE 13:</b><br>PIN 1. GATE 1<br>2. SOURCE 2<br>3. GATE 2<br>4. DRAIN 2<br>5. SOURCE 1<br>6. DRAIN 1 | <b>STYLE 14:</b><br>PIN 1. ANODE<br>2. SOURCE<br>3. GATE<br>4. CATHODE/DRAIN<br>5. CATHODE/DRAIN<br>6. CATHODE/DRAIN | <b>STYLE 15:</b><br>PIN 1. ANODE<br>2. SOURCE<br>3. GATE<br>4. DRAIN<br>5. N/C<br>6. CATHODE                        | <b>STYLE 16:</b><br>PIN 1. ANODE/CATHODE<br>2. BASE<br>3. EMITTER<br>4. COLLECTOR<br>5. ANODE<br>6. CATHODE | <b>STYLE 17:</b><br>PIN 1. EMITTER<br>2. BASE<br>3. ANODE/CATHODE<br>4. ANODE<br>5. CATHODE<br>6. COLLECTOR       |  |

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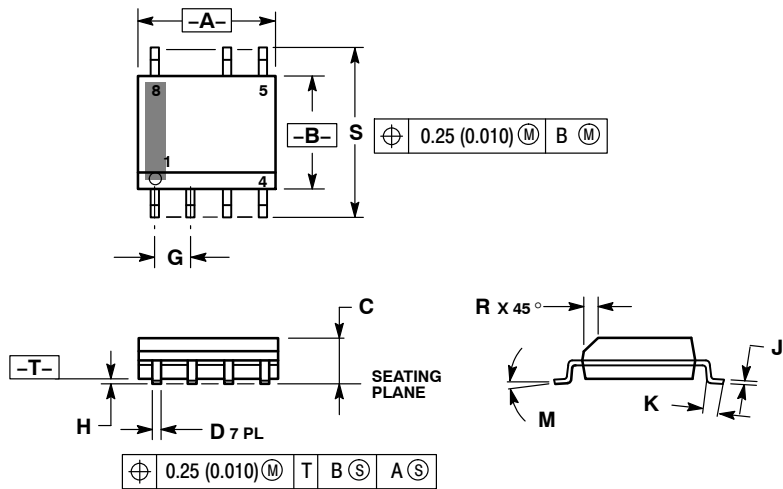
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ISSUE E

DATE 20 OCT 2009

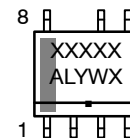


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B ARE DATUMS AND T IS A DATUM SURFACE.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 0.10        | 0.25 | 0.004     | 0.010 |
| J   | 0.19        | 0.25 | 0.007     | 0.010 |
| K   | 0.40        | 1.27 | 0.016     | 0.050 |
| M   | 0° - 8°     |      | 0° - 8°   |       |
| N   | 0.25        | 0.50 | 0.010     | 0.020 |
| S   | 5.80        | 6.20 | 0.228     | 0.244 |

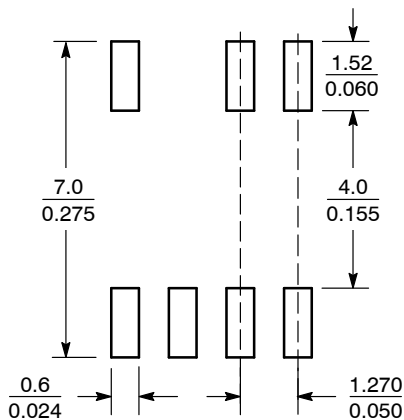
GENERIC MARKING DIAGRAM



- XXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

SOLDERING FOOTPRINT\*



SCALE 6:1 (mm/inches)

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, [SOLDERRM/D](#).

STYLES ON PAGE 2

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**SOIC-7**  
**CASE 751U**  
**ISSUE E**

DATE 20 OCT 2009

- |  |  |   |
|--|--|---|
| <p>STYLE 1:<br/>         PIN 1. EMITTER<br/>         2. COLLECTOR<br/>         3. COLLECTOR<br/>         4. EMITTER<br/>         5. EMITTER<br/>         6.<br/>         7. NOT USED<br/>         8. EMITTER</p>                         | <p>STYLE 2:<br/>         PIN 1. COLLECTOR, DIE, #1<br/>         2. COLLECTOR, #1<br/>         3. COLLECTOR, #2<br/>         4. COLLECTOR, #2<br/>         5. BASE, #2<br/>         6. EMITTER, #2<br/>         7. NOT USED<br/>         8. EMITTER, #1</p>                     | <p>STYLE 3:<br/>         PIN 1. DRAIN, DIE #1<br/>         2. DRAIN, #1<br/>         3. DRAIN, #2<br/>         4. DRAIN, #2<br/>         5. GATE, #2<br/>         6. SOURCE, #2<br/>         7. NOT USED<br/>         8. SOURCE, #1</p>   |
| <p>STYLE 4:<br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. ANODE<br/>         4. ANODE<br/>         5. ANODE<br/>         6. ANODE<br/>         7. NOT USED<br/>         8. COMMON CATHODE</p>                          | <p>STYLE 5:<br/>         PIN 1. DRAIN<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. DRAIN<br/>         5.<br/>         6.<br/>         7. NOT USED<br/>         8. SOURCE</p>  | <p>STYLE 6:<br/>         PIN 1. SOURCE<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. SOURCE<br/>         5. SOURCE<br/>         6.<br/>         7. NOT USED<br/>         8. SOURCE</p>  |
| <p>STYLE 7:<br/>         PIN 1. INPUT<br/>         2. EXTERNAL BYPASS<br/>         3. THIRD STAGE SOURCE<br/>         4. GROUND<br/>         5. DRAIN<br/>         6. GATE 3<br/>         7. NOT USED<br/>         8. FIRST STAGE Vd</p> | <p>STYLE 8:<br/>         PIN 1. COLLECTOR (DIE 1)<br/>         2. BASE (DIE 1)<br/>         3. BASE (DIE 2)<br/>         4. COLLECTOR (DIE 2)<br/>         5. COLLECTOR (DIE 2)<br/>         6. EMITTER (DIE 2)<br/>         7. NOT USED<br/>         8. COLLECTOR (DIE 1)</p> | <p>STYLE 9:<br/>         PIN 1. EMITTER (COMMON)<br/>         2. COLLECTOR (DIE 1)<br/>         3. COLLECTOR (DIE 2)<br/>         4. EMITTER (COMMON)<br/>         5. EMITTER (COMMON)<br/>         6. BASE (DIE 2)<br/>         7. NOT USED<br/>         8. EMITTER (COMMON)</p> |
| <p>STYLE 10:<br/>         PIN 1. GROUND<br/>         2. BIAS 1<br/>         3. OUTPUT<br/>         4. GROUND<br/>         5. GROUND<br/>         6. BIAS 2<br/>         7. NOT USED<br/>         8. GROUND</p>                           | <p>STYLE 11:<br/>         PIN 1. SOURCE (DIE 1)<br/>         2. GATE (DIE 1)<br/>         3. SOURCE (DIE 2)<br/>         4. GATE (DIE 2)<br/>         5. DRAIN (DIE 2)<br/>         6. DRAIN (DIE 2)<br/>         7. NOT USED<br/>         8. DRAIN (DIE 1)</p>                |   |

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