

NCL30160

1.0A Constant-Current Buck Regulator for Driving High Power LEDs

The NCL30160 is an NFET hysteretic step-down, constant-current driver for high power LEDs. Ideal for industrial and general lighting applications utilizing minimal external components. The NCL30160 operates with an input voltage range from 6.3 V to 40 V. The hysteretic control gives good power supply rejection and fast response during load transients and PWM dimming to LED arrays of varying number and type. A dedicated PWM input ($\overline{\text{DIM/EN}}$) enables wide range of pulsed dimming and a high switching frequency up to 1.4 MHz allows the use of smaller external components minimizing space and cost. Protection features include resistor-programmed constant LED current, shorted LED protection, under-voltage and thermal shutdown. The NCL30160 is available in a SOIC-8 package.

Features

- Integrated 1.0A MOSFET
- VIN Range 6.3 V to 40 V
- Short LED Shutdown Protection
- Up to 1.4 MHz Switching Frequency
- No Control Loop Compensation Required
- Adjustable LED Current
- Single Pin Brightness and Enable/Disable Control Using PWM
- Supports All-Ceramic Output Capacitors and Capacitor-less Outputs
- Thermal Shutdown Protection
- Capable of 100% Duty Cycle Operation
- This is a Pb-Free Device

Typical Application

- LED Driver
- Constant Current Source
- General Illumination
- Industrial Lighting



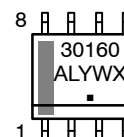
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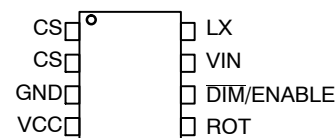
SOIC-8 NB
CASE 751

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCL30160DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCL30160

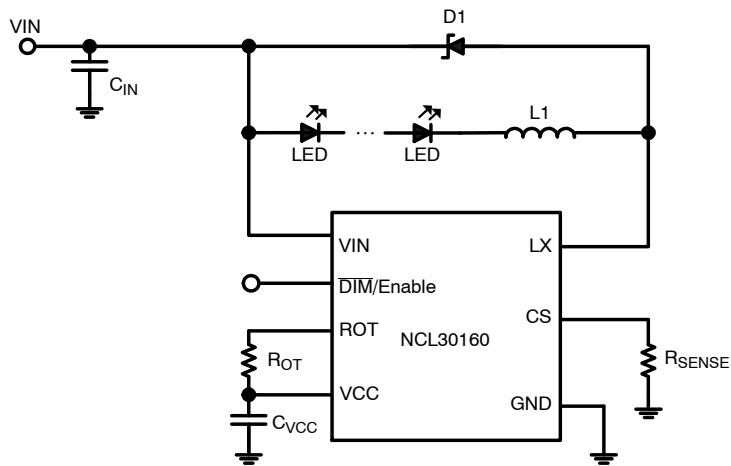


Figure 1. Typical Application Circuit

PIN FUNCTION DESCRIPTION

Pin	Pin Name	Description	Application Information
1, 2	CS	Current Sense feedback pin	Set the current through the LED array by connecting a resistor from this pin to ground.
3	GND	Ground Pin	Ground. Reference point for all voltages
4	VCC	Output of Internal 5 V linear regulator	The VCC pin supplies the power to the internal circuitry. The VCC is the output of a linear regulator which is powered from VIN. A 2 μ F ceramic capacitor is recommended for bypassing and should be placed as close as possible to the VCC and AGND pins. Do not connect to an external load.
5	ROT	Off-Time Setting Resistor	Resistor ROT from this pin to VCC sets the Off-Time range for the hysteretic controller.
6	DIM/EN	PWM Dimming Control & ENABLE	Connect a logic-level PWM signal to this pin to enable/disable the power MOSFET and LED array
7	VIN	Input Voltage Pin	Nominal operating input range is 6.3 V to 40 V. Input supply pin to the internal circuitry and the positive input to the current sense comparators. Due high frequency noise, a 10 μ F ceramic capacitor is recommended to be placed as close as possible to VIN and power ground.
8	LX	Drain of Internal Power MOSFET	The LX pin connects to the inductor and provides the switching current necessary to operate in hysteretic mode.

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MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
VIN to GND	VIN	-0.3	40	V
MOSFET Drain Voltage to GND	LX	-	40	V
VCC to GND	VCC	-	6	V
$\overline{\text{DIM}}/\text{EN}$ to GND	DIM	-0.3	6	V
CS to GND	CS	-0.3	6	V
ROT to GND	ROT	-0.3	6	V
Absolute Maximum Junction Temperature	$T_{J(\text{MAX})}$	150		°C
Operating Junction Temperature Range	T_J	-40	125	°C
Maximum LED Drive Current	ILIM	1.5		A
Storage Temperature Range	T_{stg}	-55 to +125		°C
Thermal Characteristics SOIC-8 Plastic Package Maximum Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1) Thermal Resistance Junction-to-Air (Note 2)	PD $R_{\theta\text{JA}}$	1.11 111.7		W °C/W
Lead Temperature Soldering (10 sec): Re-flow (SMD styles only) Pb-Free (Note 3)	T_L	260 peak		°C
Moisture Sensitivity Level (Note 4)	MSL	1		-

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_{J(\text{max})} - T_A}{R_{\theta\text{JA}}}$$

2. When mounted on a multi-layer board with 35 mm² copper area, using 1 oz Cu.

3. 60–180 seconds minimum above 237°C.

4. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J-STD-020A.

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ELECTRICAL CHARACTERISTICS (Unless otherwise noted: $V_{IN} = 12\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise specified.)

Symbol	Characteristics	Min	Typ	Max	Unit
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SYSTEM PARAMETERS

V_{IN}	Input Supply Voltage Range	Normal Operation	8.0		40	V
		Functional (Note 5)	6.3			
I_{Q_IN}	Quiescent Current into V_{IN}			1.5		mA
V_{CC}	Internal Regulator Output (Note 6)			5.0		V
V_{UV+}	Under-Voltage Lock-out Threshold (V_{IN} Rising)		5.5	6.0	6.5	V
V_{UV-}	Under-Voltage Lock-out Threshold (V_{IN} Falling)		5.2	5.6	6.3	V

CURRENT LIMIT AND REGULATION

V_{CS_UL}	CS Regulation Upper Limit (CS Increasing, FET Turns-OFF)	25°C	213	220	226	mV
		-40 to 125°C	209		231	
V_{CS_LL}	CS Regulation Lower Limit (CS Decreasing, FET Turns-ON)	25°C	174	180	186	mV
		-40 to 125°C	171		189	
V_{OCP}	Over Current Protect Limit (Reference to CS Pin)			500		mV
F_{SW}	Switching Frequency Range (Note 7)				1400	kHz

DIM INPUT

$V_{PWMH/L}$	PWM (DIM/EN) high level input voltage		1.4			V
V_{PWML}	PWM (DIM/EN) low level input voltage				0.4	V
I_{DIM_PU}	DIM/EN Pull-up Current			50		μA
f_{pwm}	PWM (DIM/EN) dimming frequency range		0.1		20	kHz
d_{max}	Maximum Duty Cycle (Note 7)			100		%

POWER MOSFET

V_{BRDSS}	Drain-to-Source Breakdown Voltage		40			V
I_{DSS}	Drain-to-Source Leakage Current ($V_{GS} = 0\text{ V}$, $V_{DS} = 40\text{ V}$)				10	μA
$R_{DS(on)}$	On Resistance ($I_d = 500\text{ mA}$)				55	$\text{m}\Omega$
V_{SD}	Source-Drain Body Diode (Forward On-Voltage)			0.8	1.1	V
t_{PD_Off}	Propagation Delay $V_{CS_UL} - LX_High$			35		ns

THERMAL SHUTDOWN

T_{SD}	Thermal Shutdown			165		$^\circ\text{C}$
T_{Hyst}	Thermal Hysteresis			40		$^\circ\text{C}$

OFF TIMER

t_{OFF_MIN}	Minimum Off-time			137		ns
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- The functional range of V_{IN} is the voltage range over which the device will function. Output current and internal parameters may deviate from normal values for V_{IN} and V_{CC} voltages between 6.3 V and 8 V, depending on load conditions
- V_{CC} should not be driven from a voltage higher than V_{IN} or in the absence of a voltage at V_{IN} .
- Guaranteed by design.

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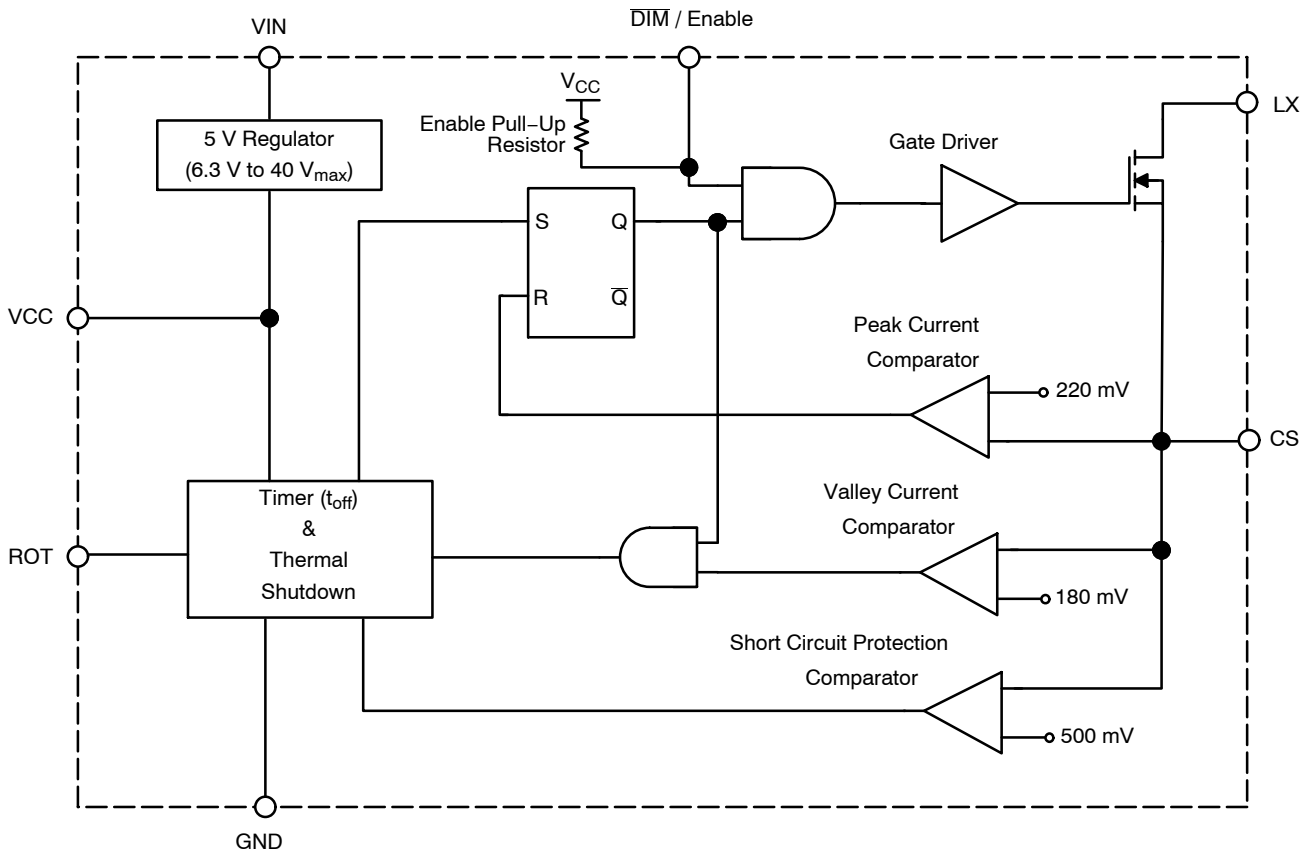


Figure 2. Simplified Block Diagram

TYPICAL APPLICATION CIRCUITS AND WAVEFORMS

($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)

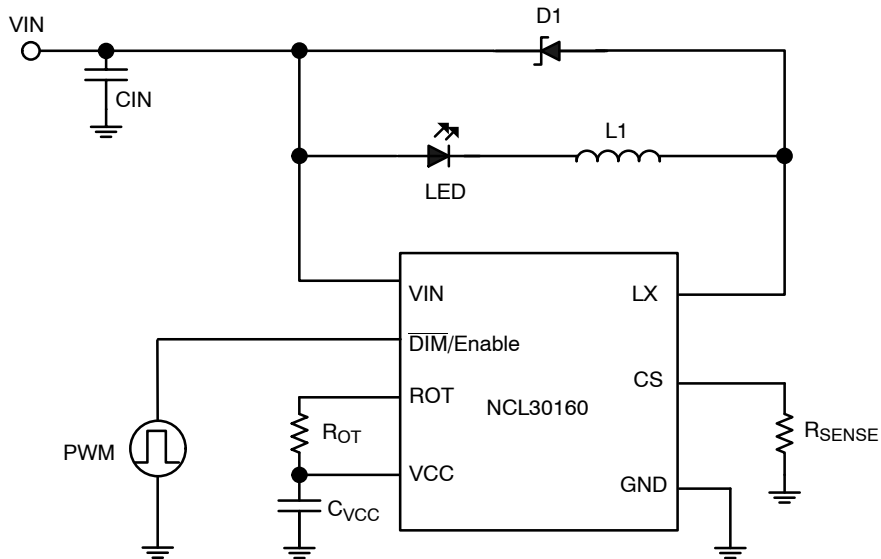


Figure 3. Typical Application Circuit To Drive One LED (Buck)

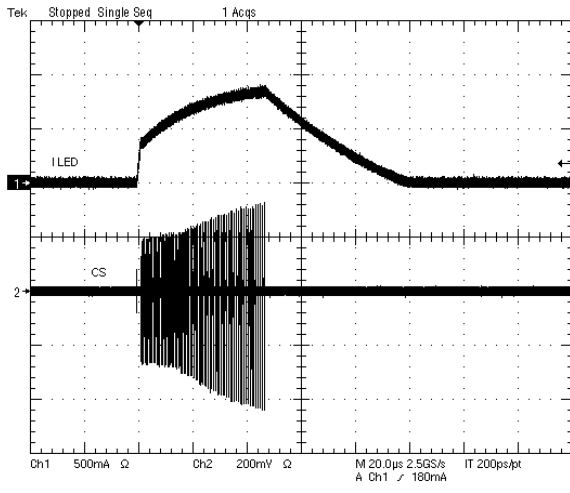


Figure 6. Short-Circuit Protection

When V_{IN} rises above the UVLO threshold voltage, switching operation of the FET will begin. However, until the V_{IN} voltage reaches 8 V, the VCC regulator may not provide the expected gate drive voltage to the FET. This could result in the $R_{DS(on)}$ of the FET being higher than expected or there not being enough gate drive capability to operate at the maximum rated switching frequency. For optimal performance, it is recommended to operate the part at a V_{IN} voltage of 8 V or greater.

Setting The Output Current

The average output current is determined as being the middle of the peak and valley of the output current, set by the CS comparator thresholds. The nominal average output current will be the current value equivalent to 200 mV at the CS pin. The proper R_{SENSE} value for a desired average output current can be calculated by:

$$R_{SENSE} = \frac{200 \text{ mV}}{I_{LED}}$$

PWM Dimming

For a given R_{SENSE} value, the average output current, and therefore the brightness of the LED, can be set to a lower value through the DIM/EN pin. When the DIM/EN pin is brought low, the internal FET will turn off and switching will remain off until the DIM/EN pin is brought back into its high state.

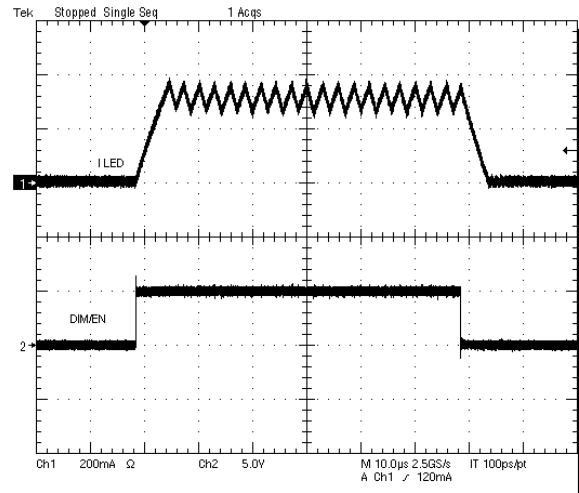


Figure 7. Dimming Waveforms

By applying a pulsed signal to DIM/EN, the average output current can be adjusted to the duty ratio of the pulsed signal. It is recommended to keep the frequency of the DIM/EN signal above 100 Hz to avoid any visible flickering of the LED.

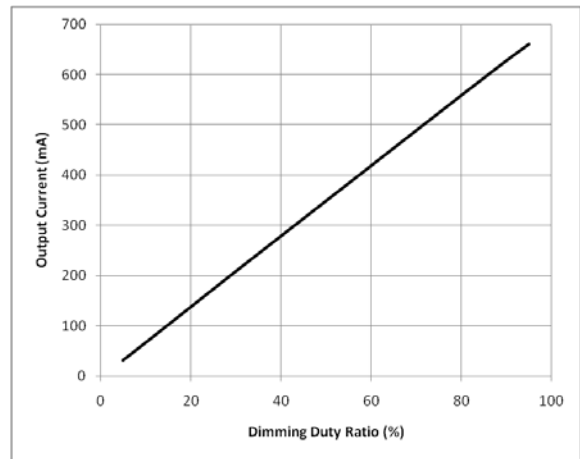


Figure 8. Dimming Performance

Inductor Selection

The inductor that is used directly affects the switching frequency the driver operates at. The value of the inductor sets the slope at which the output current rises and falls during the switching operation. The slope of the current, in turn, determines how long it takes the current to go from the valley point of the current ripple to the peak when the FET is on and the current is rising, and how long it takes the current to go from the peak point of the current to the valley when the FET is off and the current is falling. These times can be approximated from the following equations:

$$t_{ON} = \frac{L \times \Delta I}{V_{IN} - V_{LED} - I_{OUT} \times (R_{DS(on)} + DCR_L + R_{SENSE})}$$

$$t_{OFF} = \frac{L \times \Delta I}{V_{LED} + V_{diode} + I_{OUT} \times DCR_L}$$

Where DCR_L is the dc resistance of the inductor, V_{LED} is the forward voltages of the LEDs, $FET_{RDS(ON)}$ is the on-resistance of the power MOSFET, and V_{diode} is the forward voltage of the catch diode.

The switching frequency can then be approximated from the following:

$$f_{SW} = \frac{1}{t_{ON} + t_{OFF}}$$

Higher values of inductance lead to slower rates of rise and fall of the output current. This allows for smaller discrepancies between the expected and actual output current ripple due to propagation delays between sensing at the CS pin and the turning on and off of the power MOSFET. However, the inductor value should be chosen such that the peak output current value does not exceed the rated saturation current of the inductor.

Catch Diode Selection

The catch diode needs to be selected such that average current through the diode does not exceed the rated average forward current of the diode. The average current through the diode can be calculated as:

$$I_{avg_diode} = I_{OUT} \times \frac{t_{OFF}}{t_{ON} + t_{OFF}}$$

It is also important to select a diode that is capable of withstanding the peak reverse voltage it will see in the application. It is recommended to select a diode with a rated reverse voltage greater than V_{IN} . It is also recommended to use a low-capacitance Schottky diode for better efficiency performance.

Selecting The Off-Time Setting Resistor

The off-time setting resistor (R_{OT}) programs the NCL30160 with the initial time duration that the MOSFET is turned off when the switching operation begins. During subsequent switching cycles, the voltage at the CS pin is sensed every time the MOSFET is turned on, and the off-time will be adjusted depending on how much of a discrepancy exists between the sensed value and the CS lower limit threshold value. The R_{OT} value can be calculated using the following equation:

$$R_{OT} = t_{OFF} \times 10^{11} \Omega$$

Where t_{OFF} is the expected off time during normal switching operation, calculated in the Inductor Selection section above.

Input Capacitor

A decoupling capacitor from V_{IN} to ground should be used to provide the current needed when the power MOSFET turns on. A 4.7 μF ceramic capacitor is recommended.

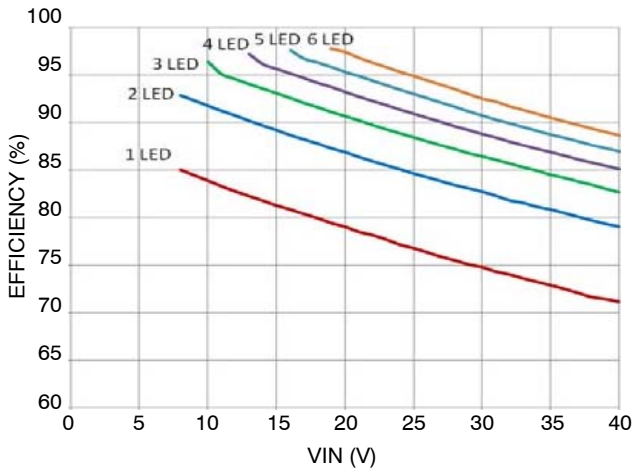


Figure 9. Efficiency, 350 mA, $V_{f_LED} = 3.5$ V

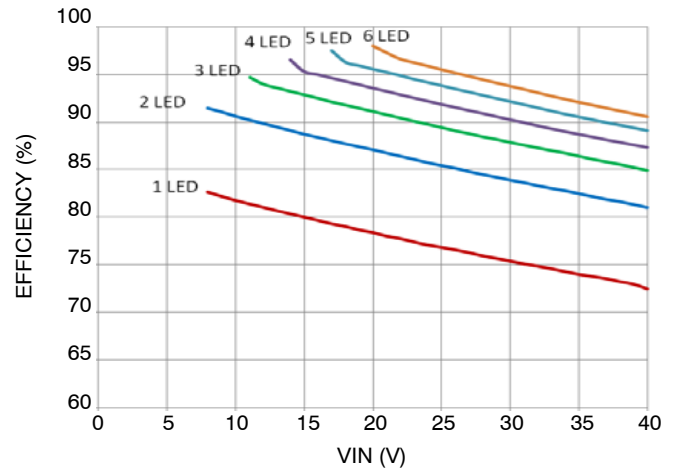


Figure 10. Efficiency, 700 mA, $V_{f_LED} = 3.5$ V

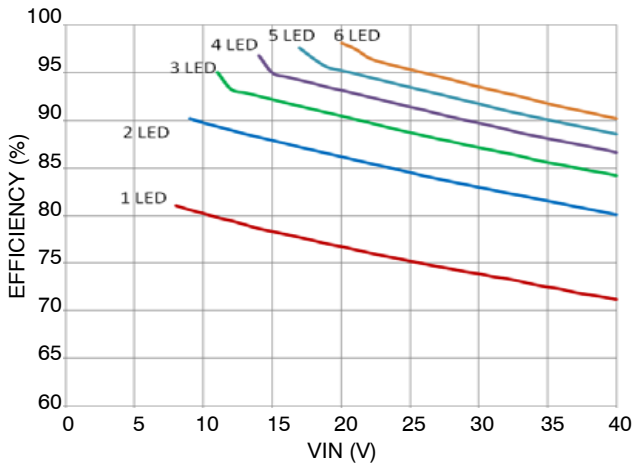


Figure 11. Efficiency, 1 A, $V_{f_LED} = 3.5$ V

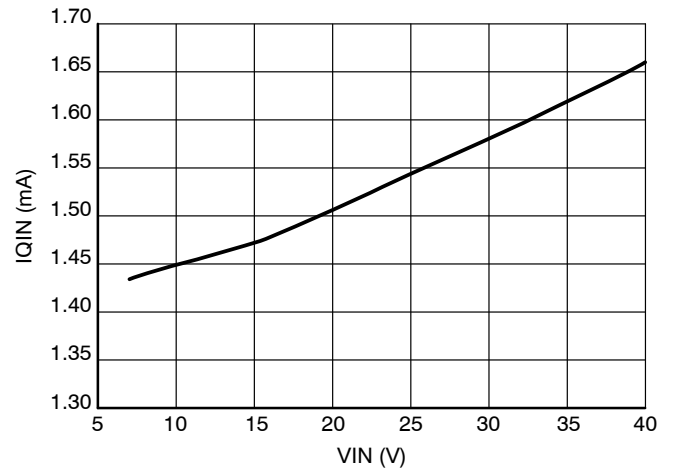


Figure 12. I_{QIN} vs. V_{IN}

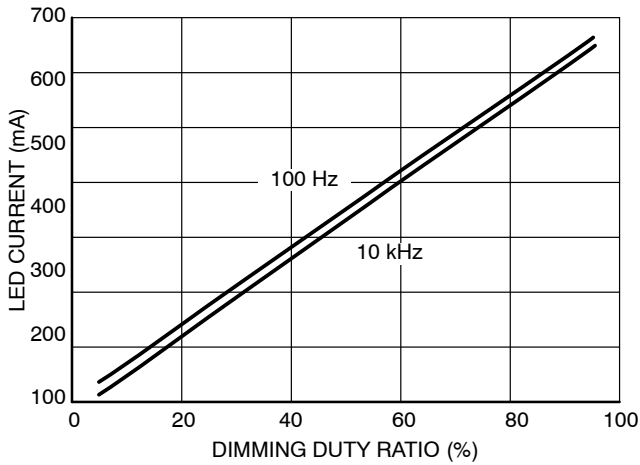


Figure 13. LED Current vs. Dimming Duty Ratio

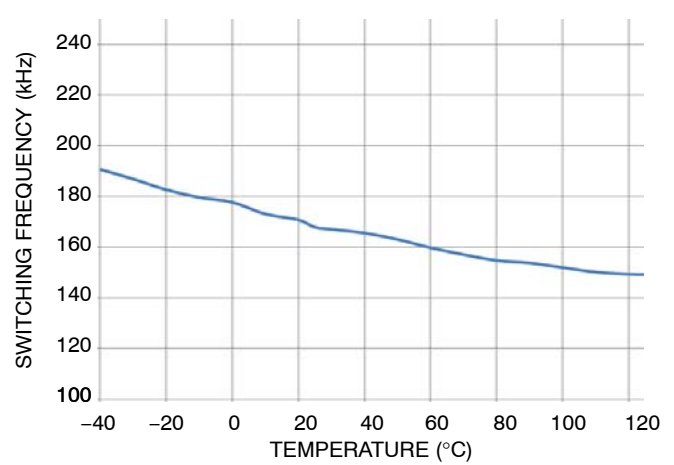


Figure 14. Switching Frequency vs. Temperature (12 V V_{IN} , 3 LEDs, 0.7 A, 0.47 μ H)

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

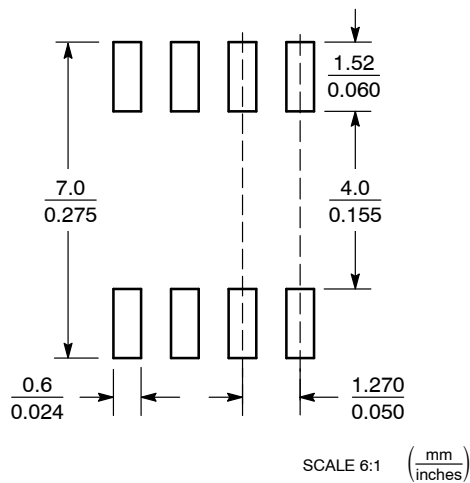
DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
 A = Assembly Location
 L = Wafer Lot
 Y = Year
 W = Work Week
 ■ = Pb-Free Package

XXXXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

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SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

- | | | | |
|---|--|--|--|
| <p>STYLE 1:
 PIN 1. EMITTER
 2. COLLECTOR
 3. COLLECTOR
 4. EMITTER
 5. EMITTER
 6. BASE
 7. BASE
 8. EMITTER</p> | <p>STYLE 2:
 PIN 1. COLLECTOR, DIE, #1
 2. COLLECTOR, #1
 3. COLLECTOR, #2
 4. COLLECTOR, #2
 5. BASE, #2
 6. EMITTER, #2
 7. BASE, #1
 8. EMITTER, #1</p> | <p>STYLE 3:
 PIN 1. DRAIN, DIE #1
 2. DRAIN, #1
 3. DRAIN, #2
 4. DRAIN, #2
 5. GATE, #2
 6. SOURCE, #2
 7. GATE, #1
 8. SOURCE, #1</p> | <p>STYLE 4:
 PIN 1. ANODE
 2. ANODE
 3. ANODE
 4. ANODE
 5. ANODE
 6. ANODE
 7. ANODE
 8. COMMON CATHODE</p> |
| <p>STYLE 5:
 PIN 1. DRAIN
 2. DRAIN
 3. DRAIN
 4. DRAIN
 5. GATE
 6. GATE
 7. SOURCE
 8. SOURCE</p> | <p>STYLE 6:
 PIN 1. SOURCE
 2. DRAIN
 3. DRAIN
 4. SOURCE
 5. SOURCE
 6. GATE
 7. GATE
 8. SOURCE</p> | <p>STYLE 7:
 PIN 1. INPUT
 2. EXTERNAL BYPASS
 3. THIRD STAGE SOURCE
 4. GROUND
 5. DRAIN
 6. GATE 3
 7. SECOND STAGE Vd
 8. FIRST STAGE Vd</p> | <p>STYLE 8:
 PIN 1. COLLECTOR, DIE #1
 2. BASE, #1
 3. BASE, #2
 4. COLLECTOR, #2
 5. COLLECTOR, #2
 6. EMITTER, #2
 7. EMITTER, #1
 8. COLLECTOR, #1</p> |
| <p>STYLE 9:
 PIN 1. EMITTER, COMMON
 2. COLLECTOR, DIE #1
 3. COLLECTOR, DIE #2
 4. EMITTER, COMMON
 5. EMITTER, COMMON
 6. BASE, DIE #2
 7. BASE, DIE #1
 8. EMITTER, COMMON</p> | <p>STYLE 10:
 PIN 1. GROUND
 2. BIAS 1
 3. OUTPUT
 4. GROUND
 5. GROUND
 6. BIAS 2
 7. INPUT
 8. GROUND</p> | <p>STYLE 11:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. DRAIN 2
 7. DRAIN 1
 8. DRAIN 1</p> | <p>STYLE 12:
 PIN 1. SOURCE
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 13:
 PIN 1. N.C.
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> | <p>STYLE 14:
 PIN 1. N-SOURCE
 2. N-GATE
 3. P-SOURCE
 4. P-GATE
 5. P-DRAIN
 6. P-DRAIN
 7. N-DRAIN
 8. N-DRAIN</p> | <p>STYLE 15:
 PIN 1. ANODE 1
 2. ANODE 1
 3. ANODE 1
 4. ANODE 1
 5. CATHODE, COMMON
 6. CATHODE, COMMON
 7. CATHODE, COMMON
 8. CATHODE, COMMON</p> | <p>STYLE 16:
 PIN 1. EMITTER, DIE #1
 2. BASE, DIE #1
 3. EMITTER, DIE #2
 4. BASE, DIE #2
 5. COLLECTOR, DIE #2
 6. COLLECTOR, DIE #2
 7. COLLECTOR, DIE #1
 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:
 PIN 1. VCC
 2. V2OUT
 3. V1OUT
 4. TXE
 5. RXE
 6. VEE
 7. GND
 8. ACC</p> | <p>STYLE 18:
 PIN 1. ANODE
 2. ANODE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. CATHODE
 8. CATHODE</p> | <p>STYLE 19:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. MIRROR 2
 7. DRAIN 1
 8. MIRROR 1</p> | <p>STYLE 20:
 PIN 1. SOURCE (N)
 2. GATE (N)
 3. SOURCE (P)
 4. GATE (P)
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 21:
 PIN 1. CATHODE 1
 2. CATHODE 2
 3. CATHODE 3
 4. CATHODE 4
 5. CATHODE 5
 6. COMMON ANODE
 7. COMMON ANODE
 8. CATHODE 6</p> | <p>STYLE 22:
 PIN 1. I/O LINE 1
 2. COMMON CATHODE/VCC
 3. COMMON CATHODE/VCC
 4. I/O LINE 3
 5. COMMON ANODE/GND
 6. I/O LINE 4
 7. I/O LINE 5
 8. COMMON ANODE/GND</p> | <p>STYLE 23:
 PIN 1. LINE 1 IN
 2. COMMON ANODE/GND
 3. COMMON ANODE/GND
 4. LINE 2 IN
 5. LINE 2 OUT
 6. COMMON ANODE/GND
 7. COMMON ANODE/GND
 8. LINE 1 OUT</p> | <p>STYLE 24:
 PIN 1. BASE
 2. EMITTER
 3. COLLECTOR/ANODE
 4. COLLECTOR/ANODE
 5. CATHODE
 6. CATHODE
 7. COLLECTOR/ANODE
 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25:
 PIN 1. VIN
 2. N/C
 3. REXT
 4. GND
 5. IOUT
 6. IOUT
 7. IOUT
 8. IOUT</p> | <p>STYLE 26:
 PIN 1. GND
 2. dv/dt
 3. ENABLE
 4. ILIMIT
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. VCC</p> | <p>STYLE 27:
 PIN 1. ILIMIT
 2. OVLO
 3. UVLO
 4. INPUT+
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. DRAIN</p> | <p>STYLE 28:
 PIN 1. SW_TO_GND
 2. DASIC_OFF
 3. DASIC_SW_DET
 4. GND
 5. V_MON
 6. VBULK
 7. VBULK
 8. VIN</p> |
| <p>STYLE 29:
 PIN 1. BASE, DIE #1
 2. EMITTER, #1
 3. BASE, #2
 4. EMITTER, #2
 5. COLLECTOR, #2
 6. COLLECTOR, #2
 7. COLLECTOR, #1
 8. COLLECTOR, #1</p> | <p>STYLE 30:
 PIN 1. DRAIN 1
 2. DRAIN 1
 3. GATE 2
 4. SOURCE 2
 5. SOURCE 1/DRAIN 2
 6. SOURCE 1/DRAIN 2
 7. SOURCE 1/DRAIN 2
 8. GATE 1</p> | | |

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