

# TinyLogic HS 2-Input NOR Gate

## NC7S02

### Description

The NC7S02 is a single 2-Input high performance CMOS NOR Gate. Advanced Silicon Gate CMOS fabrication assures high speed and low power circuit operation over a broad  $V_{CC}$  range. ESD protection diodes inherently guard both inputs and output with respect to the  $V_{CC}$  and GND rails. Three stages of gain between inputs and outputs assures high noise immunity and reduced sensitivity to input edge rate.

### Features

- Space Saving SOT23-5 and SC88A 5-Lead Packages
- Ultra Small MicroPak™ Leadless Package
- High Speed:  $t_{PD} = 3.5 \text{ ns Typ}$
- Low Quiescent Power:  $I_{CC} < 1 \mu\text{A}$
- Balanced Output Drive:  $2 \text{ mA } I_{OL}, -2 \text{ mA } I_{OH}$
- Broad  $V_{CC}$  Operating Range:  $2 \text{ V} - 6 \text{ V}$
- Balanced Propagation Delays
- Specified for 3 V Operation
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

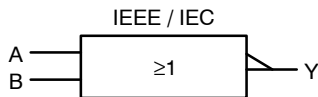
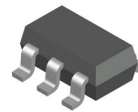
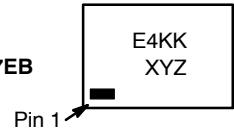


Figure 1. Logic Symbol

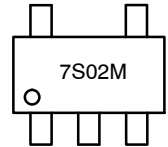
### MARKING DIAGRAMS



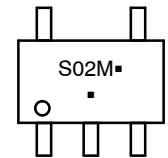
SIP6  
CASE 127EB



SOT23-5  
CASE 527AH



SC-88A  
CASE 419A-02



E4, 7S02, S02 = Specific Device Code  
KK = 2-Digit Lot Run Traceability Code  
XY = 2-Digit Date Code Format  
Z = Assembly Plant Code  
M = Date Code\*

\*Date Code orientation and/or position may vary depending upon manufacturing location.

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

# NC7S02

## Pin Configurations

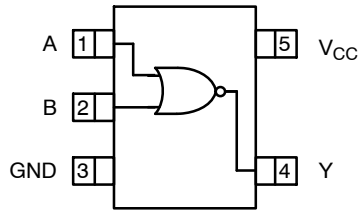


Figure 2. SC-88A and SOT23-5 (Top View)



Figure 3. MicroPak (Top Through View)

## PIN DESCRIPTIONS

Pin Name	Description
A, B	Inputs
Y	Output
NC	No Connect

## FUNCTION TABLE ( $Y = \overline{A + B}$ )

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH Logic Level  
L = LOW Logic Level

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
$V_{CC}$	Supply Voltage		-0.5	6.5	V
$I_{IK}$	DC Input Diode Current	$V_{IN} < 0\text{ V}$	-	-20	mA
		$V_{IN} > V_{CC}$	-	+20	
$V_{IN}$	DC Input Voltage		-0.5	$V_{CC} + 0.5$	V
$I_{OK}$	DC Output Diode Current	$V_{OUT} < 0\text{ V}$	-	-20	mA
		$V_{OUT} > V_{CC}$	-	+20	
$V_{OUT}$	DC Output Voltage		-0.5	$V_{CC} + 0.5$	V
$I_{OUT}$	DC Output Source or Sink Current		-	$\pm 12.5$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current per Output Pin		-	$\pm 25$	mA
$T_{STG}$	Storage Temperature		-65	+150	$^{\circ}\text{C}$
$T_J$	Junction Temperature		-	+150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (Soldering, 10 Seconds)		-	+260	$^{\circ}\text{C}$
$P_D$	Power Dissipation in Still Air	SOT23-5	-	390	mW
		SC-88A	-	332	
		MicroPak-6	-	812	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

# NC7S02

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	Supply Voltage		2.0	6.0	V
V <sub>IN</sub>	Input Voltage		0	V <sub>CC</sub>	V
V <sub>OUT</sub>	Output Voltage		0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature		-40	+85	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Times	V <sub>CC</sub> at 2.0 V	0	20	ns/V
		V <sub>CC</sub> at 3.0 V	0	20	
		V <sub>CC</sub> at 4.5 V	0	10	
		V <sub>CC</sub> at 6.0 V	0	5	
θ <sub>JA</sub>	Thermal Resistance	SOT23-5	-	320	°C/W
		SC-88A	-	377	
		MicroPak-6	-	154	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Unused inputs must be held HIGH or LOW. They may not float.

## DC ELECTRICAL CHARACTERISTICS

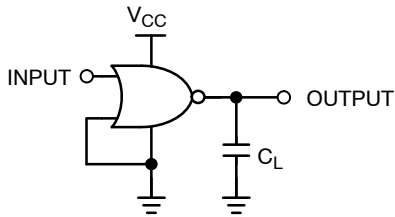
Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40 to +85°C		Unit
				Min	Typ	Max	Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage	2.0 3.0 - 6.0		1.50 0.7 V <sub>CC</sub>	- -	- -	1.50 0.7 V <sub>CC</sub>	- -	V
V <sub>IL</sub>	LOW Level Input Voltage	2.0 3.0 - 6.0		- -	- -	0.50 0.3 V <sub>CC</sub>	- -	0.50 0.3 V <sub>CC</sub>	V
V <sub>OH</sub>	HIGH Level Output Voltage	2.0 3.0 4.5 6.0	I <sub>OH</sub> = -20 μA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	1.90 2.90 4.40 5.90	2.0 3.0 4.5 6.0	- - - -	1.90 2.90 4.40 5.90	- - - -	V
		3.0 4.5 6.0	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -1.3 mA I <sub>OH</sub> = -2.0 mA I <sub>OH</sub> = -2.6 mA	2.68 4.18 5.68	2.85 4.35 5.85	- - -	2.63 4.13 5.63	- - -	V
V <sub>OL</sub>	LOW Level Output Voltage	2.0 3.0 4.5 6.0	I <sub>OL</sub> = 20 μA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	- - - -	0.0 0.0 0.0 0.0	0.10 0.10 0.10 0.10	- - - -	0.10 0.10 0.10 0.10	V
		3.0 4.5 6.0	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 1.3 mA I <sub>OL</sub> = 2.0 mA I <sub>OL</sub> = 2.6 mA	- - -	0.1 0.1 0.1	0.26 0.26 0.26	- - -	0.33 0.33 0.33	V
I <sub>IN</sub>	Input Leakage Current	6.0	V <sub>IN</sub> = V <sub>CC</sub> , GND	-	-	±0.1	-	±1.0	μA
I <sub>CC</sub>	Quiescent Supply Current	6.0	V <sub>IN</sub> = V <sub>CC</sub> , GND	-	-	1.0	-	10.0	μA

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40 to +85°C		Unit
				Min	Typ	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay (Figure 4, 6)	5.0	C <sub>L</sub> = 15 pF	-	3.5	15	-	-	ns
		2.0	C <sub>L</sub> = 50 pF	-	19	100	-	125	ns
		3.0		-	10.5	27	-	35	
		4.5		-	7.5	20	-	25	
6.0	-	6.5	17	-	21				
t <sub>TLH</sub> , t <sub>THL</sub>	Output Transition Time (Figure 4, 6)	5.0	C <sub>L</sub> = 15 pF	-	3	10	-	-	ns
		2.0	C <sub>L</sub> = 50 pF	-	25	125	-	155	ns
		3.0		-	16	35	-	45	
		4.5		-	11	25	-	31	
6.0	-	9	21	-	26				
C <sub>IN</sub>	Input Capacitance	Open		-	2	10	-	10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Figure 5)	5.0	(Note 2)	-	6	-	-	-	pF

2. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I<sub>CCD</sub>) at no output loading and operating at 50% duty cycle. C<sub>PD</sub> is related to I<sub>CCD</sub> dynamic operating current by the expression:  
 $I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CCstatic})$ .

AC Loading and Waveforms



C<sub>L</sub> includes load and stray capacitance  
 Input PRR = 1.0 MHz; t<sub>w</sub> = 500 ns

Figure 4. AC Test Circuit

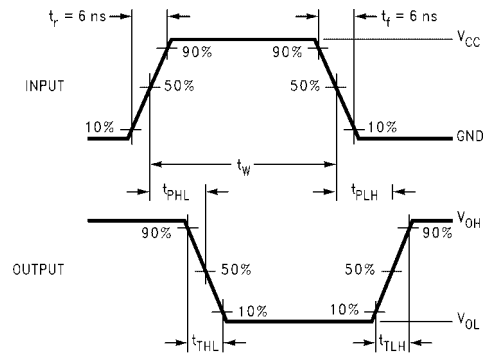
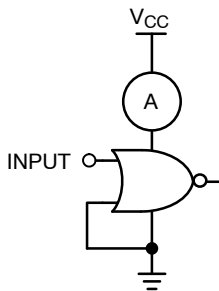


Figure 6. AC Waveforms



Input = AC Waveform;  
 PRR = Variable; Duty Cycle = 50%.

Figure 5. I<sub>CCD</sub> Test Circuit

## NC7S02

### ORDERING INFORMATION

Order Number	Top Mark	Package Description	Shipping <sup>†</sup>
NC7S02M5X	7S02	SOT23-5	3000 / Tape & Reel
NC7S02M5X-L22090	7S02	SOT23-5	3000 / Tape & Reel
NC7S02P5X	S02	SC-88A	3000 / Tape & Reel
NC7S02P5X-L22057	S02	SC-88A	3000 / Tape & Reel
NC7S02L6X	E4	SIP6, MicroPak	5000 / Tape & Reel
NC7S02L6X-L22175	E4	SIP6, MicroPak	5000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



SIP6 1.45X1.0  
CASE 127EB  
ISSUE O

DATE 31 AUG 2016



NOTES:

1. CONFORMS TO JEDEC STANDARD MO-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-2009
4. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

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<b>DESCRIPTION:</b>	<b>SIP6 1.45X1.0</b>	<b>PAGE 1 OF 1</b>

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

## SC-88A (SC-70-5/SOT-353) CASE 419A-02 ISSUE M

DATE 11 APR 2023



### RECOMMENDED MOUNTING FOOTPRINT

\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.95	1.10
A1	---	---	0.10
A3	0.20 REF		
b	0.10	0.20	0.30
c	0.10	---	0.25
D	1.80	2.00	2.20
E	2.00	2.10	2.20
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.10	0.15	0.30

### GENERIC MARKING DIAGRAM\*



\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code

M = Date Code

▪ = Pb-Free Package

(Note: Microdot may be in either location)

#### STYLE 1:

- PIN 1. BASE
- EMITTER
- BASE
- COLLECTOR
- COLLECTOR

#### STYLE 2:

- PIN 1. ANODE
- EMITTER
- BASE
- COLLECTOR
- CATHODE

#### STYLE 3:

- PIN 1. ANODE 1
- N/C
- ANODE 2
- CATHODE 2
- CATHODE 1

#### STYLE 4:

- PIN 1. SOURCE 1
- DRAIN 1/2
- SOURCE 1
- GATE 1
- GATE 2

#### STYLE 5:

- PIN 1. CATHODE
- COMMON ANODE
- CATHODE 2
- CATHODE 3
- CATHODE 4

#### STYLE 6:

- PIN 1. EMITTER 2
- BASE 2
- EMITTER 1
- COLLECTOR
- COLLECTOR 2/BASE 1

#### STYLE 7:

- PIN 1. BASE
- EMITTER
- BASE
- COLLECTOR
- COLLECTOR

#### STYLE 8:

- PIN 1. CATHODE
- COLLECTOR
- N/C
- BASE
- EMITTER

#### STYLE 9:

- PIN 1. ANODE
- CATHODE
- ANODE
- ANODE
- ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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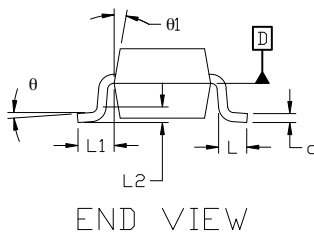
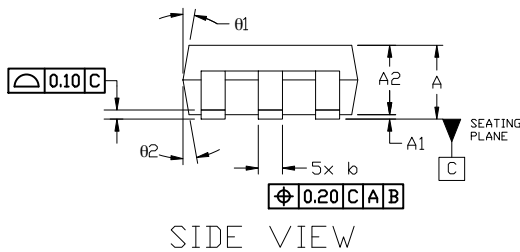
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®

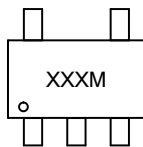


## SOT-23, 5 Lead CASE 527AH ISSUE A

DATE 09 JUN 2021



### GENERIC MARKING DIAGRAM\*



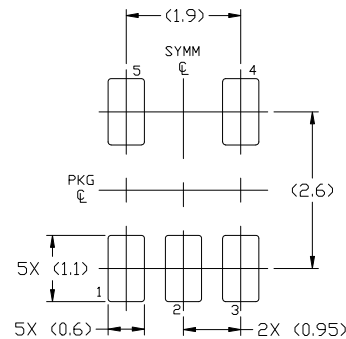
XXX = Specific Device Code  
M = Date Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1989A
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM D.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL NOT BE LESS THAN 0.07mm.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	—	1.45
A1	0.00	—	0.15
A2	0.90	1.15	1.30
b	0.30	—	0.50
c	0.08	—	0.22
D	2.90 BSC		
E	2.80 BSC		
E1	1.60 BSC		
e	0.95 BSC		
L	0.30	0.45	0.60
L1	0.60 REF		
L2	0.25 REF		
theta	0°	4°	8°
theta1	0°	10°	15°
theta2	0°	10°	15°



For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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