

PNP Silicon General Purpose High Voltage Transistor

MSB92T1G

This PNP Silicon Planar Transistor is designed for general purpose amplifier applications. This device is housed in the SC-59 package which is designed for low power surface mount applications.

Features

- This is a Pb-Free Device

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

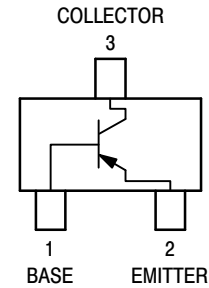
Rating	Symbol	Value	Unit
Collector-Base Voltage	$V_{(BR)CBO}$	-300	Vdc
Collector-Emitter Voltage	$V_{(BR)CEO}$	-300	Vdc
Emitter-Base Voltage	$V_{(BR)EBO}$	-5.0	Vdc
Collector Current – Continuous	I_C	150	mAdc

THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit
Power Dissipation (Note 1)	P_D	150	mW
Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 ~ +150	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

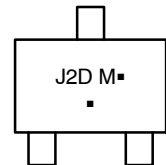
- Device mounted on a FR-4 glass epoxy printed circuit board using the minimum recommended footprint.



MARKING DIAGRAM



SC-59
CASE 318D
STYLE 1



J2D = Device Marking Code

M = Date Code

▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping [†]
MSB92T1G	SC-59 (Pb-Free)	3000/Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MSB92T1G

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Collector-Emitter Breakdown Voltage ($I_C = -1.0 \text{ mAdc}$, $I_B = 0$)	$V_{(BR)CEO}$	-300	–	Vdc
Collector-Base Breakdown Voltage ($I_C = -100 \text{ } \mu\text{Adc}$, $I_E = 0$)	$V_{(BR)CBO}$	-300	–	Vdc
Emitter-Base Breakdown Voltage ($I_E = -100 \text{ } \mu\text{Adc}$, $I_E = 0$)	$V_{(BR)EBO}$	-5.0	–	Vdc
Collector-Base Cutoff Current ($V_{CB} = -200 \text{ Vdc}$, $I_E = 0$)	I_{CBO}	–	-0.25	μA
Emitter-Base Cutoff Current ($V_{EB} = -3.0 \text{ Vdc}$, $I_B = 0$)	I_{EBO}	–	-0.1	μA
DC Current Gain (Note 2) ($V_{CE} = -10 \text{ Vdc}$, $I_C = -1.0 \text{ mAdc}$) ($V_{CE} = -10 \text{ Vdc}$, $I_C = -10 \text{ mAdc}$) ($V_{CE} = -10 \text{ Vdc}$, $I_C = -30 \text{ mAdc}$)	h_{FE1} h_{FE2} h_{FE3}	25 40 25	– – –	–
Collector-Emitter Saturation Voltage ($I_C = -20 \text{ mAdc}$, $I_B = -2.0 \text{ mAdc}$)	$V_{CE(sat)}$	–	-0.5	Vdc
Base-Emitter Saturation Voltage ($I_C = -20 \text{ mAdc}$, $I_B = -2.0 \text{ mAdc}$)	$V_{BE(sat)}$	–	-0.9	Vdc

SMALL SIGNAL CHARACTERISTICS

Current-Gain – Bandwidth Product ($I_C = -10 \text{ mAdc}$, $V_{CE} = -20 \text{ Vdc}$, $f = 20 \text{ MHz}$)	f_T	50	–	MHz
Collector-Base Capacitance ($V_{CB} = -20 \text{ Vdc}$, $I_E = 0$, $f = 1.0 \text{ MHz}$)	C_{cb}	–	6.0	pF

2. Pulse Test: Pulse Width $\leq 300 \text{ } \mu\text{s}$, Duty Cycle $\leq 2\%$.

MSB92T1G

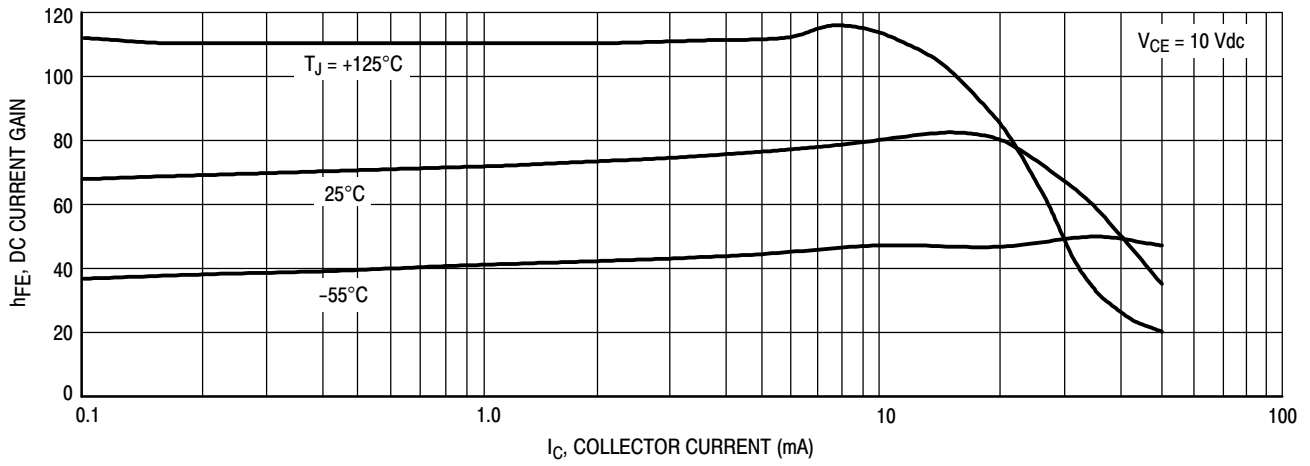


Figure 1. DC Current Gain

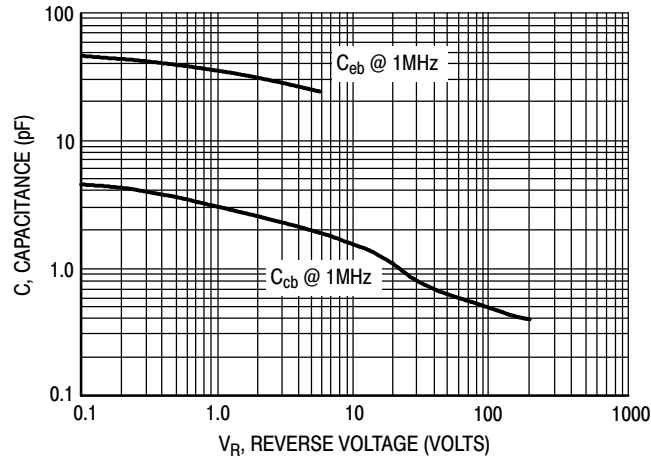


Figure 2. Capacitance

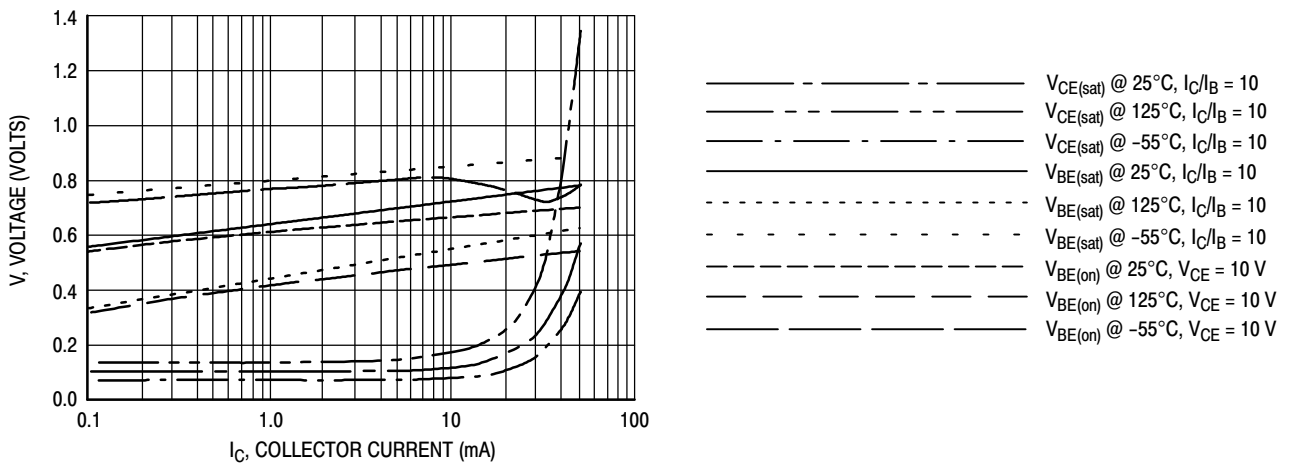


Figure 3. "ON" Voltages



SCALE 4:1

SOT-23 (TO-236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

DATE 14 AUG 2024



MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.89	1.00	1.11
A1	0.01	0.06	0.10
b	0.37	0.44	0.50
c	0.08	0.14	0.20
D	2.80	2.90	3.04
E	1.20	1.30	1.40
e	1.78	1.90	2.04
L	0.30	0.43	0.55
L1	0.35	0.54	0.69
HE	2.10	2.40	2.64
T	0°	---	10°

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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STYLE 1 THRU 5: CANCELLED	STYLE 6: PIN 1. BASE 2. EMITTER 3. COLLECTOR	STYLE 7: PIN 1. EMITTER 2. BASE 3. COLLECTOR	STYLE 8: PIN 1. ANODE 2. NO CONNECTION 3. CATHODE		
STYLE 9: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 10: PIN 1. DRAIN 2. SOURCE 3. GATE	STYLE 11: PIN 1. ANODE 2. CATHODE 3. CATHODE-ANODE	STYLE 12: PIN 1. CATHODE 2. CATHODE 3. ANODE	STYLE 13: PIN 1. SOURCE 2. DRAIN 3. GATE	STYLE 14: PIN 1. CATHODE 2. GATE 3. ANODE
STYLE 15: PIN 1. GATE 2. CATHODE 3. ANODE	STYLE 16: PIN 1. ANODE 2. CATHODE 3. CATHODE	STYLE 17: PIN 1. NO CONNECTION 2. ANODE 3. CATHODE	STYLE 18: PIN 1. NO CONNECTION 2. CATHODE 3. ANODE	STYLE 19: PIN 1. CATHODE 2. ANODE 3. CATHODE-ANODE	STYLE 20: PIN 1. CATHODE 2. ANODE 3. GATE
STYLE 21: PIN 1. GATE 2. SOURCE 3. DRAIN	STYLE 22: PIN 1. RETURN 2. OUTPUT 3. INPUT	STYLE 23: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 24: PIN 1. GATE 2. DRAIN 3. SOURCE	STYLE 25: PIN 1. ANODE 2. CATHODE 3. GATE	STYLE 26: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION
STYLE 27: PIN 1. CATHODE 2. CATHODE 3. CATHODE	STYLE 28: PIN 1. ANODE 2. ANODE 3. ANODE				

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