

ON Semiconductor

Is Now

onsemi™

To learn more about onsemi™, please visit our website at
www.onsemi.com

onsemi and **onsemi** and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi** product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner. Other names and brands may be claimed as the property of others.

MPF102

Preferred Devices

JFET VHF Amplifier

N-Channel – Depletion

Features

- Pb-Free Package is Available*

MAXIMUM RATINGS

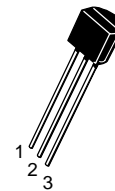
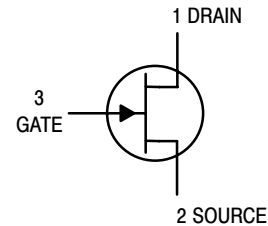
| Rating | Symbol | Value | Unit |
|---|-----------|-------------|----------------------------|
| Drain-Source Voltage | V_{DS} | 25 | Vdc |
| Drain-Gate Voltage | V_{DG} | 25 | Vdc |
| Gate-Source Voltage | V_{GS} | -25 | Vdc |
| Gate Current | I_G | 10 | mAdc |
| Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C | P_D | 350 2.8 | mW mW/ $^\circ\text{C}$ |
| Junction Temperature Range | T_J | 125 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^\circ\text{C}$ |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.



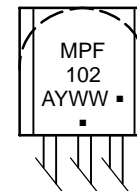
ON Semiconductor®

<http://onsemi.com>



TO-92 (TO-226AA)
CASE 29-11
STYLE 5

MARKING DIAGRAM



MPF102 = Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

| Device | Package | Shipping |
|---------|--------------------|-----------------|
| MPF102 | TO-92 | 1000 Units/Bulk |
| MPF102G | TO-92 (Pb-Free) | 1000 Units/Bulk |

Preferred devices are recommended choices for future use and best overall value.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MPF102

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Max | Unit |
|--|----------------------|--------------|--------------|--------------|
| OFF CHARACTERISTICS | | | | |
| Gate-Source Breakdown Voltage (I _G = -10 μAdc, V _{DS} = 0) | V _{(BR)GSS} | -25 | - | Vdc |
| Gate Reverse Current (V _{GS} = -15 Vdc, V _{DS} = 0) (V _{GS} = -15 Vdc, V _{DS} = 0, T _A = 100°C) | I _{GSS} | - | -2.0 -2.0 | nAdc μAdc |
| Gate-Source Cutoff Voltage (V _{DS} = 15 Vdc, I _D = 2.0 nAdc) | V _{GS(off)} | - | -8.0 | Vdc |
| Gate-Source Voltage (V _{DS} = 15 Vdc, I _D = 0.2 mAdc) | V _{GS} | -0.5 | -7.5 | Vdc |
| ON CHARACTERISTICS | | | | |
| Zero-Gate-Voltage Drain Current (Note 1) (V _{DS} = 15 Vdc, V _{GS} = 0 Vdc) | I _{DSS} | 2.0 | 20 | mAdc |
| SMALL-SIGNAL CHARACTERISTICS | | | | |
| Forward Transfer Admittance (Note 1) (V _{DS} = 15 Vdc, V _{GS} = 0, f = 1.0 kHz) (V _{DS} = 15 Vdc, V _{GS} = 0, f = 100 MHz) | y _{fs} | 2000 1600 | 7500 - | μmhos |
| Input Admittance (V _{DS} = 15 Vdc, V _{GS} = 0, f = 100 MHz) | Re(y _{is}) | - | 800 | μmhos |
| Output Conductance (V _{DS} = 15 Vdc, V _{GS} = 0, f = 100 MHz) | Re(y _{os}) | - | 200 | μmhos |
| Input Capacitance (V _{DS} = 15 Vdc, V _{GS} = 0, f = 1.0 MHz) | C _{iss} | - | 7.0 | pF |
| Reverse Transfer Capacitance (V _{DS} = 15 Vdc, V _{GS} = 0, f = 1.0 MHz) | C _{rss} | - | 3.0 | pF |

1. Pulse Test; Pulse Width ≤ 630 ms, Duty Cycle ≤ 10%.

MPF102

COMMON SOURCE CHARACTERISTICS

ADMITTANCE PARAMETERS

($V_{DS} = 15 \text{ Vdc}$, $T_{channel} = 25^\circ\text{C}$)

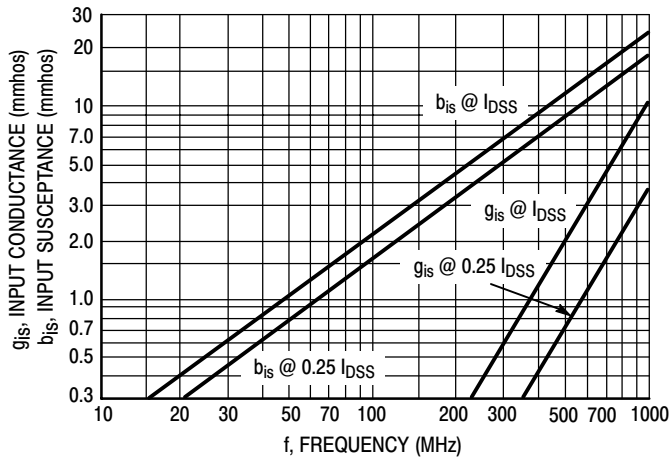


Figure 1. Input Admittance (y_{is})

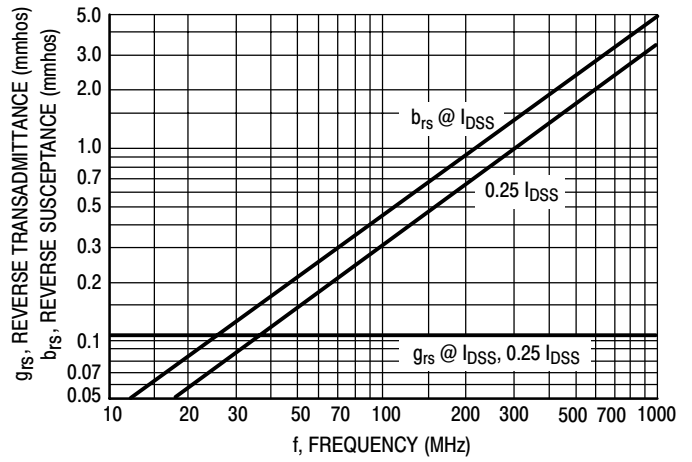


Figure 2. Reverse Transfer Admittance (y_{rs})

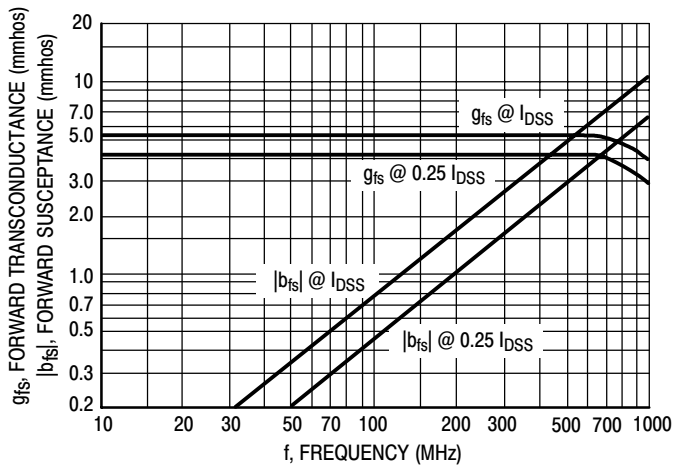


Figure 3. Forward Transfer Admittance (y_{fs})

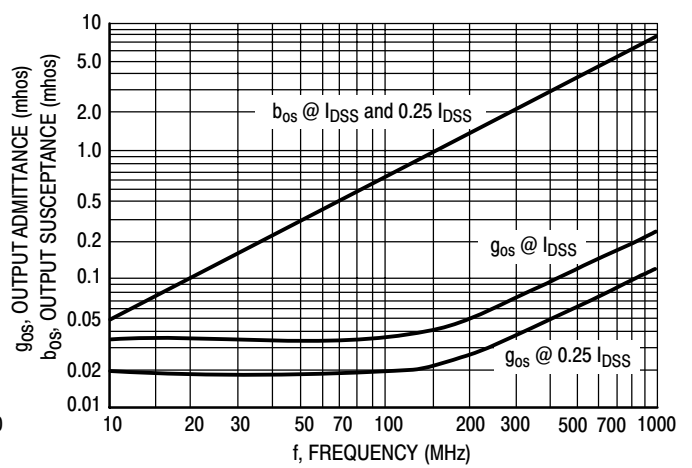


Figure 4. Output Admittance (y_{os})

COMMON SOURCE CHARACTERISTICS
S-PARAMETERS

($V_{DS} = 15 \text{ Vdc}$, $T_{channel} = 25^\circ\text{C}$, Data Points in MHz)

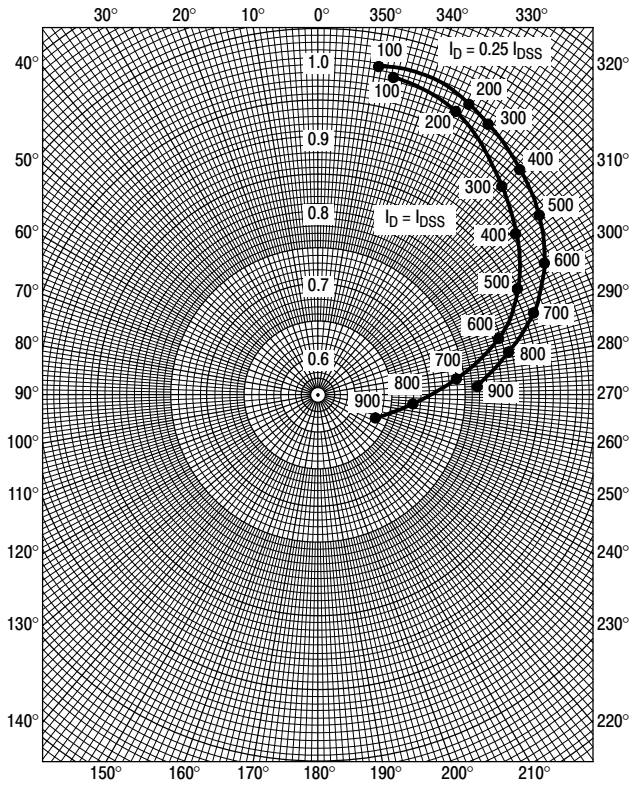


Figure 5. S_{11s}

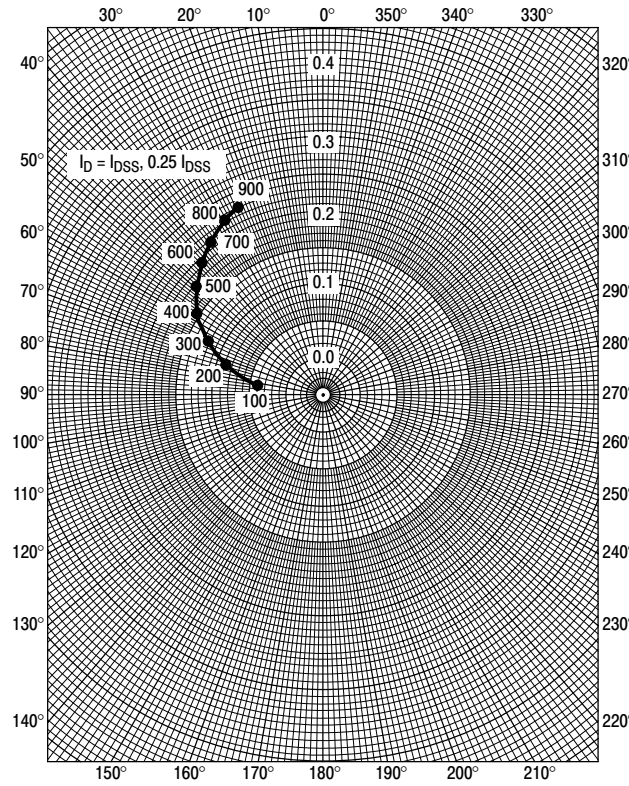


Figure 6. S_{12s}

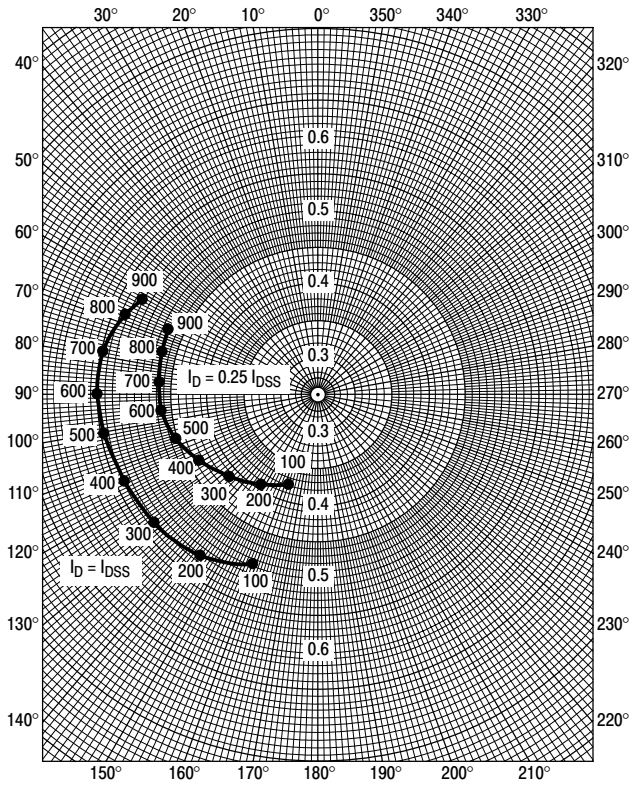


Figure 7. S_{21s}

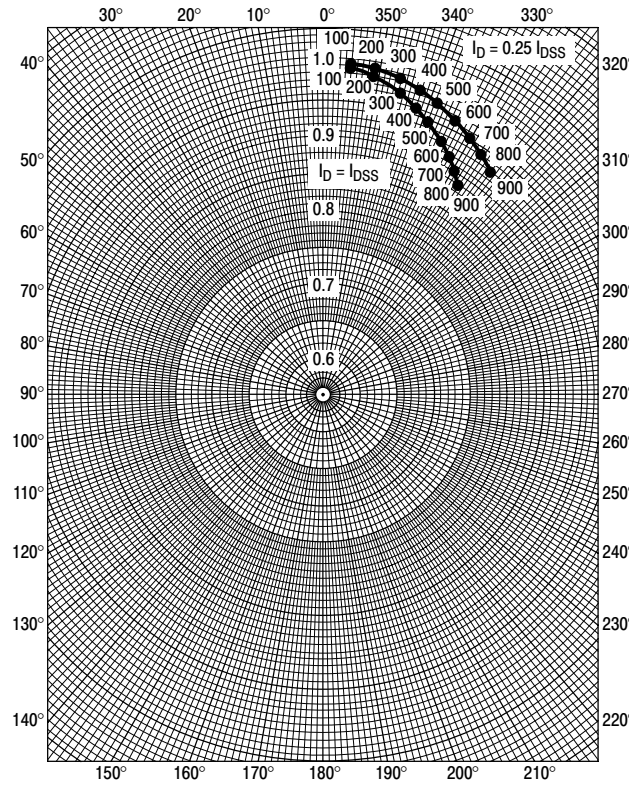


Figure 8. S_{22s}

MPF102

COMMON GATE CHARACTERISTICS

ADMITTANCE PARAMETERS

($V_{DG} = 15 \text{ Vdc}$, $T_{channel} = 25^\circ\text{C}$)

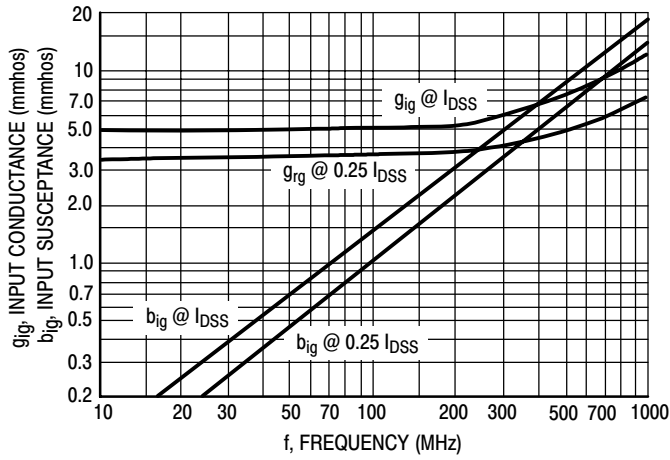


Figure 9. Input Admittance (y_{ig})

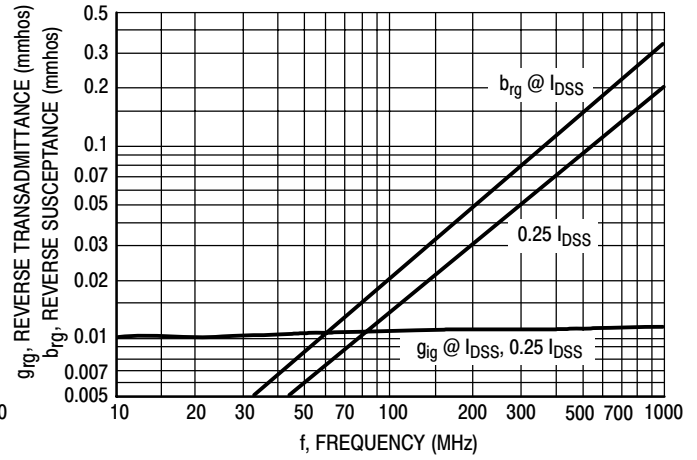


Figure 10. Reverse Transfer Admittance (y_{rg})

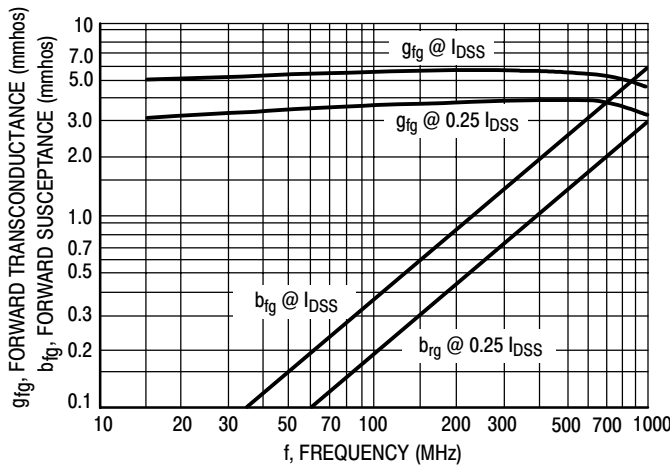


Figure 11. Forward Transfer Admittance (y_{fg})

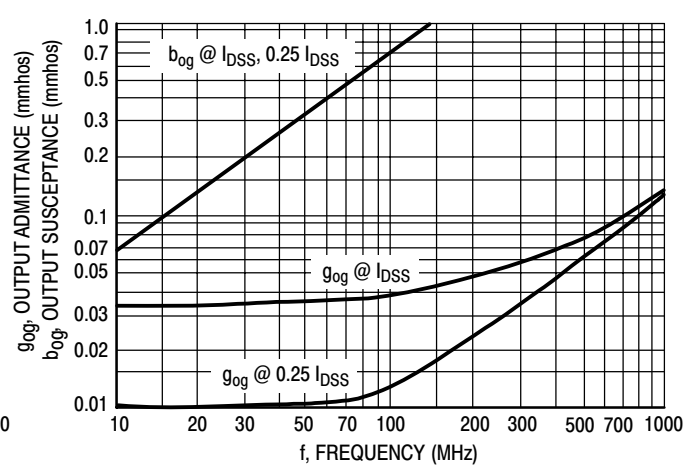


Figure 12. Output Admittance (y_{og})

COMMON GATE CHARACTERISTICS
S-PARAMETERS

($V_{DS} = 15 \text{ Vdc}$, $T_{\text{channel}} = 25^\circ\text{C}$, Data Points in MHz)

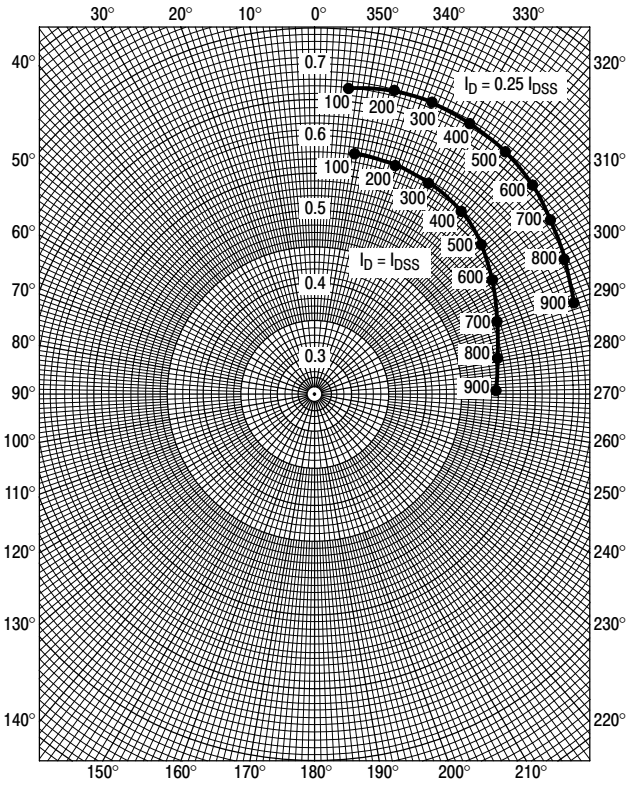


Figure 13. S_{11g}

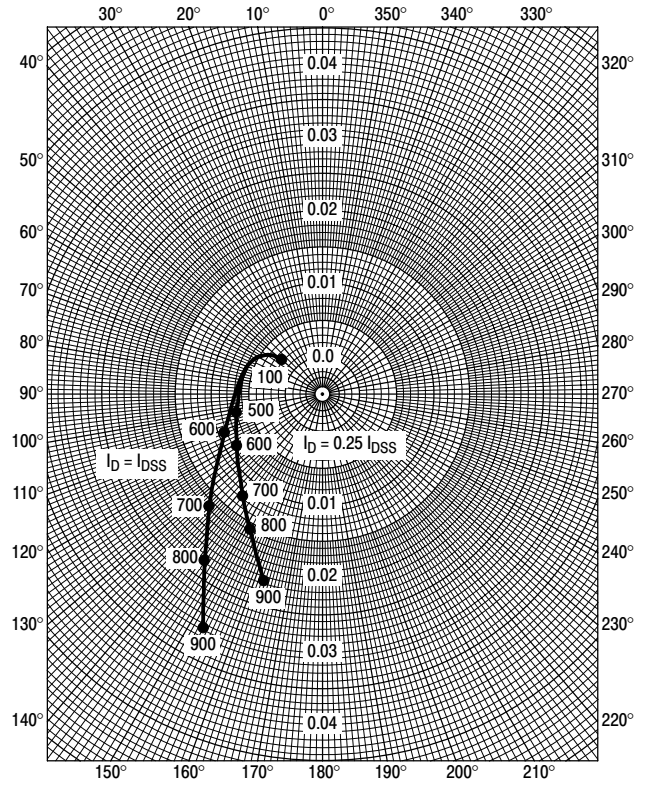


Figure 14. S_{12g}

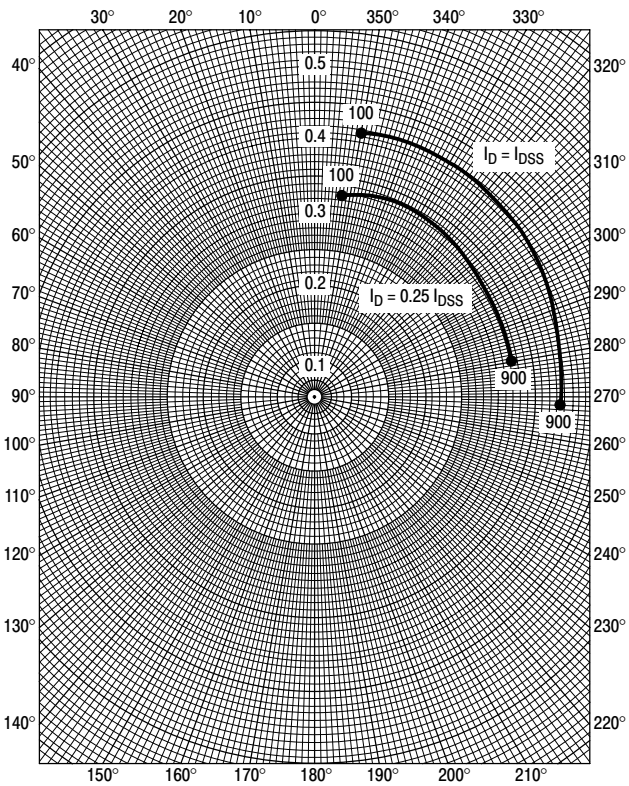


Figure 15. S_{21a}

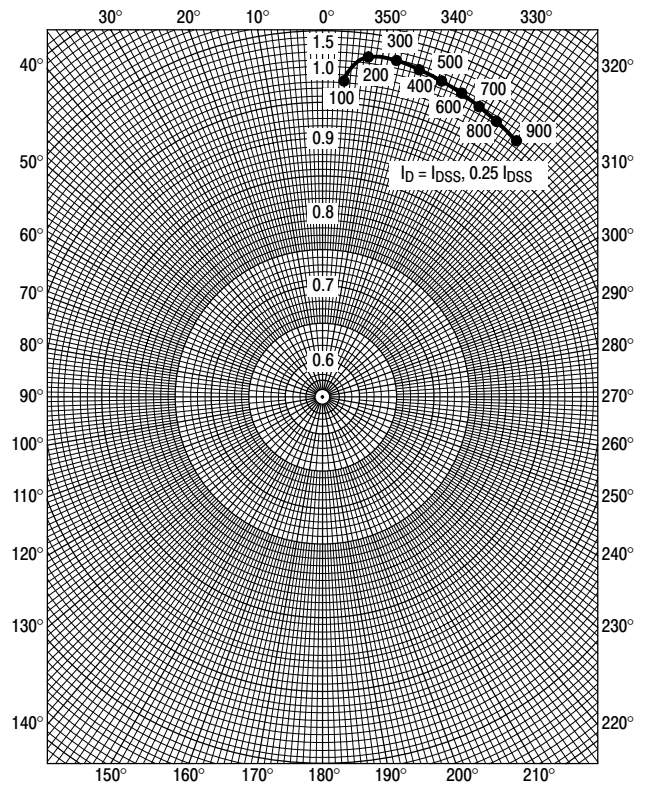
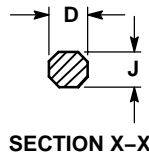
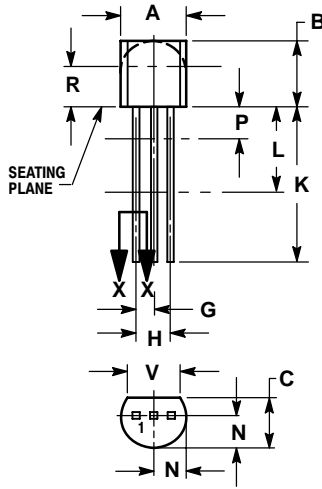


Figure 16. S_{22a}

MPF102

PACKAGE DIMENSIONS

TO-92 (TO-226)
CASE 29-11
ISSUE AL



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

| DIM | INCHES | | MILLIMETERS | |
|-----|--------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.175 | 0.205 | 4.45 | 5.20 |
| B | 0.170 | 0.210 | 4.32 | 5.33 |
| C | 0.125 | 0.165 | 3.18 | 4.19 |
| D | 0.016 | 0.021 | 0.407 | 0.533 |
| G | 0.045 | 0.055 | 1.15 | 1.39 |
| H | 0.095 | 0.105 | 2.42 | 2.66 |
| J | 0.015 | 0.020 | 0.39 | 0.50 |
| K | 0.500 | --- | 12.70 | --- |
| L | 0.250 | --- | 6.35 | --- |
| N | 0.080 | 0.105 | 2.04 | 2.66 |
| P | --- | 0.100 | --- | 2.54 |
| R | 0.115 | --- | 2.93 | --- |
| V | 0.135 | --- | 3.43 | --- |

STYLE 5:

1. DRAIN
2. SOURCE
3. GATE

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA
Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada
Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.