

# MMBF4416LT1

Preferred Device

## JFET VHF/UHF Amplifier Transistor

### N-Channel

#### Features

- Pb-Free Package is Available

#### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	30	Vdc
Drain-Gate Voltage	$V_{DG}$	30	Vdc
Gate-Source Voltage	$V_{GS}$	30	Vdc
Gate Current	$I_G$	10	mAdc

#### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR-5 Board, (Note 1) $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	225 1.8	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	556	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

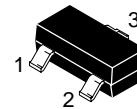
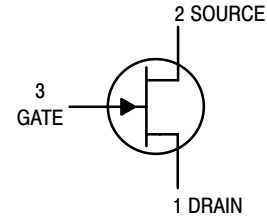
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. FR-5 = 1.0 x 0.75 x 0.062 in.



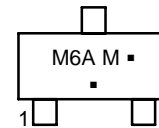
ON Semiconductor®

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SOT-23 (TO-236)  
CASE 318  
STYLE 10

#### MARKING DIAGRAM



M6A = Device Code  
M = Date Code\*  
■ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation and/or overbar may vary depending upon manufacturing location.

#### ORDERING INFORMATION

Device	Package	Shipping†
MMBF4416LT1	SOT-23	3,000 / Tape & Reel
MMBF4416LT1G	SOT-23 (Pb-Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

# MMBF4416LT1

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Gate-Source Breakdown Voltage ( $I_G = 1.0 \mu\text{Adc}$ , $V_{DS} = 0$ )	$V_{(BR)GSS}$	30	-	Vdc
Gate Reverse Current ( $V_{GS} = 20 \text{Vdc}$ , $V_{DS} = 0$ ) ( $V_{GS} = 20 \text{Vdc}$ , $V_{DS} = 0$ , $T_A = 150^\circ\text{C}$ )	$I_{GSS}$	-	1.0 200	nAdc
Gate Source Cutoff Voltage ( $I_D = 1.0 \text{nAdc}$ , $V_{DS} = 15 \text{Vdc}$ )	$V_{GS(off)}$	-	-6.0	Vdc
Gate Source Voltage ( $I_D = 0.5 \text{mAdc}$ , $V_{DS} = 15 \text{Vdc}$ )	$V_{GS}$	-1.0	-5.5	Vdc
<b>ON CHARACTERISTICS</b>				
Zero-Gate-Voltage Drain Current ( $V_{GS} = 15 \text{Vdc}$ , $V_{GS} = 0$ )	$I_{DSS}$	5.0	15	mAdc
Gate-Source Forward Voltage ( $I_G = 1.0 \text{mAdc}$ , $V_{DS} = 0$ )	$V_{GS(f)}$	-	1.0	Vdc
<b>SMALL-SIGNAL CHARACTERISTICS</b>				
Forward Transfer Admittance ( $V_{DS} = 15 \text{Vdc}$ , $V_{GS} = 0$ , $f = 1.0 \text{kHz}$ )	$ Y_{fs} $	4500	7500	$\mu\text{mhos}$
Output Admittance ( $V_{DS} = 15 \text{Vdc}$ , $V_{GS} = 0$ , $f = 1.0 \text{kHz}$ )	$ y_{os} $	-	50	$\mu\text{mhos}$
Input Capacitance ( $V_{DS} = 15 \text{Vdc}$ , $V_{GS} = 0$ , $f = 1.0 \text{MHz}$ )	$C_{iss}$	-	4.0	pF
Reverse Transfer Capacitance ( $V_{DS} = 15 \text{Vdc}$ , $V_{GS} = 0$ , $f = 10 \text{MHz}$ )	$C_{rss}$	-	0.8	pF
Output Capacitance ( $V_{DS} = 15 \text{Vdc}$ , $V_{GS} = 0$ , $f = 1.0 \text{MHz}$ )	$C_{oss}$	-	2.0	pF

## COMMON SOURCE CHARACTERISTICS ADMITTANCE PARAMETERS

( $V_{DS} = 15 \text{Vdc}$ ,  $T_{channel} = 25^\circ\text{C}$ )

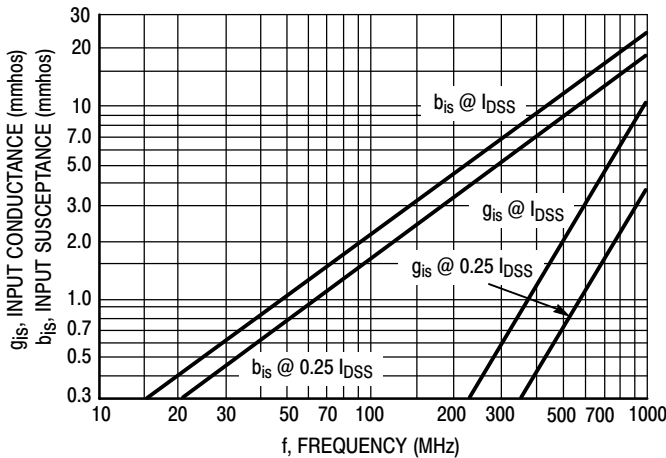


Figure 1. Input Admittance ( $y_{is}$ )

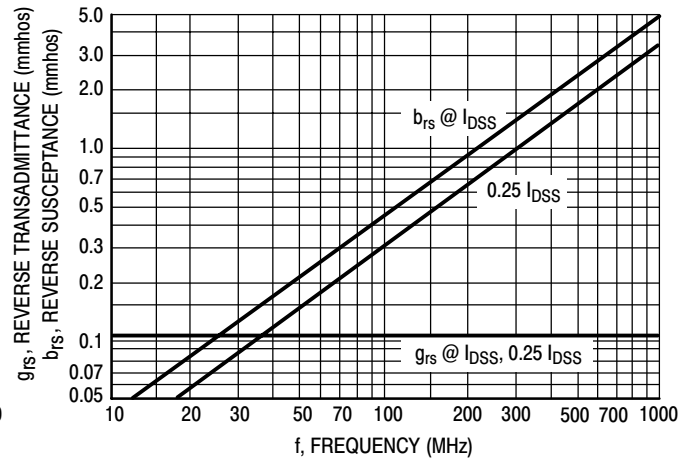


Figure 2. Reverse Transfer Admittance ( $y_{rs}$ )

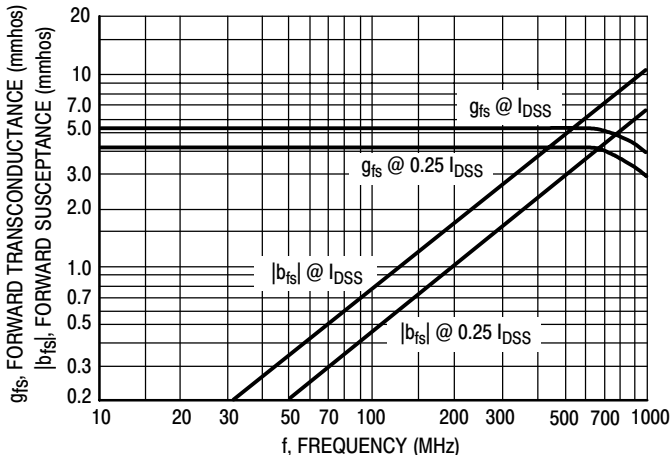


Figure 3. Forward Transadmittance ( $y_{fs}$ )

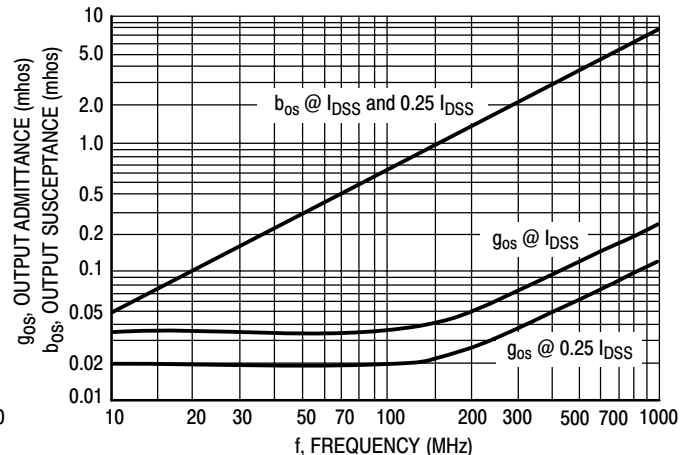


Figure 4. Output Admittance ( $y_{os}$ )

COMMON SOURCE CHARACTERISTICS  
S-PARAMETERS

( $V_{DS} = 15 \text{ Vdc}$ ,  $T_{\text{channel}} = 25^\circ\text{C}$ , Data Points in MHz)

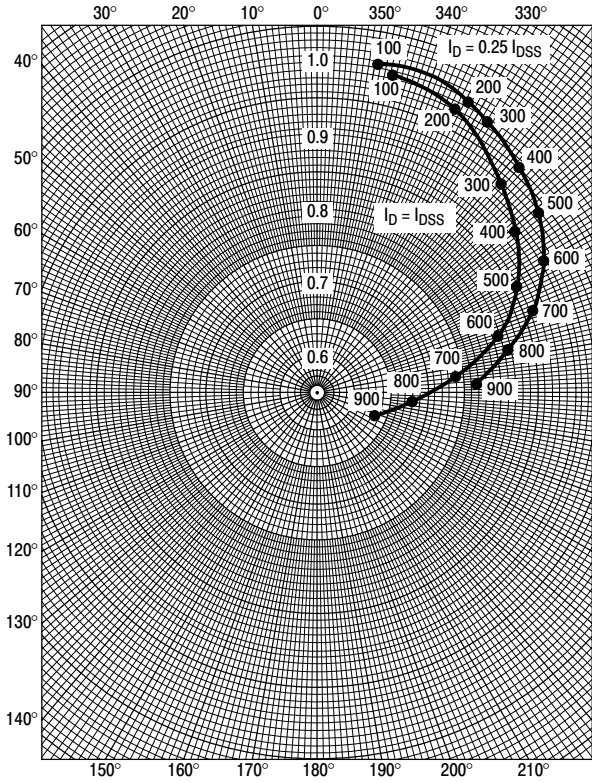


Figure 5.  $S_{11s}$

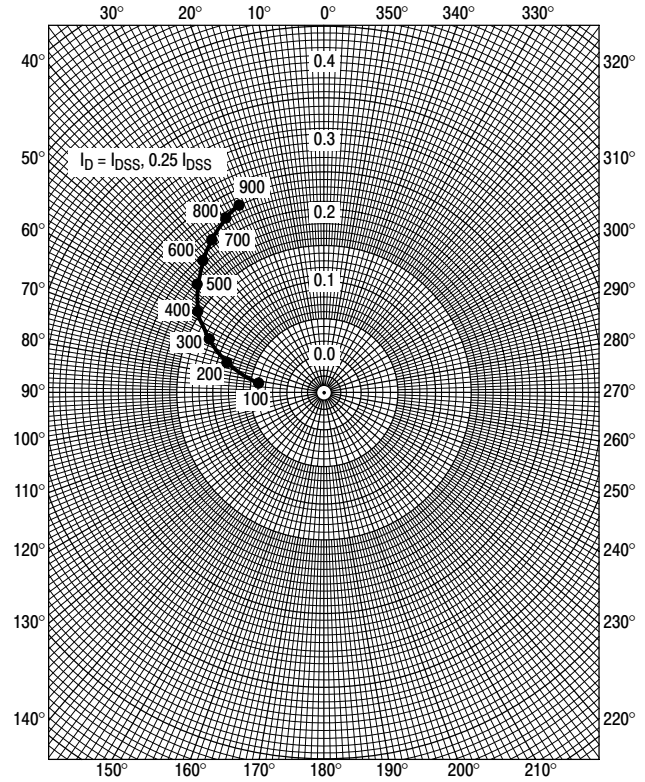


Figure 6.  $S_{12s}$

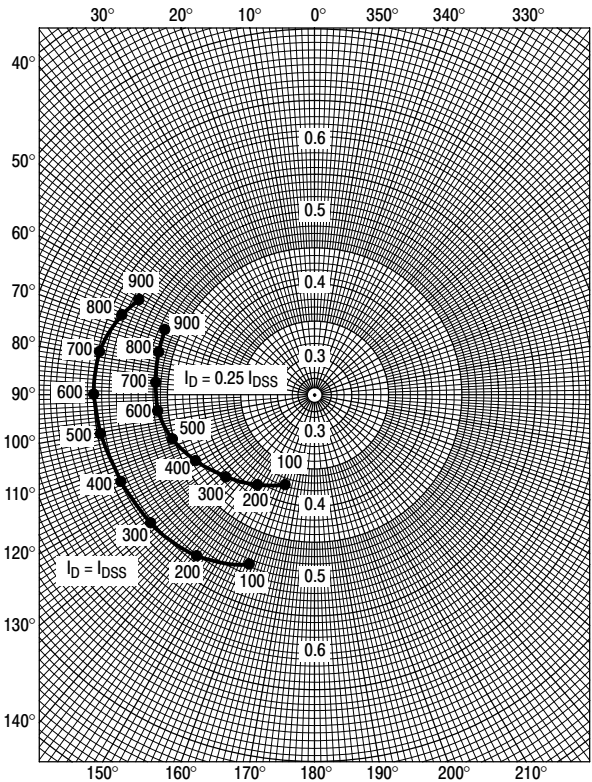


Figure 7.  $S_{21s}$

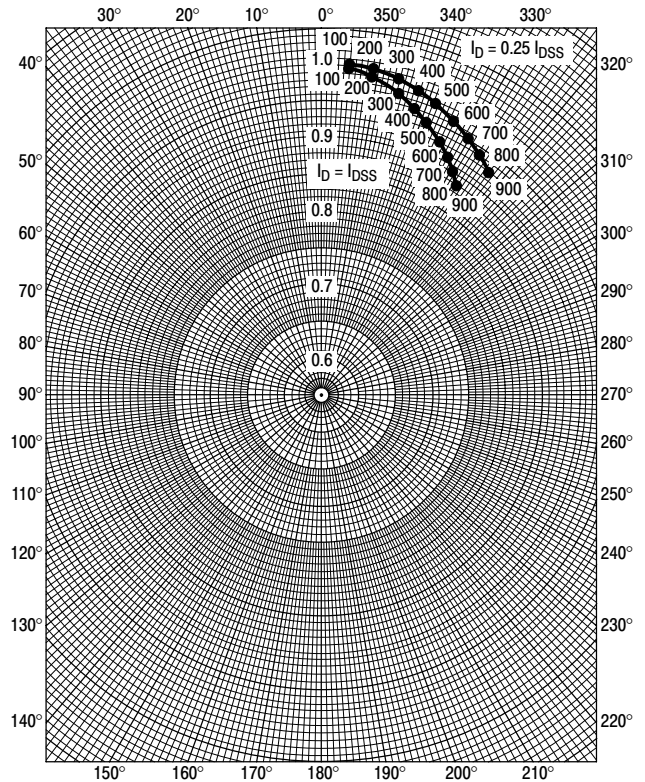


Figure 8.  $S_{22s}$

# MMBF4416LT1

## COMMON GATE CHARACTERISTICS ADMITTANCE PARAMETERS

( $V_{DG} = 15 \text{ Vdc}$ ,  $T_{\text{channel}} = 25^\circ\text{C}$ )

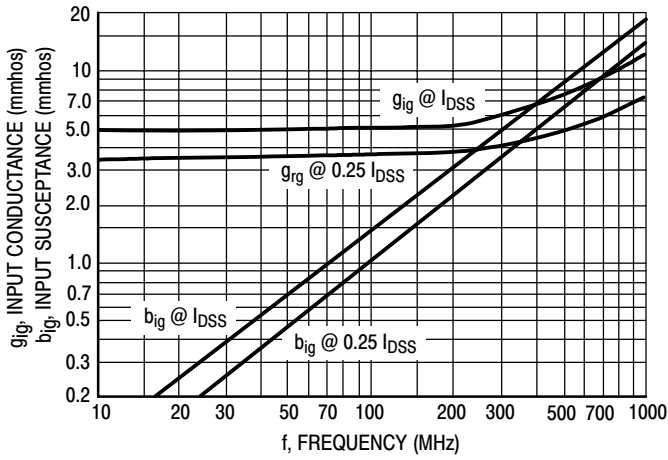


Figure 9. Input Admittance ( $y_{ig}$ )

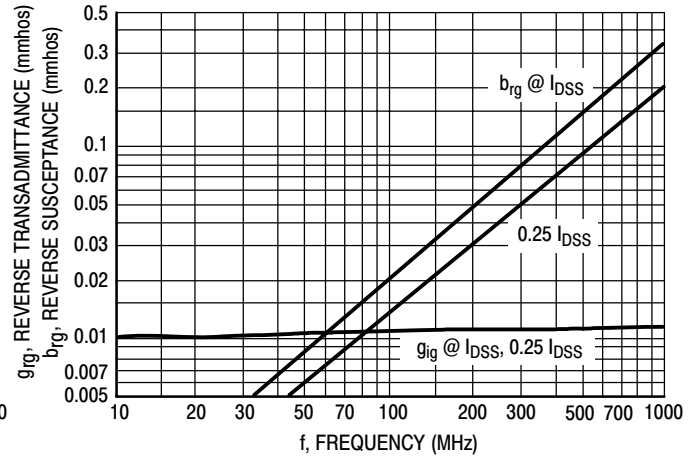


Figure 10. Reverse Transfer Admittance ( $y_{rg}$ )

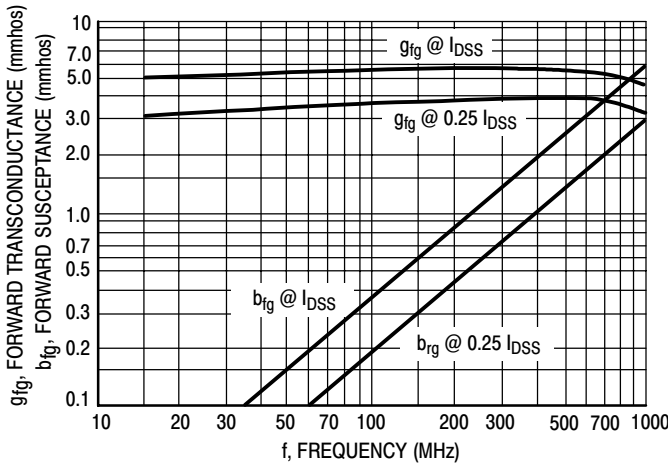


Figure 11. Forward Transfer Admittance ( $y_{fg}$ )

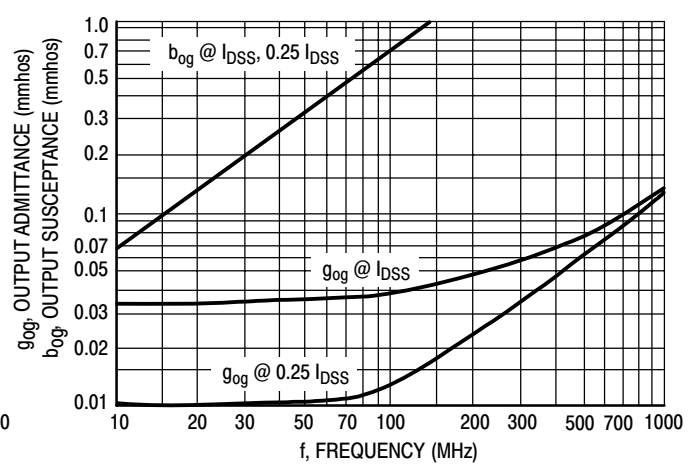


Figure 12. Output Admittance ( $y_{og}$ )

COMMON GATE CHARACTERISTICS  
S-PARAMETERS

( $V_{DS} = 15$  Vdc,  $T_{channel} = 25^{\circ}\text{C}$ , Data Points in MHz)

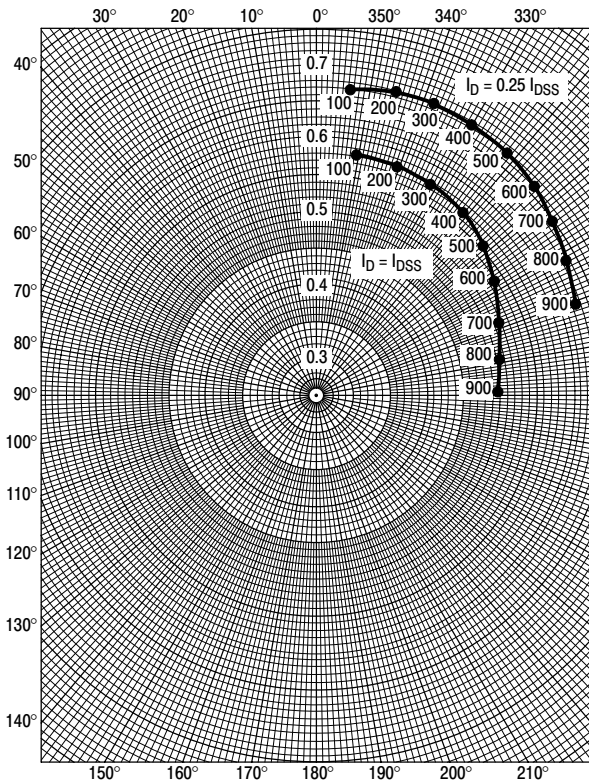


Figure 13.  $S_{11g}$

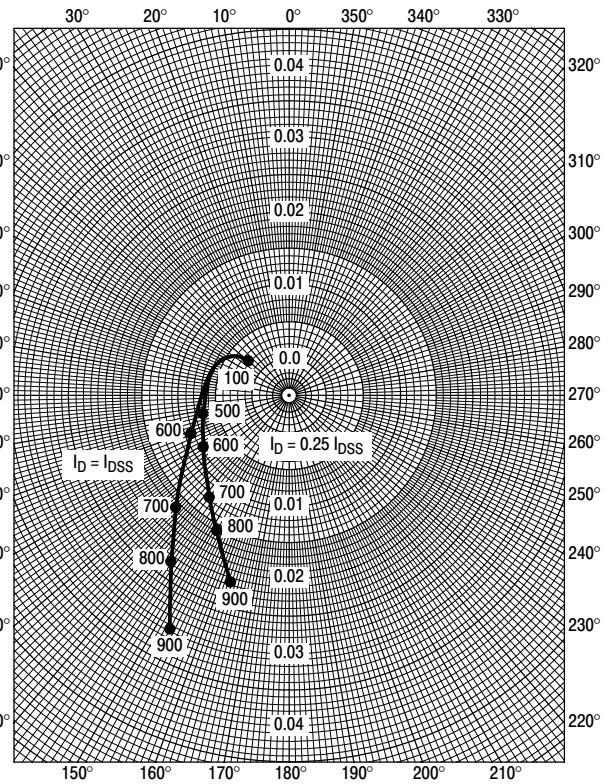


Figure 14.  $S_{12g}$

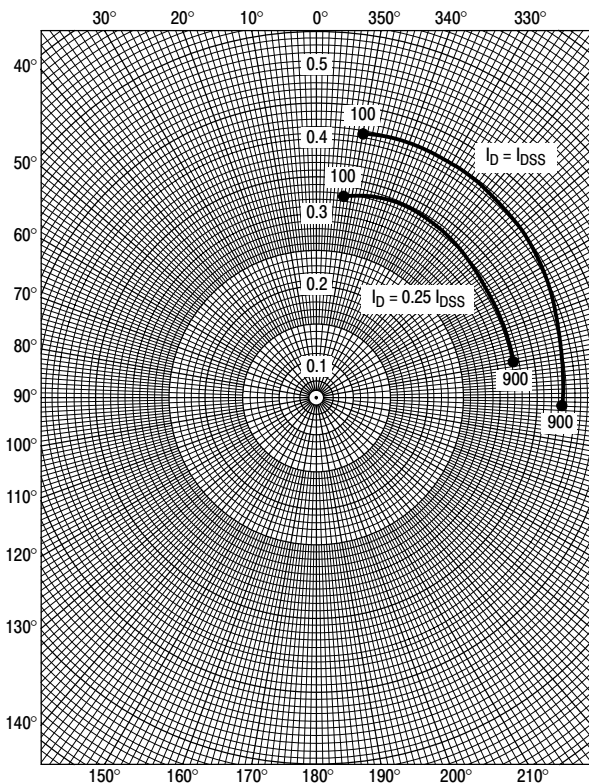


Figure 15.  $S_{21g}$

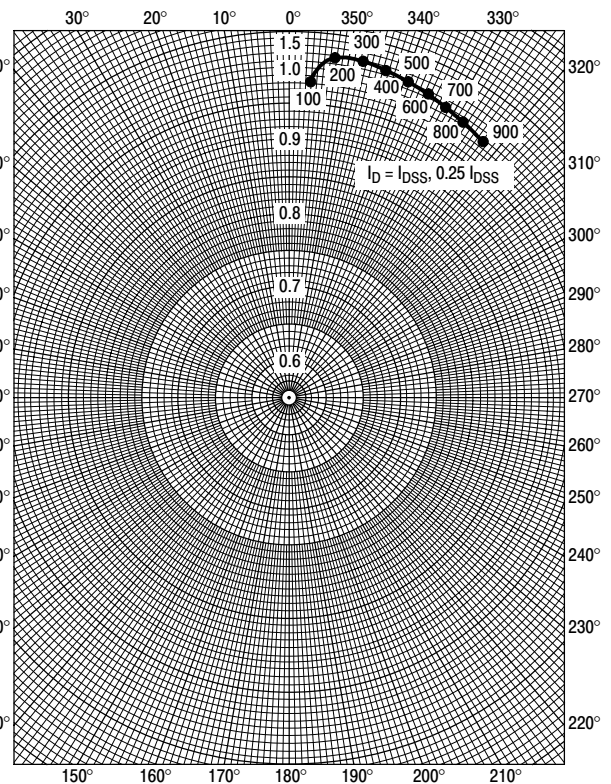


Figure 16.  $S_{22g}$

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



**SOT-23 (TO-236)**  
CASE 318  
ISSUE AT

DATE 01 MAR 2023

SCALE 4:1



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H <sub>E</sub>	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

**GENERIC MARKING DIAGRAM\***



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



**RECOMMENDED MOUNTING FOOTPRINT**

\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**STYLES ON PAGE 2**

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**MECHANICAL CASE OUTLINE**  
**PACKAGE DIMENSIONS**



**SOT-23 (TO-236)**  
**CASE 318**  
**ISSUE AT**

DATE 01 MAR 2023

- |   |   |   |   |   |   |
|---|---|---|---|---|---|
| STYLE 1 THRU 5:<br>CANCELLED                            | STYLE 6:<br>PIN 1. BASE<br>2. EMITTER<br>3. COLLECTOR | STYLE 7:<br>PIN 1. EMITTER<br>2. BASE<br>3. COLLECTOR       | STYLE 8:<br>PIN 1. ANODE<br>2. NO CONNECTION<br>3. CATHODE  |   |   |
| STYLE 9:<br>PIN 1. ANODE<br>2. ANODE<br>3. CATHODE      | STYLE 10:<br>PIN 1. DRAIN<br>2. SOURCE<br>3. GATE     | STYLE 11:<br>PIN 1. ANODE<br>2. CATHODE<br>3. CATHODE-ANODE | STYLE 12:<br>PIN 1. CATHODE<br>2. CATHODE<br>3. ANODE       | STYLE 13:<br>PIN 1. SOURCE<br>2. DRAIN<br>3. GATE           | STYLE 14:<br>PIN 1. CATHODE<br>2. GATE<br>3. ANODE          |
| STYLE 15:<br>PIN 1. GATE<br>2. CATHODE<br>3. ANODE      | STYLE 16:<br>PIN 1. ANODE<br>2. CATHODE<br>3. CATHODE | STYLE 17:<br>PIN 1. NO CONNECTION<br>2. ANODE<br>3. CATHODE | STYLE 18:<br>PIN 1. NO CONNECTION<br>2. CATHODE<br>3. ANODE | STYLE 19:<br>PIN 1. CATHODE<br>2. ANODE<br>3. CATHODE-ANODE | STYLE 20:<br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE          |
| STYLE 21:<br>PIN 1. GATE<br>2. SOURCE<br>3. DRAIN       | STYLE 22:<br>PIN 1. RETURN<br>2. OUTPUT<br>3. INPUT   | STYLE 23:<br>PIN 1. ANODE<br>2. ANODE<br>3. CATHODE         | STYLE 24:<br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE           | STYLE 25:<br>PIN 1. ANODE<br>2. CATHODE<br>3. GATE          | STYLE 26:<br>PIN 1. CATHODE<br>2. ANODE<br>3. NO CONNECTION |
| STYLE 27:<br>PIN 1. CATHODE<br>2. CATHODE<br>3. CATHODE | STYLE 28:<br>PIN 1. ANODE<br>2. ANODE<br>3. ANODE     |   |   |   |   |

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