

MC74VHC00

Quad 2-Input NAND Gate

The MC74VHC00 is an advanced high speed CMOS 2-input NAND gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7 V, allowing the interface of 5 V systems to 3 V systems.

Features

- High Speed: $t_{PD} = 3.7 \text{ ns}$ (Typ) at $V_{CC} = 5 \text{ V}$
- Low Power Dissipation: $I_{CC} = 2 \mu\text{A}$ (Max) at $T_A = 25^\circ\text{C}$
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2 V to 5.5 V Operating Range
- Low Noise: $V_{OLP} = 0.8 \text{ V}$ (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 32 FETs or 8 Equivalent Gates
- These Devices are Pb-Free and are RoHS Compliant

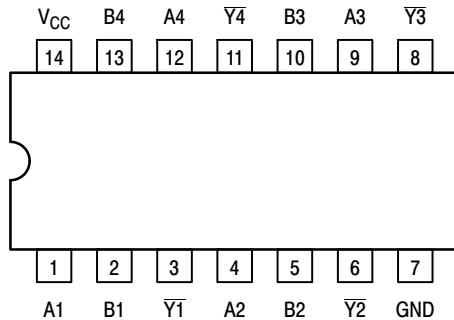


Figure 1. Pinout: 14-Lead Packages
(Top View)

FUNCTION TABLE

| Inputs | | Output |
|--------|---|-----------|
| A | B | \bar{Y} |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |



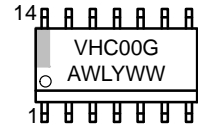
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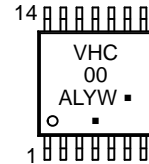
MARKING DIAGRAMS



SO-14
D SUFFIX
CASE 751A



TSSOP-14
DT SUFFIX
CASE 948G



A = Assembly Location
L, WL = Wafer Lot
Y = Year
W, WW = Work Week
G, ■ = Pb-Free Device

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MC74VHC00

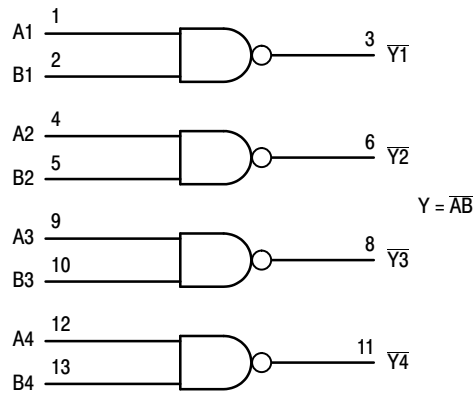


Figure 2. Logic Diagram

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit | |
|----------------|--|--|---------------|----|
| V_{CC} | Positive DC Supply Voltage | -0.5 to +7.0 | V | |
| V_{IN} | Digital Input Voltage | -0.5 to +7.0 | V | |
| V_{OUT} | DC Output Voltage | -0.5 to $V_{CC} + 0.5$ | V | |
| I_{IK} | Input Diode Current | -20 | mA | |
| I_{OK} | Output Diode Current | ± 20 | mA | |
| I_{OUT} | DC Output Current, per Pin | ± 25 | mA | |
| I_{CC} | DC Supply Current, V_{CC} and GND Pins | ± 75 | mA | |
| P_D | Power Dissipation in Still Air | SOIC Package 200 TSSOP 180 | mW | |
| T_{STG} | Storage Temperature Range | -65 to +150 | $^{\circ}C$ | |
| V_{ESD} | ESD Withstand Voltage | Human Body Model (Note 1) >2000 Machine Model (Note 2) >200 Charged Device Model (Note 3) N/A | V | |
| $I_{LATCH-UP}$ | Latch-Up Performance | Above V_{CC} and Below GND at 125 $^{\circ}C$ (Note 4) | ± 300 | mA |
| θ_{JA} | Thermal Resistance, Junction to Ambient | SOIC Package 143 TSSOP 164 | $^{\circ}C/W$ | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22-A114-A
2. Tested to EIA/JESD22-A115-A
3. Tested to JESD22-C101-A
4. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

| Symbol | Characteristics | Min | Max | Unit |
|------------|--|-----|----------|-------------|
| V_{CC} | DC Supply Voltage | 2.0 | 5.5 | V |
| V_{IN} | DC Input Voltage | 0 | 5.5 | V |
| V_{OUT} | DC Output Voltage | 0 | V_{CC} | V |
| T_A | Operating Temperature Range, All Package Types | -55 | 125 | $^{\circ}C$ |
| t_r, t_f | Input Rise or Fall Time | | | |
| | $V_{CC} = 3.3 V \pm 0.3 V$ | 0 | 100 | ns/V |
| | $V_{CC} = 5.0 V \pm 0.5 V$ | 0 | 20 | |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

MC74VHC00

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | V _{CC} V | T _A = 25°C | | | T _A = -40 to 85°C | | T _A = -55 to +125°C | | Unit |
|-----------------|---------------------------|--|----------------------|----------------------------------|-------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|------|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| V _{IH} | High-Level Input Voltage | | 2.0 3.0 to 5.5 | 1.50 V _{CC} × 0.7 | | | 1.50 V _{CC} × 0.7 | | 1.50 V _{CC} × 0.7 | | V |
| V _{IL} | Low-Level Input Voltage | | 2.0 3.0 to 5.5 | | | 0.50 V _{CC} × 0.3 | | 0.50 V _{CC} × 0.3 | | 0.50 V _{CC} × 0.3 | V |
| V _{OH} | High-Level Output Voltage | V _{in} = V _{IH} or V _{IL} I _{OH} = - 50 μA | 2.0 3.0 4.5 | 1.9 2.9 4.4 | 2.0 3.0 4.5 | | 1.9 2.9 4.4 | | 1.9 2.9 4.4 | | V |
| | | V _{in} = V _{IH} or V _{IL} I _{OH} = - 4 mA I _{OH} = - 8 mA | 3.0 4.5 | 2.58 3.94 | | | 2.48 3.80 | | 2.40 3.70 | | |
| V _{OL} | Low-Level Output Voltage | V _{in} = V _{IH} or V _{IL} I _{OL} = 50 μA | 2.0 3.0 4.5 | | 0.0 0.0 0.0 | 0.1 0.1 0.1 | | 0.1 0.1 0.1 | | 0.1 0.1 0.1 | V |
| | | V _{in} = V _{IH} or V _{IL} I _{OL} = 4 mA I _{OL} = 8 mA | 3.0 4.5 | | | 0.36 0.36 | | 0.44 0.44 | | 0.55 0.55 | |
| I _{in} | Input Leakage Current | V _{in} = 5.5 V or GND | 0 to 5.5 | | | ±0.1 | | ±1.0 | | ±2.0 | μA |
| I _{CC} | Quiescent Supply Current | V _{in} = V _{CC} or GND | 5.5 | | | 2.0 | | 20 | | 40 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0 ns)

| Symbol | Parameter | Test Conditions | T _A = 25°C | | | T _A = -40 to 85°C | | T _A = -55 to +125°C | | Unit |
|--|--|---|-----------------------|------------|-------------|------------------------------|-------------|--------------------------------|------------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| t _{PLH} , t _{PHL} | Propagation Delay, A or B to \bar{Y} | V _{CC} = 3.3 ± 0.3 V C _L = 15 pF C _L = 50 pF | | 5.5 8.0 | 7.9 11.4 | 1.0 1.0 | 9.5 13.0 | 1.0 1.0 | 10 14.5 | ns |
| | | V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF | | 3.7 5.2 | 5.5 7.5 | 1.0 1.0 | 6.5 8.5 | 1.0 1.0 | 7.0 9.5 | |
| C _{in} | Input Capacitance | | | 4.0 10 | | | 10 | | 10 | pF |

| | | | | |
|-----------------|--|---|--|----|
| C _{PD} | Power Dissipation Capacitance (Note 5) | Typical @ 25°C, V _{CC} = 5.0 V | | pF |
| | | 19 | | |

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/4 (per gate). C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

NOISE CHARACTERISTICS (Input t_r = t_f = 3.0 ns, C_L = 50 pF, V_{CC} = 5.0 V, Measured in SOIC Package)

| Symbol | Characteristic | T _A = 25°C | | Unit |
|------------------|--|-----------------------|-------|------|
| | | Typ | Max | |
| V _{OLP} | Quiet Output Maximum Dynamic V _{OL} | 0.3 | 0.8 | V |
| V _{OLV} | Quiet Output Minimum Dynamic V _{OL} | - 0.3 | - 0.8 | V |
| V _{IHD} | Minimum High Level Dynamic Input Voltage | | 3.5 | V |
| V _{ILD} | Maximum Low Level Dynamic Input Voltage | | 1.5 | V |

MC74VHC00

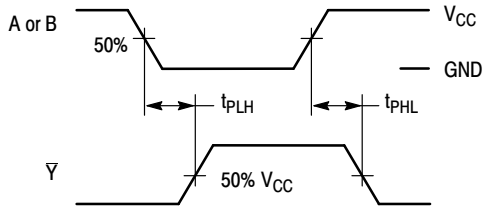
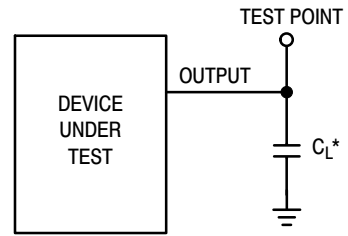


Figure 3. Switching Waveforms



*Includes all probe and jig capacitance

Figure 4. Test Circuit

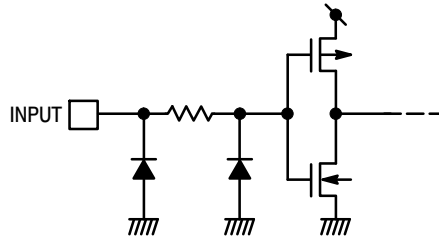


Figure 5. Input Equivalent Circuit

ORDERING INFORMATION

| Device | Package | Shipping† |
|----------------|------------------------|--------------------|
| MC74VHC00DR2G | SOIC-14 (Pb-Free) | 2500 / Tape & Reel |
| MC74VHC00DTG | TSSOP-14* (Pb-Free) | 96 Units / Rail |
| MC74VHC00DTR2G | TSSOP-14* (Pb-Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

SOIC-14 NB
CASE 751A-03
ISSUE L

DATE 03 FEB 2016



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.054 | 0.068 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A3 | 0.19 | 0.25 | 0.008 | 0.010 |
| b | 0.35 | 0.49 | 0.014 | 0.019 |
| D | 8.55 | 8.75 | 0.337 | 0.344 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.019 |
| L | 0.40 | 1.25 | 0.016 | 0.049 |
| M | 0° | 7° | 0° | 7° |

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

STYLES ON PAGE 2

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SOIC-14
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. NO CONNECTION
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 2:
 CANCELLED

STYLE 3:
 PIN 1. NO CONNECTION
 2. ANODE
 3. ANODE
 4. NO CONNECTION
 5. ANODE
 6. NO CONNECTION
 7. ANODE
 8. ANODE
 9. ANODE
 10. NO CONNECTION
 11. ANODE
 12. ANODE
 13. NO CONNECTION
 14. COMMON CATHODE

STYLE 4:
 PIN 1. NO CONNECTION
 2. CATHODE
 3. CATHODE
 4. NO CONNECTION
 5. CATHODE
 6. NO CONNECTION
 7. CATHODE
 8. CATHODE
 9. CATHODE
 10. NO CONNECTION
 11. CATHODE
 12. CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 5:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. COMMON ANODE
 8. COMMON CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 6:
 PIN 1. CATHODE
 2. CATHODE
 3. CATHODE
 4. CATHODE
 5. CATHODE
 6. CATHODE
 7. CATHODE
 8. ANODE
 9. ANODE
 10. ANODE
 11. ANODE
 12. ANODE
 13. ANODE
 14. ANODE

STYLE 7:
 PIN 1. ANODE/CATHODE
 2. COMMON ANODE
 3. COMMON CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. COMMON CATHODE
 12. COMMON ANODE
 13. ANODE/CATHODE
 14. ANODE/CATHODE

STYLE 8:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. COMMON ANODE
 8. COMMON ANODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. NO CONNECTION
 12. ANODE/CATHODE
 13. ANODE/CATHODE
 14. COMMON CATHODE

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



TSSOP-14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016

SCALE 2:1



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

GENERIC MARKING DIAGRAM*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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