

Dual J-K Flip-Flop with Reset

MC74HC73A

The MC74HC73A is identical in pinout to the LS73. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

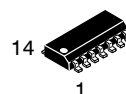
Each flip-flop is negative-edge clocked and has an active-low asynchronous reset.

The MC74HC73A is identical in function to the HC107, but has a different pinout.

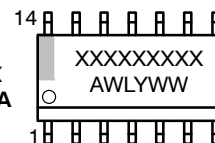
Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the JEDEC Standard No. 7.0 A Requirements
- Chip Complexity: 92 FETs or 23 Equivalent Gates
- -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

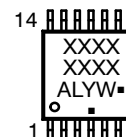
MARKING DIAGRAMS



SOIC-14
D SUFFIX
CASE 751A



TSSOP-14
DT SUFFIX
CASE 948G



XXXX = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 7 of this data sheet.

MC74HC73A

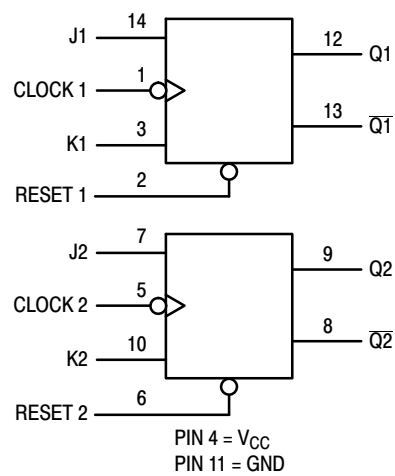


Figure 1. Logic Diagram

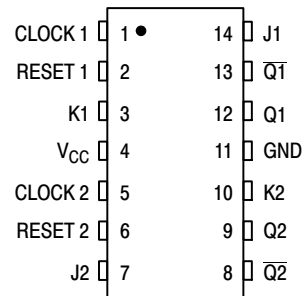


Figure 2. Pinout (Top View)

FUNCTION TABLE

| Inputs | | | | Outputs | |
|--------|-------|---|---|-----------|----------------|
| Reset | Clock | J | K | Q | \overline{Q} |
| L | X | X | X | L | H |
| H | | L | L | No Change | |
| H | | L | H | L | H |
| H | | H | L | H | L |
| H | | H | H | Toggle | |
| H | L | X | X | No Change | |
| H | H | X | X | No Change | |
| H | | X | X | No Change | |

MC74HC73A

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---------------|--|---|------|
| V_{CC} | DC Supply Voltage | −0.5 to +6.5 | V |
| V_{IN} | DC Input Voltage | −0.5 to $V_{CC} + 0.5$ | V |
| V_{OUT} | DC Output Voltage | −0.5 to $V_{CC} + 0.5$ | V |
| I_{IN} | DC Input Diode Current, per Pin | ±20 | mA |
| I_{OUT} | DC Output Diode Current, per Pin | ±25 | mA |
| I_{CC} | DC Supply Current, V_{CC} and GND Pins | ±50 | mA |
| I_{IK} | Input Clamp Current ($V_{IN} < 0$ or $V_{IN} > V_{CC}$) | ±20 | mA |
| I_{OK} | Output Clamp Current ($V_{OUT} < 0$ or $V_{OUT} > V_{CC}$) | ±20 | mA |
| T_{STG} | Storage Temperature Range | −65 to +150 | °C |
| T_L | Lead Temperature, 1 mm from Case for 10 Seconds | 260 | °C |
| T_J | Junction Temperature Under Bias | ±150 | °C |
| θ_{JA} | Thermal Resistance (Note 1) | SOIC−14 TSSOP−14 116 150 | °C/W |
| P_D | Power Dissipation in Still Air at 25°C | SOIC−14 TSSOP−14 1077 833 | mW |
| MSL | Moisture Sensitivity | Level 1 | – |
| F_R | Flammability Rating | Oxygen Index: 28 to 34 UL 94 V−0 @ 0.125 in | – |
| V_{ESD} | ESD Withstand Voltage (Note 2) | Human Body Model Charged Device Model > 2000 N/A | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76mm-by-114mm, 2-ounce copper trace no air flow per JESD51-7.
2. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|-------------------|---|--|--------------------|------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V |
| V_{IN}, V_{OUT} | DC Input Voltage, Output Voltage (Referenced to GND) (Note 3) | 0 | V_{CC} | V |
| T_A | Operating Free-Air Temperature | − 55 | + 125 | °C |
| t_r, t_f | Input Rise and Fall Time | $V_{CC} = 2.0\text{ V}$ $V_{CC} = 4.5\text{ V}$ $V_{CC} = 6.0\text{ V}$ 0 0 0 | 1000 500 400 | ns |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

MC74HC73A

DC ELECTRICAL CHARACTERISTICS (MC74HC73A)

| Symbol | Parameter | Test Conditions | V _{CC} V | Guaranteed Limit | | | Unit |
|-----------------|--|--|--------------------------|---------------------------|---------------------------|---------------------------|------|
| | | | | – 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| V _{IH} | Minimum High-Level Input Voltage | V _{OUT} = 0.1 V or V _{CC} – 0.1 V I _{OUT} ≤ 20 µA | 2.0 3.0 4.5 6.0 | 1.5 2.1 3.15 4.2 | 1.5 2.1 3.15 4.2 | 1.5 2.1 3.15 4.2 | V |
| V _{IL} | Maximum Low-Level Input Voltage | V _{OUT} = 0.1 V or V _{CC} – 0.1 V I _{OUT} ≤ 20 µA | 2.0 3.0 4.5 6.0 | 0.3 0.9 1.35 1.8 | 0.3 0.9 1.35 1.8 | 0.3 0.9 1.35 1.8 | V |
| V _{OH} | Minimum High-Level Output Voltage | V _{IN} = V _{IH} or V _{IL} | | | | | V |
| | | I _{OUT} ≤ 20 µA | 2.0 4.5 6.0 | 1.9 4.4 5.9 | 1.9 4.4 5.9 | 1.9 4.4 5.9 | |
| | | I _{OUT} ≤ 2.4 mA | 3.0 | 2.48 | 2.34 | 2.2 | |
| | | I _{OUT} ≤ 4.0 mA | 4.5 | 3.98 | 3.84 | 3.7 | |
| V _{OL} | Maximum Low-Level Output Voltage | V _{IN} = V _{IH} or V _{IL} | | | | | V |
| | | I _{OUT} ≤ 20 µA | 2.0 4.5 6.0 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | |
| | | I _{OUT} ≤ 2.4 mA | 3.0 | 0.26 | 0.33 | 0.40 | |
| | | I _{OUT} ≤ 4.0 mA | 4.5 | 0.26 | 0.33 | 0.40 | |
| I _{IN} | Maximum Input Leakage Current | V _{IN} = V _{CC} or GND | 6.0 | ± 0.1 | ± 1.0 | ± 1.0 | µA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{IN} = V _{CC} or GND I _{OUT} = 0 µA | 6.0 | 2.0 | 20 | 80 | µA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

MC74HC73A

AC ELECTRICAL CHARACTERISTICS (MC74HC73A)

| Symbol | Parameter | V _{CC} V | Guaranteed Limit | | | Unit |
|--|--|----------------------|------------------|--------|---------|------|
| | | | – 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| f _{MAX} | Maximum Clock Frequency (50% Duty Cycle) (Figure 4) | 2.0 | 6.0 | 4.8 | 4.0 | MHz |
| | | 3.0 | 15 | 10 | 8.0 | |
| | | 4.5 | 30 | 24 | 20 | |
| | | 6.0 | 35 | 28 | 24 | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Clock to Q or \bar{Q} (Figure 4) | 2.0 | 125 | 155 | 190 | ns |
| | | 3.0 | TBD | TBD | TBD | |
| | | 4.5 | 25 | 31 | 38 | |
| | | 6.0 | 21 | 26 | 32 | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Reset to Q or \bar{Q} (Figure 5) | 2.0 | 155 | 195 | 235 | ns |
| | | 3.0 | TBD | TBD | TBD | |
| | | 4.5 | 31 | 39 | 47 | |
| | | 6.0 | 26 | 33 | 40 | |
| t _{TLH} , t _{THL} | Maximum Output Transition Time, Any Output (Figure 4) | 2.0 | 75 | 95 | 110 | ns |
| | | 3.0 | 30 | 40 | 55 | |
| | | 4.5 | 15 | 19 | 22 | |
| | | 6.0 | 13 | 16 | 19 | |
| C _{IN} | Maximum Input Capacitance | — | 10 | 10 | 10 | pF |

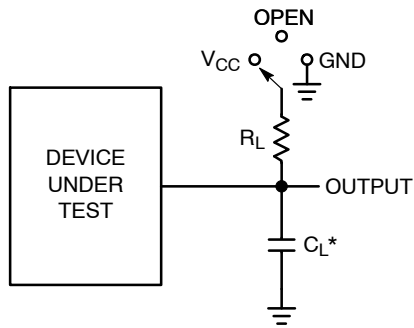
| | | | | |
|-----------------|---|-----|---|----|
| C _{PD} | Power Dissipation Capacitance (Per Enabled Output) (Note 4) | 5.0 | Typical @ 25°C, V _{CC} = 5.0 V | pF |
| | | | 35 | |

4. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

TIMING REQUIREMENTS (MC74HC73A)

| Symbol | Parameter | V _{CC} V | Guaranteed Limit | | | Unit |
|---------------------------------|--|----------------------|------------------|--------|---------|------|
| | | | – 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| t _{su} | Minimum Setup Time, J or K to Clock (Figure 6) | 2.0 | 100 | 125 | 150 | ns |
| | | 3.0 | TBD | TBD | TBD | |
| | | 4.5 | 20 | 25 | 30 | |
| | | 6.0 | 17 | 21 | 26 | |
| t _h | Minimum Hold Time, Clock to J or K (Figure 6) | 2.0 | 3.0 | 3.0 | 3.0 | ns |
| | | 3.0 | 3.0 | 3.0 | 3.0 | |
| | | 4.5 | 3.0 | 3.0 | 3.0 | |
| | | 6.0 | 3.0 | 3.0 | 3.0 | |
| t _{rec} | Minimum Recovery Time, Reset Inactive to Clock (Figure 5) | 2.0 | 100 | 125 | 150 | ns |
| | | 3.0 | TBD | TBD | TBD | |
| | | 4.5 | 20 | 25 | 30 | |
| | | 6.0 | 17 | 21 | 26 | |
| t _w | Minimum Pulse Width, Clock (Figure 4) | 2.0 | 80 | 100 | 120 | ns |
| | | 3.0 | TBD | TBD | TBD | |
| | | 4.5 | 16 | 20 | 24 | |
| | | 6.0 | 14 | 17 | 20 | |
| t _w | Minimum Pulse Width, Reset (Figure 5) | 2.0 | 80 | 100 | 120 | ns |
| | | 3.0 | TBD | TBD | TBD | |
| | | 4.5 | 16 | 20 | 24 | |
| | | 6.0 | 14 | 17 | 20 | |
| t _r , t _f | Maximum Input Rise and Fall Times (Figure 4) | 2.0 | 1000 | 1000 | 1000 | ns |
| | | 3.0 | 800 | 800 | 800 | |
| | | 4.5 | 500 | 500 | 500 | |
| | | 6.0 | 400 | 400 | 400 | |

MC74HC73A



*C_L Includes probe and jig capacitance

| Test | Switch Position | C _L | R _L |
|-------------------------------------|-----------------|----------------|----------------|
| t _{PLH} / t _{PHL} | Open | 50 pF | 1 kΩ |
| t _{PLZ} / t _{PZL} | V _{CC} | | |
| t _{PHZ} / t _{PZH} | GND | | |

Figure 3. Test Circuit

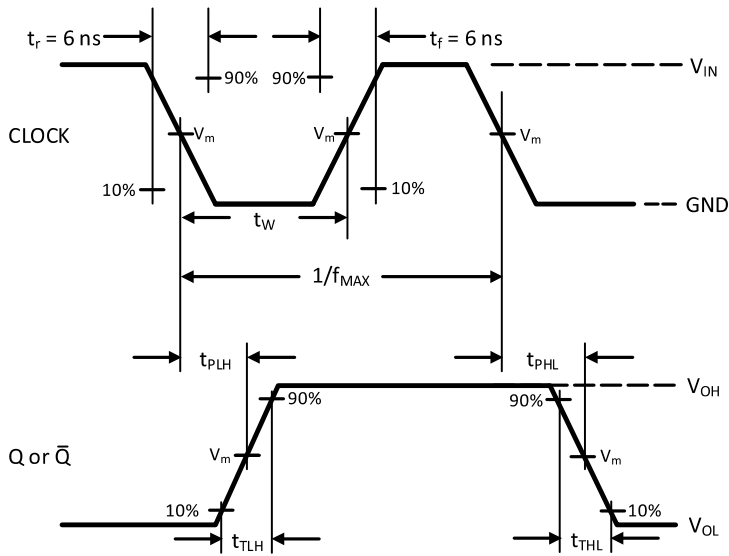


Figure 4.

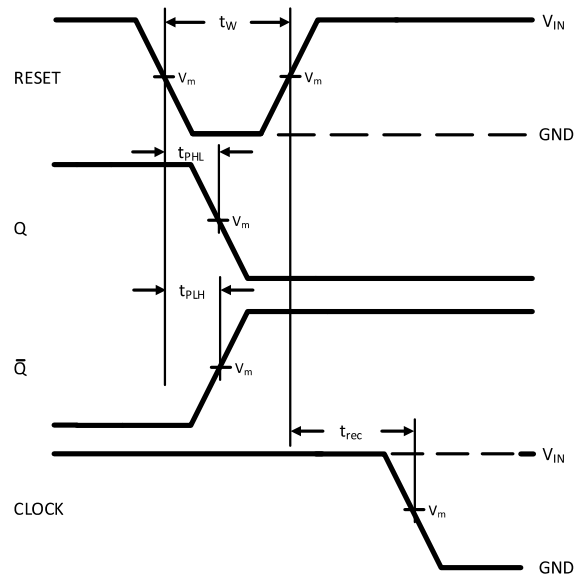


Figure 5.

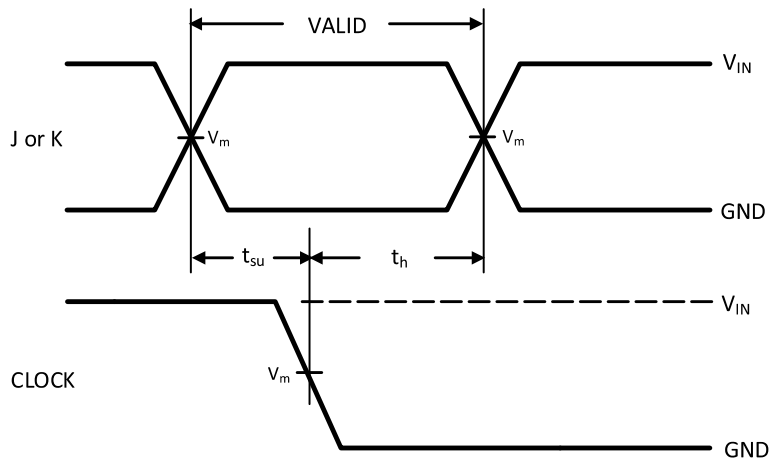


Figure 6.

| Device | V _{IN} , V | V _m , V |
|-----------|---------------------|-----------------------|
| MC74HC73A | V _{CC} | 50% x V _{CC} |

MC74HC73A

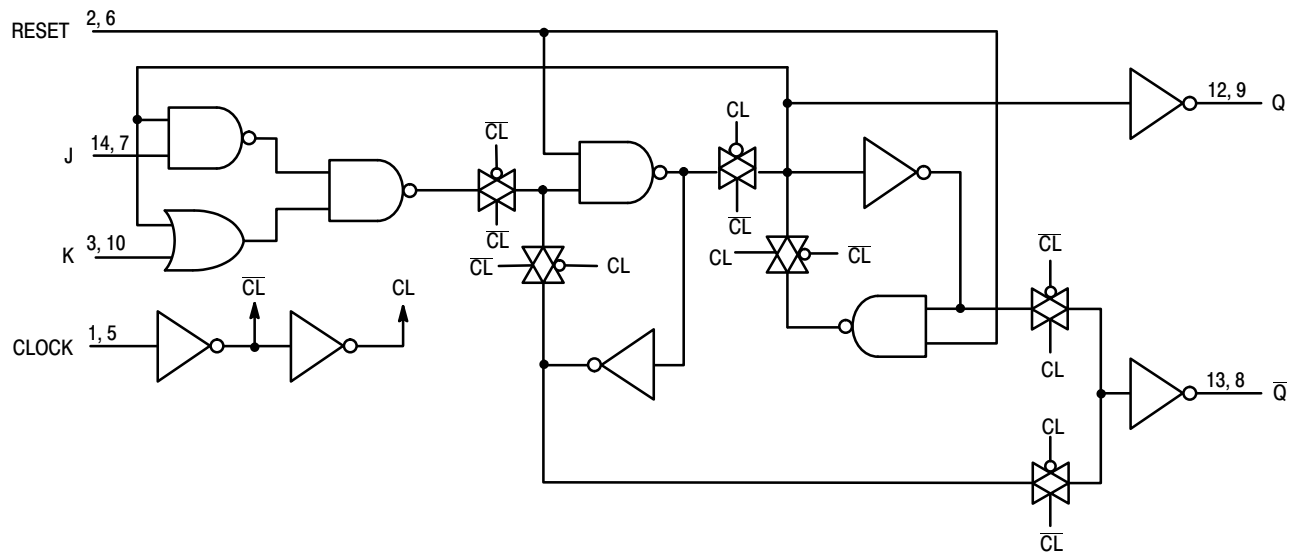


Figure 7. Expanded Logic Diagram

ORDERING INFORMATION

| Device | Marking | Package | Shipping [†] |
|------------------|-----------|----------|-----------------------|
| MC74HC73ADG | HC73AG | SOIC-14 | 55 Units / Rail |
| MC74HC73ADR2G | HC73AG | SOIC-14 | 2500 / Tape & Reel |
| MC74HC73ADR2G-Q* | HC73AG | SOIC-14 | 2500 / Tape & Reel |
| MC74HC73ADTR2G | HC 73A | TSSOP-14 | 2500 / Tape & Reel |

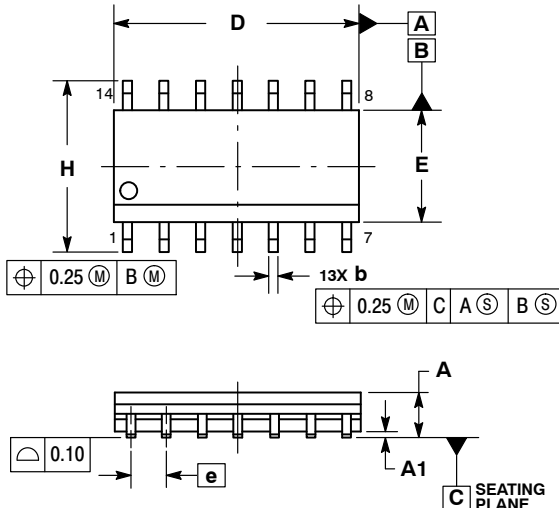
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.



SOIC-14 NB
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

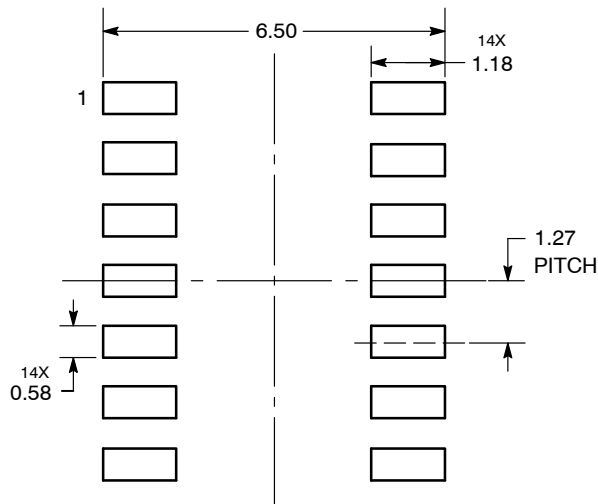


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.054 | 0.068 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A3 | 0.19 | 0.25 | 0.008 | 0.010 |
| b | 0.35 | 0.49 | 0.014 | 0.019 |
| D | 8.55 | 8.75 | 0.337 | 0.344 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.019 |
| L | 0.40 | 1.25 | 0.016 | 0.049 |
| M | 0° | 7° | 0° | 7° |

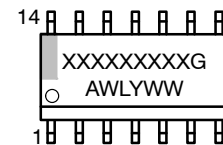
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
 A = Assembly Location
 WL = Wafer Lot
 Y = Year
 WW = Work Week
 G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC-14
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

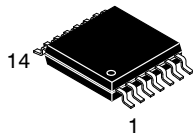
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PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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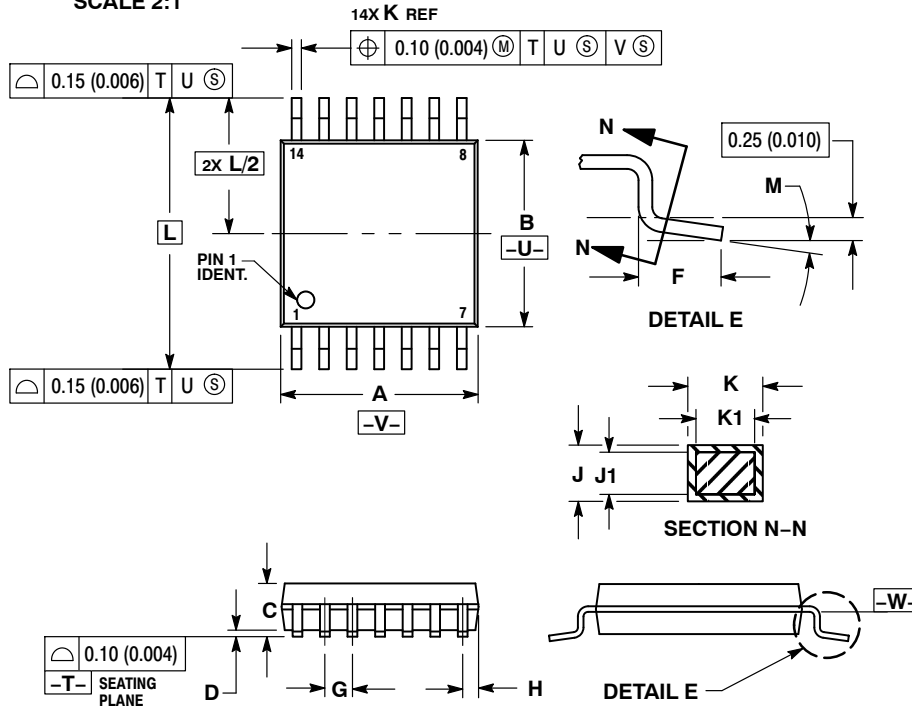
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SCALE 2:1

TSSOP-14 WB
CASE 948G
ISSUE C

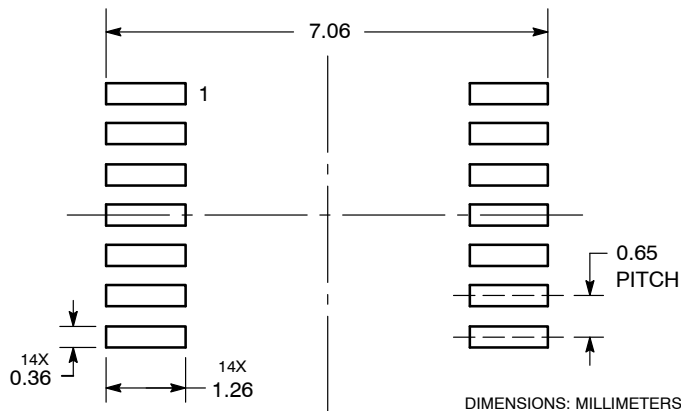
DATE 17 FEB 2016



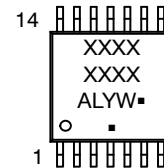
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

**RECOMMENDED
SOLDERING FOOTPRINT***


*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC
MARKING DIAGRAM***


A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION: TSSOP-14 WB

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