

MC74HC540A

Octal 3-State Inverting Buffer/Line Driver/Line Receiver

High-Performance Silicon-Gate CMOS

The MC74HC540A is identical in pinout to the LS540. The device inputs are compatible with Standard CMOS outputs. External pull-up resistors make them compatible with LSTTL outputs.

The HC540A is an octal inverting buffer/line driver/line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. This device features inputs and outputs on opposite sides of the package and two ANDed active-low output enables.

The HC540A is similar in function to the HC541A, which has noninverting outputs.

Features

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7 A Requirements
- Chip Complexity: 124 FETs or 31 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

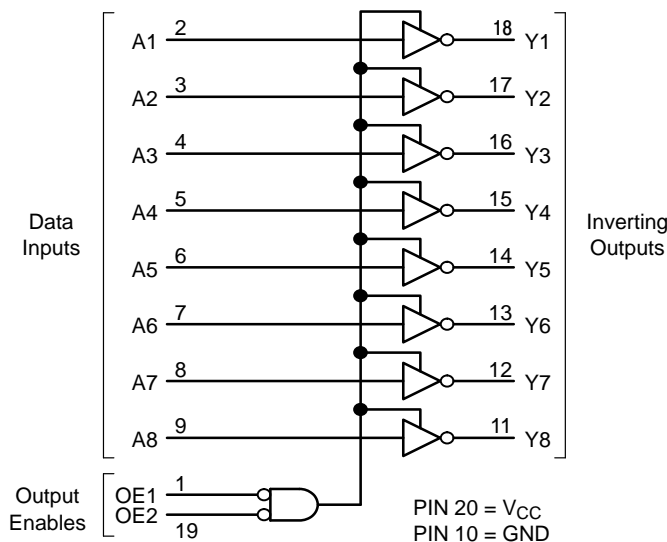
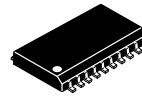


Figure 1. Logic Diagram



ON Semiconductor®

<http://onsemi.com>

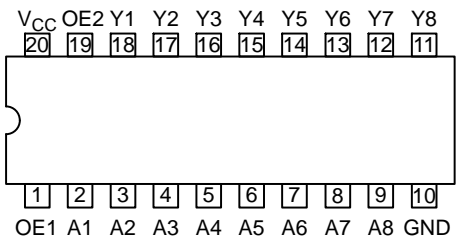


SOIC-20
DW SUFFIX
CASE 751D



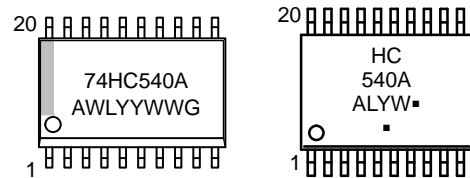
TSSOP-20
DT SUFFIX
CASE 948E

PIN ASSIGNMENT



20-Lead (Top View)

MARKING DIAGRAMS



SOIC-20

TSSOP-20

- A = Assembly Location
 - WL, L = Wafer Lot
 - YY, Y = Year
 - WW, W = Work Week
 - G or \blacksquare = Pb-Free Package
- (Note: Microdot may be in either location)

FUNCTION TABLE

| Inputs | | | Output Y |
|--------|-----|---|----------|
| OE1 | OE2 | A | |
| L | L | L | H |
| L | L | H | L |
| H | X | X | Z |
| X | H | X | Z |

Z = High Impedance

X = Don't Care

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MC74HC540A

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|----------------------|---|---|------------|
| V _{CC} | DC Supply Voltage | -0.5 to +7.0 | V |
| V _I | DC Input Voltage | -0.5 to V _{CC} + 0.5 | V |
| V _O | DC Output Voltage (Note 1) | -0.5 ≤ V _O ≤ V _{CC} + 0.5 | V |
| I _{IK} | DC Input Diode Current | ±20 | mA |
| I _{OK} | DC Output Diode Current | ±35 | mA |
| I _O | DC Output Sink Current | ±35 | mA |
| I _{CC} | DC Supply Current per Supply Pin | ±75 | mA |
| I _{GND} | DC Ground Current per Ground Pin | ±75 | mA |
| T _{STG} | Storage Temperature Range | -65 to +150 | °C |
| T _L | Lead Temperature, 1 mm from Case for 10 Seconds | 260 | °C |
| T _J | Junction Temperature Under Bias | +150 | °C |
| θ _{JA} | Thermal Resistance | SOIC TSSOP 96 128 | °C/W |
| P _D | Power Dissipation in Still Air at 85°C | SOIC TSSOP 500 450 | mW |
| MSL | Moisture Sensitivity | Level 1 | |
| F _R | Flammability Rating | Oxygen Index: 30% – 35% UL 94 V0 @ 0.125 in | |
| V _{ESD} | ESD Withstand Voltage | Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4) > 2000 > 200 > 1000 | V |
| I _{LATCHUP} | Latchup Performance | Above V _{CC} and Below GND at 85°C (Note 5) | ±300 mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|------------------------------------|--|--|--------------------|------|
| V _{CC} | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V |
| V _{in} , V _{out} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V _{CC} | V |
| T _A | Operating Temperature, All Package Types | -55 | +125 | °C |
| t _r , t _f | Input Rise and Fall Time (Figure 3) | V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V 0 0 0 | 1000 500 400 | ns |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. Unused inputs may not be left open. All inputs must be tied to a high- or low-logic input voltage level.

MC74HC540A

DC CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Condition | V _{CC} V | Guaranteed Limit | | | Unit |
|-----------------|--|---|----------------------|------------------|-------|--------|------|
| | | | | -55 to 25°C | ≤85°C | ≤125°C | |
| V _{IH} | Minimum High-Level Input Voltage | V _{out} = 0.1 V I _{out} ≤ 20 μA | 2.0 | 1.50 | 1.50 | 1.50 | V |
| | | | 3.0 | 2.10 | 2.10 | 2.10 | |
| | | | 4.5 | 3.15 | 3.15 | 3.15 | |
| | | | 6.0 | 4.20 | 4.20 | 4.20 | |
| V _{IL} | Maximum Low-Level Input Voltage | V _{out} = V _{CC} - 0.1 V I _{out} ≤ 20 μA | 2.0 | 0.50 | 0.50 | 0.50 | V |
| | | | 3.0 | 0.90 | 0.90 | 0.90 | |
| | | | 4.5 | 1.35 | 1.35 | 1.35 | |
| | | | 6.0 | 1.80 | 1.80 | 1.80 | |
| V _{OH} | Minimum High-Level Output Voltage | V _{in} = V _{IL} I _{out} ≤ 20 μA | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | 4.5 | 4.4 | 4.4 | 4.4 | |
| | | | 6.0 | 5.9 | 5.9 | 5.9 | |
| | | V _{in} = V _{IL} I _{out} ≤ 3.6 mA I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA | 3.0 | 2.48 | 2.34 | 2.20 | |
| | | | 4.5 | 3.98 | 3.84 | 3.70 | |
| | | | 6.0 | 5.48 | 5.34 | 5.20 | |
| V _{OL} | Maximum Low-Level Output Voltage | V _{in} = V _{IH} I _{out} ≤ 20 μA | 2.0 | 0.1 | 0.1 | 0.1 | V |
| | | | 4.5 | 0.1 | 0.1 | 0.1 | |
| | | | 6.0 | 0.1 | 0.1 | 0.1 | |
| | | V _{in} = V _{IH} I _{out} ≤ 3.6 mA I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA | 3.0 | 0.26 | 0.33 | 0.40 | |
| | | | 4.5 | 0.26 | 0.33 | 0.40 | |
| | | | 6.0 | 0.26 | 0.33 | 0.40 | |
| I _{in} | Maximum Input Leakage Current | V _{in} = V _{CC} or GND | 6.0 | ±0.1 | ±1.0 | ±1.0 | μA |
| I _{OZ} | Maximum Three-State Leakage Current | Output in High Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND | 6.0 | ±0.5 | ±5.0 | ±10.0 | μA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{in} = V _{CC} or GND I _{out} = 0 μA | 6.0 | 4 | 40 | 160 | μA |

AC CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

| Symbol | Parameter | V _{CC} V | Guaranteed Limit | | | Unit |
|--|---|--|------------------|-------|--------|------|
| | | | -55 to 25°C | ≤85°C | ≤125°C | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Input A to Output Y (Figures 2 and 4) | 2.0 | 80 | 100 | 120 | ns |
| | | 3.0 | 30 | 40 | 55 | |
| | | 4.5 | 18 | 23 | 28 | |
| | | 6.0 | 15 | 20 | 25 | |
| t _{PLZ} , t _{PHZ} | Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 5) | 2.0 | 110 | 140 | 165 | ns |
| | | 3.0 | 45 | 60 | 75 | |
| | | 4.5 | 25 | 31 | 38 | |
| | | 6.0 | 21 | 26 | 31 | |
| t _{PZL} , t _{PZH} | Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 5) | 2.0 | 110 | 140 | 165 | ns |
| | | 3.0 | 45 | 60 | 75 | |
| | | 4.5 | 25 | 31 | 38 | |
| | | 6.0 | 21 | 26 | 31 | |
| t _{TLH} , t _{THL} | Maximum Output Transition Time, Any Output (Figures 2 and 4) | 2.0 | 60 | 75 | 90 | ns |
| | | 3.0 | 22 | 28 | 34 | |
| | | 4.5 | 12 | 15 | 18 | |
| | | 6.0 | 10 | 13 | 15 | |
| C _{in} | Maximum Input Capacitance | | 10 | 10 | 10 | pF |
| C _{out} | Maximum 3-State Output Capacitance (Output in High Impedance State) | | 15 | 15 | 15 | pF |
| C _{PD} | Power Dissipation Capacitance (Per Buffer) (Note 7) | Typical @ 25°C, V _{CC} = 5.0 V, V _{EE} = 0 V | | | pF | |
| | | 35 | | | | |

7. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

MC74HC540A

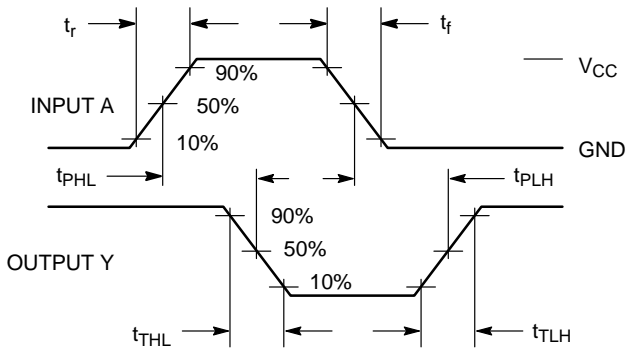


Figure 2. Switching Waveform

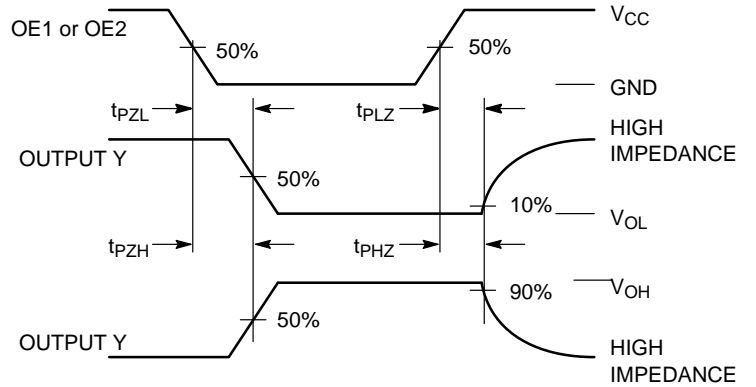
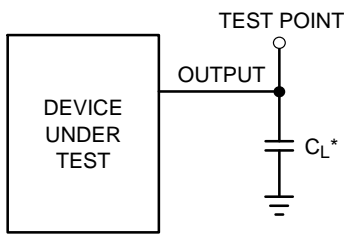
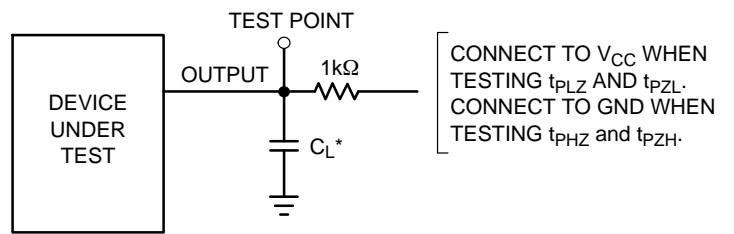


Figure 3. Switching Waveform



*Includes all probe and jig capacitance

Figure 4. Test Circuit



CONNECT TO VCC WHEN TESTING t_{pLZ} AND t_{pZL} .
CONNECT TO GND WHEN TESTING t_{pHZ} and t_{pZH} .

*Includes all probe and jig capacitance

Figure 5. Test Circuit

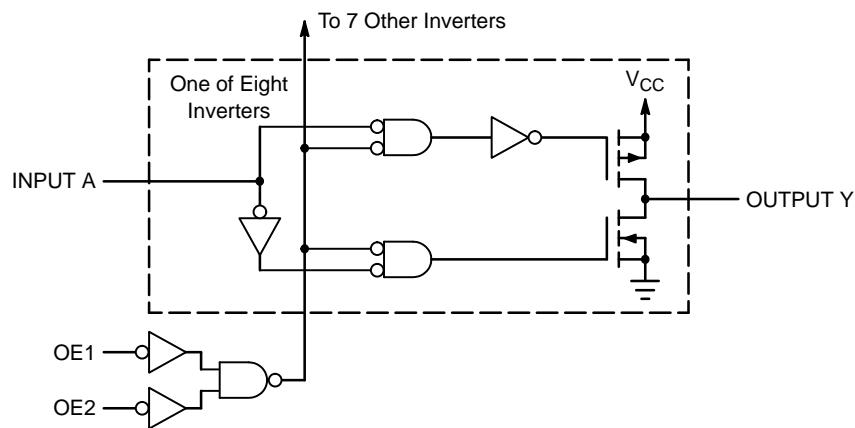


Figure 6. Logic Detail

MC74HC540A

PIN DESCRIPTIONS

INPUTS

A1, A2, A3, A4, A5, A6, A7, A8 (PINS 2, 3, 4, 5, 6, 7, 8, 9)

Data input pins. Data on these pins appear in inverted form on the corresponding Y outputs, when the outputs are enabled.

CONTROLS

OE1, OE2 (PINS 1, 19)

Output enables (active-low). When a low voltage is applied to both of these pins, the outputs are enabled and the

device functions as an inverter. When a high voltage is applied to either input, the outputs assume the high impedance state.

OUTPUTS

Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8 (PINS 18, 17, 16, 15, 14, 13, 12, 11)

Device outputs. Depending upon the state of the output enable pins, these outputs are either inverting outputs or high-impedance outputs.

ORDERING INFORMATION

| Device | Package | Shipping† |
|-------------------|---------------------------|------------------|
| MC74HC540ADWG | SOIC-20 WIDE (Pb-Free) | 38 Units / Rail |
| MC74HC540ADWR2G | SOIC-20 WIDE (Pb-Free) | 1000 Tape & Reel |
| MC74HC540ADTR2G | TSSOP-20 (Pb-Free) | 2500 Tape & Reel |
| NLV74HC540ADTR2G* | TSSOP-20 (Pb-Free) | 2500 Tape & Reel |

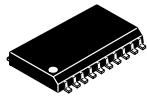
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

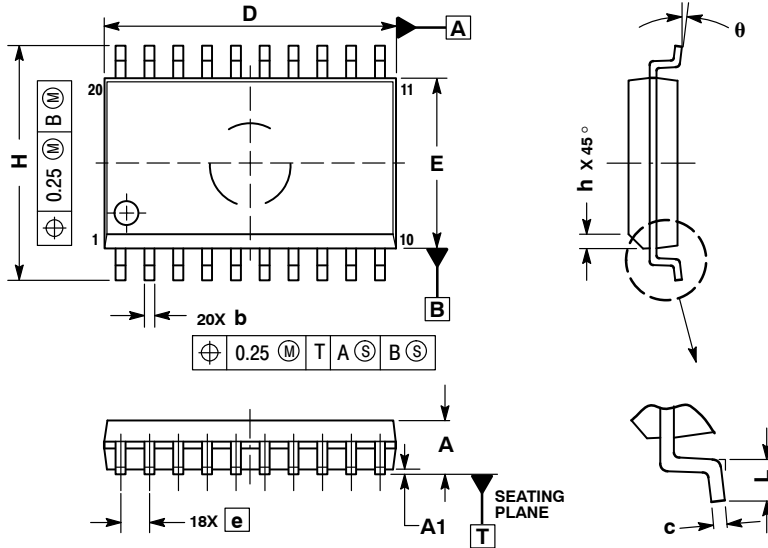
ON Semiconductor®



SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015

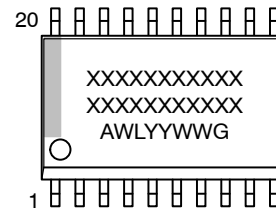


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

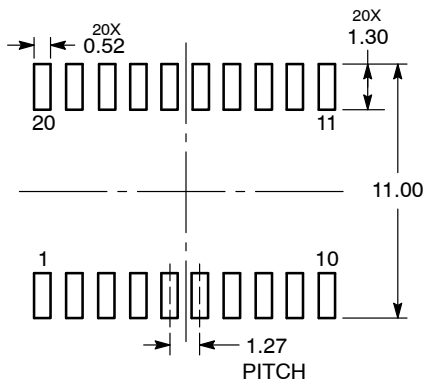
| DIM | MILLIMETERS | |
|-----|-------------|-------|
| | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| b | 0.35 | 0.49 |
| c | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

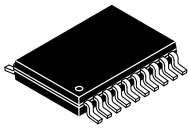
| | | |
|------------------|-------------|--|
| DOCUMENT NUMBER: | 98ASB42343B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | SOIC-20 WB | PAGE 1 OF 1 |

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

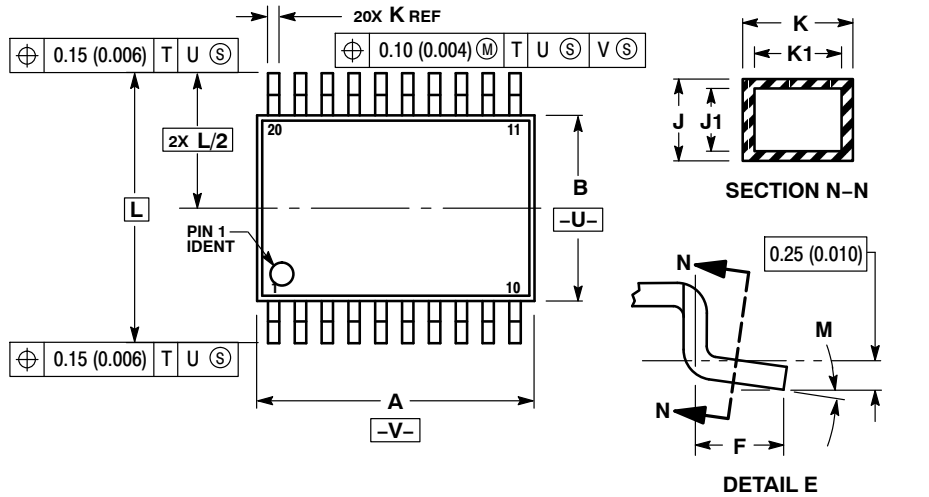
ON Semiconductor®



TSSOP-20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016

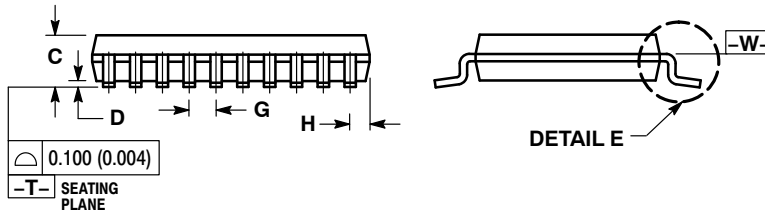
SCALE 2:1



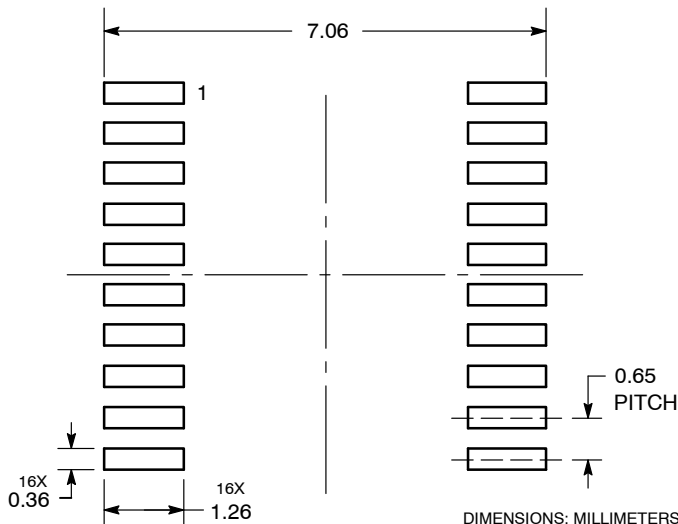
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

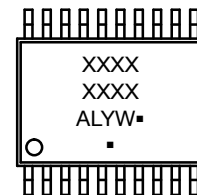
| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |



SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

| | | |
|------------------|-------------|--|
| DOCUMENT NUMBER: | 98ASH70169A | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | TSSOP-20 WB | PAGE 1 OF 1 |

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:
Voice Mail: 1 800-282-9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative