

# Dual Precision Monostable Multivibrator (Retriggerable, Resettable)

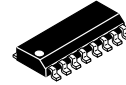
## MC74HC4538A

The MC74HC4538A is identical in pinout to the MC14538B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

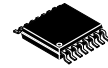
This dual monostable multivibrator may be triggered by either the positive or the negative edge of an input pulse, and produces a precision output pulse over a wide range of pulse widths. Because the device has conditioned trigger inputs, there are no trigger-input rise and fall time restrictions. The output pulse width is determined by the external timing components,  $R_x$  and  $C_x$ . The device has a reset function which forces the Q output low and the  $\bar{Q}$  output high, regardless of the state of the output pulse circuitry.

### Features

- Unlimited Rise and Fall Times Allowed on the Trigger Inputs
- Output Pulse is Independent of the Trigger Pulse Width
- $\pm 10\%$  Guaranteed Pulse Width Variation from Part to Part (Using the Same Test Jig)
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 3.0 to 6.0 V
- Low Input Current: 1.0  $\mu\text{A}$
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 145 FETs or 36 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

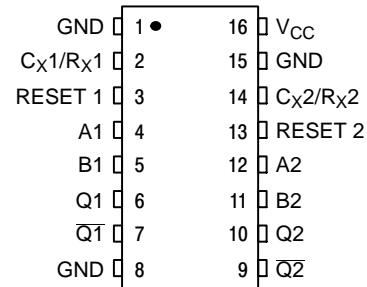


SOIC-16  
D SUFFIX  
CASE 751B

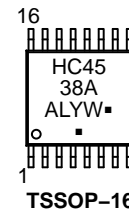
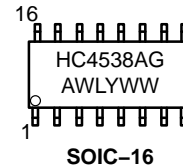


TSSOP-16  
DT SUFFIX  
CASE 948F

### PIN ASSIGNMENT



### MARKING DIAGRAMS



- A = Assembly Location
- L, WL = Wafer Lot
- Y, YY = Year
- W, WW = Work Week
- G or ■ = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 2.

# MC74HC4538A

## FUNCTION TABLE

| Inputs |      |      | Outputs       |               |
|--------|------|------|---------------|---------------|
| Reset  | A    | B    | Q             | $\bar{Q}$     |
| H      |      | H    |               |               |
| H      | L    |      |               |               |
| H      | X    | L    | Not Triggered | Not Triggered |
| H      | H    | X    | Not Triggered | Not Triggered |
| H      | L,H, | H    | Not Triggered | Not Triggered |
| H      | L    | L,H, | Not Triggered | Not Triggered |
| L      | X    | X    | L             | H             |
|        | X    | X    | Not Triggered | Not Triggered |

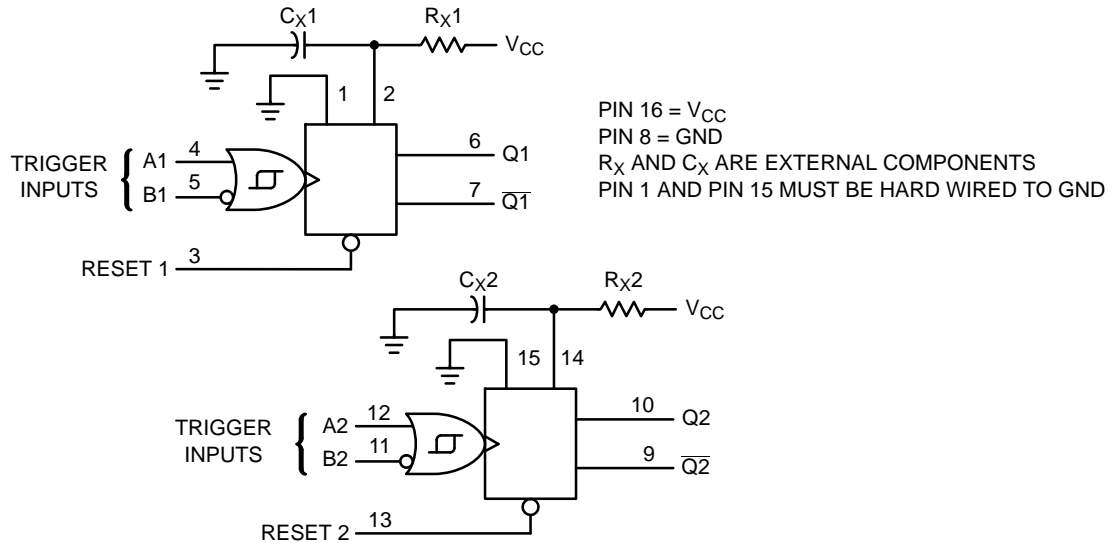


Figure 1. Logic Diagram

### ORDERING INFORMATION

| Device          | Package              | Shipping <sup>†</sup> |
|-----------------|----------------------|-----------------------|
| MC74HC4538ADR2G | SOIC-16<br>(Pb-Free) | 2500 / Tape & Reel    |

### DISCONTINUED (Note 1)

|                   |                       |                    |
|-------------------|-----------------------|--------------------|
| MC74HC4538ADG     | SOIC-16<br>(Pb-Free)  | 48 Units / Rail    |
| NLV74HC4538ADR2G* | SOIC-16<br>(Pb-Free)  | 2500 / Tape & Reel |
| MC74HC4538ADTR2G  | TSSOP-16<br>(Pb-Free) | 2500 / Tape & Reel |
| NLVHC4538ADTR2G*  | TSSOP-16<br>(Pb-Free) | 2500 / Tape & Reel |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

1. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on [www.onsemi.com](http://www.onsemi.com).

# MC74HC4538A

## MAXIMUM RATINGS

| Symbol               | Parameter   | Value   | Unit |
|----------------------|---|---|------|
| V <sub>CC</sub>      | DC Supply Voltage   | -0.5 to +7.0                                  | V    |
| V <sub>I</sub>       | DC Input Voltage  | -0.5 ≤ V <sub>I</sub> ≤ V <sub>CC</sub> + 0.5 | V    |
| V <sub>O</sub>       | DC Output Voltage (Note 2)  | -0.5 ≤ V <sub>O</sub> ≤ V <sub>CC</sub> + 0.5 | V    |
| I <sub>IK</sub>      | DC Input Diode Current<br>A, B, Reset<br>C <sub>X</sub> , R <sub>X</sub>                                      | ±20<br>±30                                    | mA   |
| I <sub>OK</sub>      | DC Output Diode Current   | ±25   | mA   |
| I <sub>O</sub>       | DC Output Sink Current  | ±25   | mA   |
| I <sub>CC</sub>      | DC Supply Current per Supply Pin  | ±100  | mA   |
| I <sub>GND</sub>     | DC Ground Current per Ground Pin  | ±100  | mA   |
| T <sub>STG</sub>     | Storage Temperature Range   | -65 to +150                                   | °C   |
| T <sub>L</sub>       | Lead temperature, 1 mm from Case for 10 Seconds   | 260   | °C   |
| T <sub>J</sub>       | Junction temperature under Bias   | +150  | °C   |
| θ <sub>JA</sub>      | Thermal resistance<br>SOIC<br>TSSOP   | 112<br>148                                    | °C/W |
| P <sub>D</sub>       | Power Dissipation in Still Air at 85°C<br>SOIC<br>TSSOP   | 500<br>450                                    | mW   |
| MSL                  | Moisture Sensitivity  | Level 1                                       |      |
| F <sub>R</sub>       | Flammability Rating<br>Oxygen Index: 30% – 35%  | UL-94-V0 (0.125 in)                           |      |
| V <sub>ESD</sub>     | ESD Withstand Voltage<br>Human Body Model (Note 3)<br>Machine Model (Note 4)<br>Charged Device Model (Note 5) | > 2000<br>> 100<br>> 500                      | V    |
| I <sub>Latchup</sub> | Latchup Performance<br>Above V <sub>CC</sub> and Below GND at 85°C (Note 6)                                   | ±300  | mA   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. I<sub>O</sub> absolute maximum rating must be observed.
3. Tested to EIA/JESD22-A114-A.
4. Tested to EIA/JESD22-A115-A.
5. Tested to JESD22-C101-A.
6. Tested to EIA/JESD78.

## RECOMMENDED OPERATING CONDITIONS

| Symbol                             | Parameter   | Min              | Max                            | Unit |
|------------------------------------|---|------------------|--------------------------------|------|
| V <sub>CC</sub>                    | DC Supply Voltage (Referenced to GND)   | 2.0              | 6.0                            | V    |
| V <sub>in</sub> , V <sub>out</sub> | DC Input Voltage, Output Voltage (Referenced to GND)  | 0                | V <sub>CC</sub>                | V    |
| T <sub>A</sub>                     | Operating Temperature, All Package Types  | -55              | +125                           | °C   |
| t <sub>r</sub> , t <sub>f</sub>    | Input Rise and Fall Time (Figure 6)<br>V <sub>CC</sub> = 2.0 V<br>V <sub>CC</sub> = 4.5 V<br>V <sub>CC</sub> = 6.0 V<br>A or B (Figure 4) | 0<br>0<br>0<br>- | 1000<br>500<br>400<br>No Limit | ns   |
| R <sub>x</sub>                     | External Timing Resistor<br>V <sub>CC</sub> < 4.5 V<br>V <sub>CC</sub> ≥ 4.5 V  | 1.0<br>2.0       | †<br>†                         | kΩ   |
| C <sub>x</sub>                     | External Timing Capacitor   | 0                | †                              | μF   |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

† The maximum allowable values of R<sub>x</sub> and C<sub>x</sub> are a function of the leakage of capacitor C<sub>x</sub>, the leakage of the HC4538A, and leakage due to board layout and surface resistance. For most applications, C<sub>x</sub>/R<sub>x</sub> should be limited to a maximum value of 10 μF/1.0 MΩ. Values of C<sub>x</sub> > 1.0 μF may cause a problem during power down (see Power Down Considerations). Susceptibility to externally induced noise signals may occur for R<sub>x</sub> > 1.0 MΩ.

7. Unused inputs may not be left open. All inputs must be tied to a high-logic voltage level or a low-logic input voltage level.

# MC74HC4538A

## DC CHARACTERISTICS

| Symbol          | Parameter  | Test Conditions  | V <sub>CC</sub><br>V   | Guaranteed Limits |      |      |               |      |      |                |     |      | Unit |
|-----------------|--|--|--|-------------------|------|------|---------------|------|------|----------------|-----|------|------|
|                 |  |  |  | -55 to 25°C       |      |      | ≤ 85°C        |      |      | ≤ 125°C        |     |      |      |
|                 |  |  |  | Min               | Typ  | Max  | Min           | Typ  | Max  | Min            | Typ | Max  |      |
| V <sub>IH</sub> | Minimum High-Level Input Voltage                                 | V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V<br> I <sub>out</sub>   ≤ 20 μA   | 2.0  | 1.5               |      |      | 1.5           |      |      | 1.5            |     |      | V    |
|                 |  |  | 4.5  | 3.15              |      | 3.15 |               |      | 3.15 |                |     |      |      |
|                 |  |  | 6.0  | 4.2               |      | 4.2  |               |      | 4.2  |                |     |      |      |
| V <sub>IL</sub> | Maximum Low-Level Input Voltage                                  | V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V<br> I <sub>out</sub>   ≤ 20 μA   | 2.0  |                   |      | 0.5  |               |      | 0.5  |                |     | 0.5  | V    |
|                 |  |  | 4.5  |                   |      | 1.35 |               |      | 1.35 |                |     | 1.35 |      |
|                 |  |  | 6.0  |                   |      | 1.8  |               |      | 1.8  |                |     | 1.8  |      |
| V <sub>OH</sub> | Minimum High-Level Output Voltage                                | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 μA  | 2.0  | 1.9               |      |      | 1.9           |      |      | 1.9            |     |      | V    |
|                 |  |  | 4.5  | 4.4               |      |      | 4.4           |      |      | 4.4            |     |      |      |
|                 |  | 6.0  | 5.9  |                   |      | 5.9  |               |      | 5.9  |                |     |      |      |
|                 |  | 4.5  | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ -4.0 mA<br> I <sub>out</sub>   ≤ -5.2 mA | 3.98              |      |      | 3.84          |      |      | 3.7            |     |      |      |
| 6.0             | 5.48   |  |  |                   |      | 5.34 |               |      | 5.2  |                |     |      |      |
| V <sub>OL</sub> | Maximum Low-Level Output Voltage                                 | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 μA  | 2.0  |                   |      | 0.1  |               |      | 0.1  |                |     | 0.1  | V    |
|                 |  |  | 4.5  |                   |      | 0.1  |               |      | 0.1  |                |     | 0.1  |      |
|                 |  | 6.0  |  |                   | 0.1  |      |               | 0.1  |      |                | 0.1 |      |      |
|                 |  | 4.5  | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 4.0 mA<br> I <sub>out</sub>   ≤ 5.2 mA   |                   |      |      | 0.26          |      |      | 0.33           |     |      |      |
| 6.0             |  |  |  |                   | 0.26 |      |               | 0.33 |      |                | 0.4 |      |      |
| I <sub>in</sub> | Maximum Input Leakage Current (A, B, Reset)                      | V <sub>in</sub> = V <sub>CC</sub> or GND   | 6.0  |                   |      | ±0.1 |               |      | ±1.0 |                |     | ±1.0 | μA   |
| I <sub>in</sub> | Maximum Input Leakage Current (R <sub>x</sub> , C <sub>x</sub> ) | V <sub>in</sub> = V <sub>CC</sub> or GND   | 6.0  |                   |      | ±50  |               |      | ±500 |                |     | ±500 | nA   |
| I <sub>CC</sub> | Maximum Quiescent Supply Current (per package) Standby State     | V <sub>in</sub> = V <sub>CC</sub> or GND<br>Q1 and Q2 = Low<br>I <sub>out</sub> = 0 μA   | 6.0  |                   |      | 130  |               |      | 220  |                |     | 350  | μA   |
| I <sub>CC</sub> | Maximum Supply Current (per package) Active State                | V <sub>in</sub> = V <sub>CC</sub> or GND<br>Q1 and Q2 = High<br>I <sub>out</sub> = 0 μA<br>Pins 2 and 14 = 0.5 V <sub>CC</sub> | 6.0  | 25°C              |      |      | -45°C to 85°C |      |      | -55°C to 125°C |     |      | μA   |
|                 |  |  |  |                   | 400  |      |               | 600  |      |                |     | 800  |      |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# MC74HC4538A

## AC CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6.0 ns)

| Symbol                                 | Parameter   | V <sub>CC</sub><br>V | Guaranteed Limits |          |        |          |         |          | Unit |
|--|---|----------------------|-------------------|----------|--------|----------|---------|----------|------|
|  |   |                      | -55 to 25°C       |          | ≤ 85°C |          | ≤ 125°C |          |      |
|  |   |                      | Min               | Max      | Min    | Max      | Min     | Max      |      |
| t <sub>PLH</sub>                       | Maximum Propagation Delay<br>Input A or B to Q<br>(Figures 5 and 7)           | 2.0                  |                   | 175      |        | 220      |         | 265      | ns   |
|  |   | 4.5                  |                   | 35       |        | 44       |         | 53       |      |
|  |   | 6.0                  |                   | 30       |        | 37       |         | 45       |      |
| t <sub>PHL</sub>                       | Maximum Propagation Delay<br>Input A or B to NQ<br>(Figures 5 and 7)          | 2.0                  |                   | 195      |        | 245      |         | 295      | ns   |
|  |   | 4.5                  |                   | 39       |        | 49       |         | 59       |      |
|  |   | 6.0                  |                   | 33       |        | 42       |         | 50       |      |
| t <sub>PHL</sub>                       | Maximum Propagation Delay<br>Reset to Q<br>(Figures 6 and 7)                  | 2.0                  |                   | 175      |        | 220      |         | 265      | ns   |
|  |   | 4.5                  |                   | 35       |        | 44       |         | 53       |      |
|  |   | 6.0                  |                   | 30       |        | 37       |         | 45       |      |
| t <sub>PLH</sub>                       | Maximum Propagation Delay<br>Reset to NQ<br>(Figures 6 and 7)                 | 2.0                  |                   | 175      |        | 220      |         | 265      | ns   |
|  |   | 4.5                  |                   | 35       |        | 44       |         | 53       |      |
|  |   | 6.0                  |                   | 30       |        | 37       |         | 45       |      |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Maximum Output Transition Time, Any Output<br>(Figures 6 and 7)               | 2.0                  |                   | 75       |        | 95       |         | 110      | ns   |
|  |   | 4.5                  |                   | 15       |        | 19       |         | 22       |      |
|  |   | 6.0                  |                   | 13       |        | 16       |         | 19       |      |
| C <sub>in</sub>                        | Maximum Input Capacitance (A, B, Reset)<br>(C <sub>x</sub> , R <sub>x</sub> ) | -                    |                   | 10<br>25 |        | 10<br>25 |         | 10<br>25 | pF   |

| C <sub>PD</sub> | Power Dissipation Capacitance (per Multivibrator)* | Typical @ 25°C, V <sub>CC</sub> = 5.0 V |  | pF |
|-----------------|--|---|--|----|
|                 |  | 150                                     |  |    |
|                 |  |   |  |    |

\*Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>.

## TIMING CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 6.0 ns)

| Symbol                          | Parameter   | V <sub>CC</sub><br>V | Guaranteed Limits |      |        |      |         |      | Unit |
|---------------------------------|---|----------------------|-------------------|------|--------|------|---------|------|------|
|                                 |   |                      | -55 to 25°C       |      | ≤ 85°C |      | ≤ 125°C |      |      |
|                                 |   |                      | Min               | Max  | Min    | Max  | Min     | Max  |      |
| t <sub>rr</sub>                 | Minimum Retrigger Time, Input A or B<br>(Figure 6) (Note 8) | 2.0                  | -                 |      | -      |      |         |      | ns   |
|                                 |   | 4.5                  | -                 |      | -      |      |         |      |      |
|                                 |   | 6.0                  | -                 |      | -      |      |         |      |      |
| t <sub>rec</sub>                | Minimum Recovery Time, Inactive to A or B<br>(Figure 6)     | 2.0                  | 0                 |      | 0      |      | 0       |      | ns   |
|                                 |   | 4.5                  | 0                 |      | 0      |      | 0       |      |      |
|                                 |   | 6.0                  | 0                 |      | 0      |      | 0       |      |      |
| t <sub>w</sub>                  | Minimum Pulse Width, Input A or B<br>(Figure 5)             | 2.0                  | 60                |      | 75     |      | 90      |      | ns   |
|                                 |   | 4.5                  | 12                |      | 15     |      | 18      |      |      |
|                                 |   | 6.0                  | 10                |      | 13     |      | 15      |      |      |
| t <sub>w</sub>                  | Minimum Pulse Width, Reset<br>(Figure 6)                    | 2.0                  | 60                |      | 75     |      | 90      |      | ns   |
|                                 |   | 4.5                  | 12                |      | 15     |      | 18      |      |      |
|                                 |   | 6.0                  | 10                |      | 13     |      | 15      |      |      |
| t <sub>r</sub> , t <sub>f</sub> | Maximum Input Rise and Fall Times, Reset<br>(Figure 6)      | 2.0                  |                   | 1000 |        | 1000 |         | 1000 | ns   |
|                                 |   | 4.5                  |                   | 500  |        | 500  |         | 500  |      |
|                                 |   | 6.0                  |                   | 400  |        | 400  |         | 400  |      |
|                                 | A or B<br>(Figure 6)  | 2.0                  | No Limit          |      |        |      |         |      |      |
|                                 |   | 4.5                  |                   |      |        |      |         |      |      |
|                                 |   | 6.0                  |                   |      |        |      |         |      |      |

8. 
$$t_{rr}(\text{ns}) = \frac{V_{CC} (\text{volts}) \times C_x (\text{pF})}{30.5}$$

# MC74HC4538A

## OUTPUT PULSE WIDTH CHARACTERISTICS ( $R_x = 10\text{ k}\Omega$ , $C_x = 0.1\text{ }\mu\text{F}$ , $C_L = 50\text{ pF}$ )

| Symbol | Parameter   | Conditions  |               | Guaranteed Limits |      |        |     |         |      | Unit |
|--------|---|---|---------------|-------------------|------|--------|-----|---------|------|------|
|        |   | Timing Components   | $V_{CC}$<br>V | -55 to 25°C       |      | ≤ 85°C |     | ≤ 125°C |      |      |
|        |   |   |               | Min               | Max  | Min    | Max | Min     | Max  |      |
| $\tau$ | Output Pulse Width (Note 9)<br>(Figures 5 and 6)          | $R_x = 10\text{ k}\Omega$ ,<br>$C_x = 0.1\text{ }\mu\text{F}$ | 5.0           | 0.63              | 0.77 | 0.6    | 0.8 | 0.59    | 0.81 | ms   |
|        | Pulse Width Match Between<br>Circuits in the same Package |   |               | ±5.0              |      |        |     |         |      | %    |
|        | Pulse Width Match Variation<br>(Part to Part) (Note 11)   |   |               | ±10               |      |        |     |         |      | %    |

## OUTPUT PULSE WIDTH CHARACTERISTICS ( $R_x = 100\text{ k}\Omega$ , $C_x = 1\text{ nF}$ , $C_L = 50\text{ pF}$ )

| Symbol | Parameter   | Conditions  |               |                     | Guaranteed Limits |       |      | Unit                         |
|--------|---|---|---------------|---------------------|-------------------|-------|------|------------------------------|
|        |   | Timing Components                                   | $V_{CC}$<br>V | Ambient Temperature | Min               | Typ   | Max  |                              |
| $\tau$ | Output Pulse Width (Note 10)                              | $R_x = 100\text{ k}\Omega$ ,<br>$C_x = 1\text{ nF}$ | 5.0           | 25°C                | -                 | 79    | -    | $\mu\text{s}$                |
|        | Pulse Width Match Between Circuits in the<br>same Package |   |               | -55 to 125°C        | -5.0              | -     | +5.0 | %                            |
|        | Pulse Width Match Variation (Part to Part)<br>(Note 11)   |   |               | -55 to 125°C        | -10               | -     | +10  | %                            |
| -      | Temperature Variance                                      |   |               | -55 to 125°C        | -                 | +0.05 | -    | $\mu\text{s}/^\circ\text{C}$ |
| -      | Power Supply Variance                                     |   |               | -55 to 125°C        | -                 | -8.0  | -    | $\mu\text{s}/V$              |

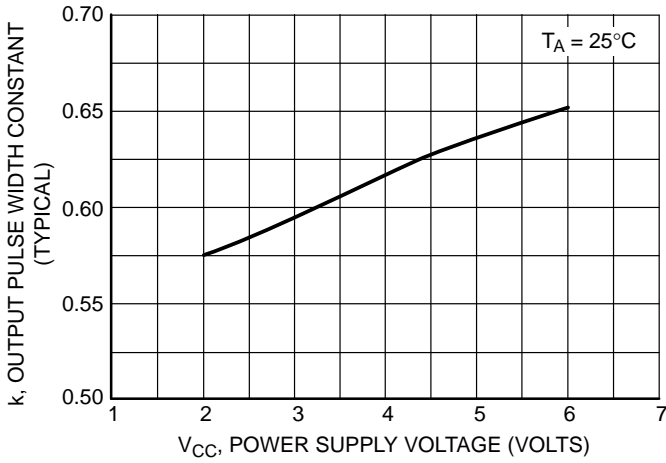
9.  $\tau = kR_xC_x$  and  $k = 0.7$  for the output pulse width corresponding to  $R_x = 10\text{ k}\Omega$ ,  $C_x = 0.1\text{ }\mu\text{F}$ .

10.  $\tau = kR_xC_x$  and  $k = 0.79$  for the output pulse width corresponding to  $R_x = 100\text{ k}\Omega$ ,  $C_x = 1\text{ nF}$ .

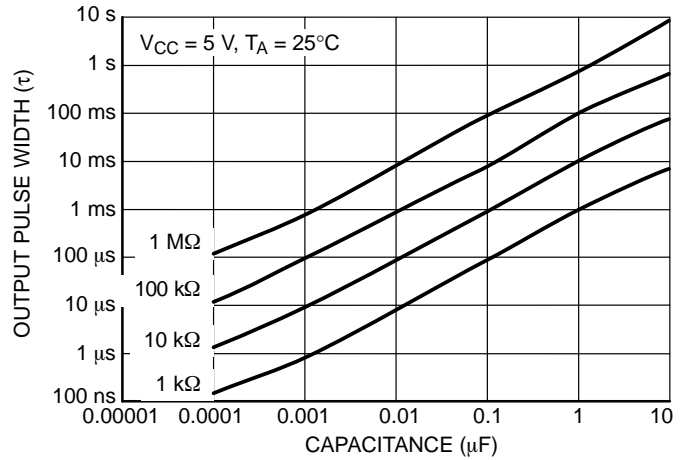
11. Pulse width match variation between ICs (part-to-part) is defined with identical  $R_x$ ,  $C_x$ ,  $V_{CC}$  and a specific temperature.

# MC74HC4538A

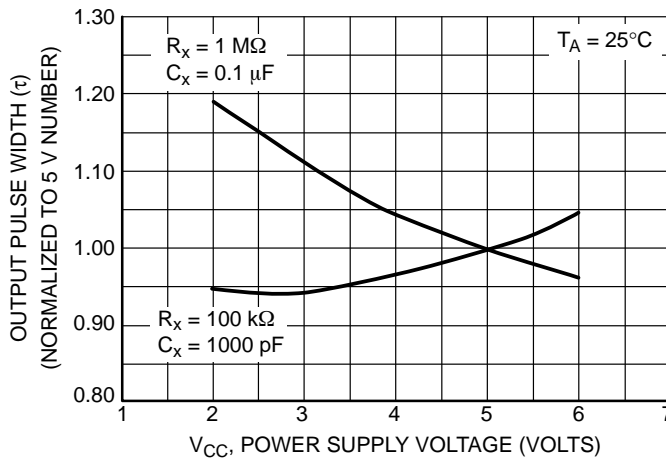
## TYPICAL CHARACTERISTICS



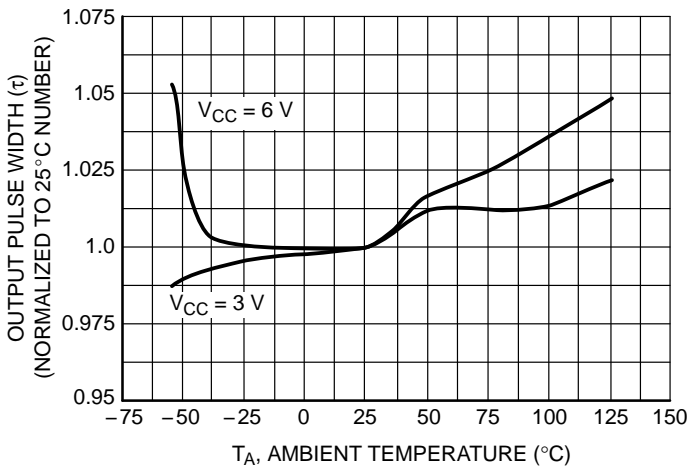
**Figure 2. Typical Output Pulse Width Constant,  $k$ , versus Supply Voltage**  
(For output pulse widths  $> 100 \mu\text{s}$ :  $\tau = kR_xC_x$ )



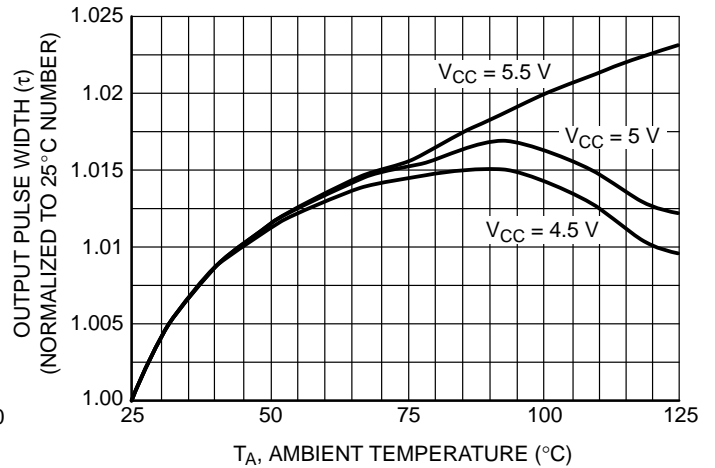
**Figure 3. Output Pulse Width versus Timing Capacitance**



**Figure 4. Normalized Output Pulse Width versus Power Supply Voltage**



**Figure 5. Normalized Output Pulse Width versus Power Supply Voltage**



**Figure 6. Normalized Output Pulse Width versus Power Supply Voltage**

# MC74HC4538A

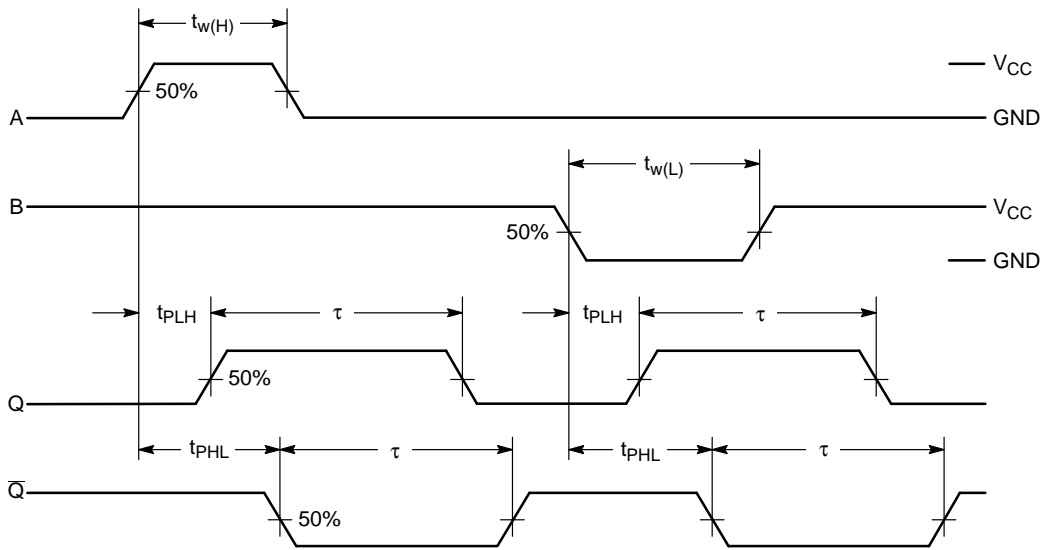


Figure 7. Switching Waveform

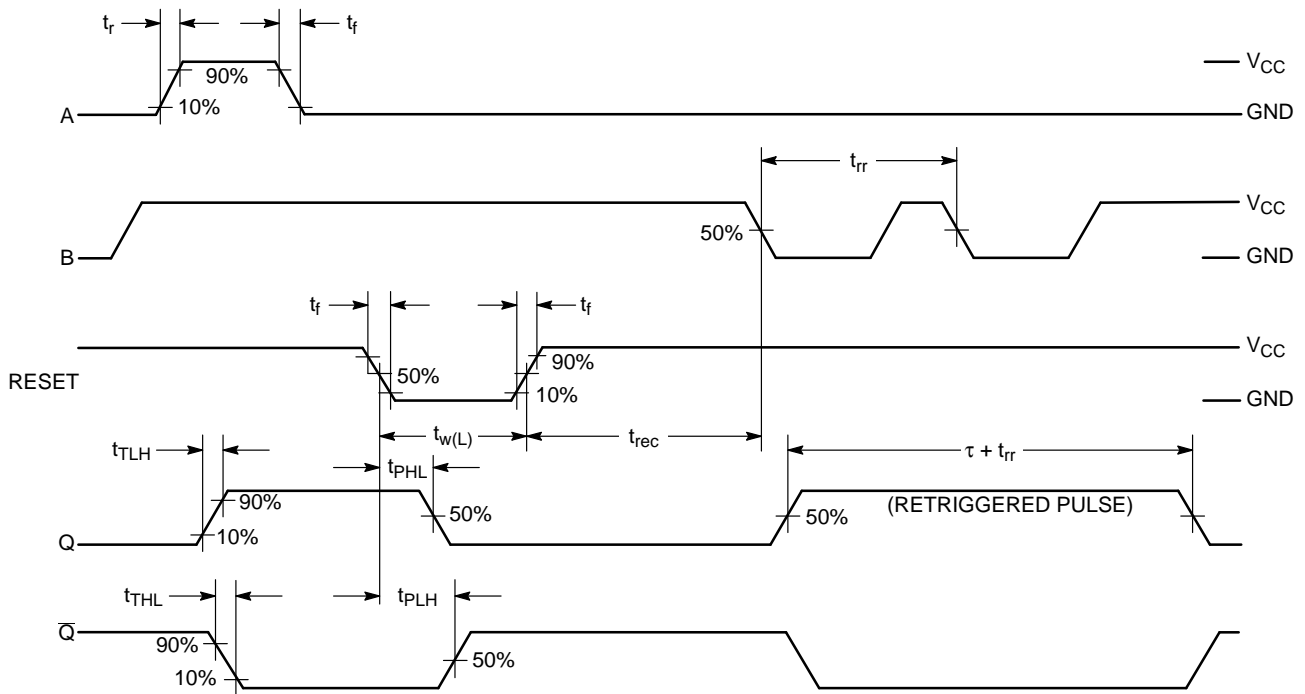
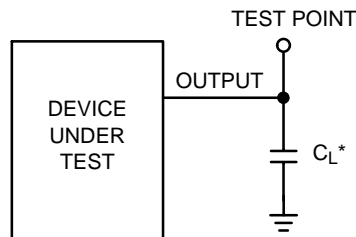


Figure 8. Switching Waveform



\*Includes all probe and jig capacitance

Figure 9. Test Circuit



# MC74HC4538A

## PIN DESCRIPTIONS

### INPUTS

#### A1, A2 (Pins 4, 12)

Positive-edge trigger inputs. A rising-edge signal on either of these pins triggers the corresponding multivibrator when there is a high level on the B1 or B2 input.

#### B1, B2 (Pins 5, 11)

Negative-edge trigger inputs. A falling-edge signal on either of these pins triggers the corresponding multivibrator when there is a low level on the A1 or A2 input.

#### Reset 1, Reset 2 (Pins 3, 13)

Reset inputs (active low). When a low level is applied to one of these pins, the Q output of the corresponding multivibrator is reset to a low level and the  $\bar{Q}$  output is set to a high level.

#### C<sub>X1</sub>/R<sub>X1</sub> and C<sub>X2</sub>/R<sub>X2</sub> (Pins 2 and 14)

External timing components. These pins are tied to the common points of the external timing resistors and

capacitors (see the Block Diagram). Polystyrene capacitors are recommended for optimum pulse width control. Electrolytic capacitors are not recommended due to high leakages associated with these type capacitors.

#### GND (Pins 1 and 15)

External ground. The external timing capacitors discharge to ground through these pins.

### OUTPUTS

#### Q1, Q2 (Pins 6, 10)

Noninverted monostable outputs. These pins (normally low) pulse high when the multivibrator is triggered at either the A or the B input. The width of the pulse is determined by the external timing components, R<sub>X</sub> and C<sub>X</sub>.

#### $\bar{Q}1, \bar{Q}2$ (Pins 7, 9)

Inverted monostable outputs. These pins (normally high) pulse low when the multivibrator is triggered at either the A or the B input. These outputs are the inverse of Q1 and Q2.

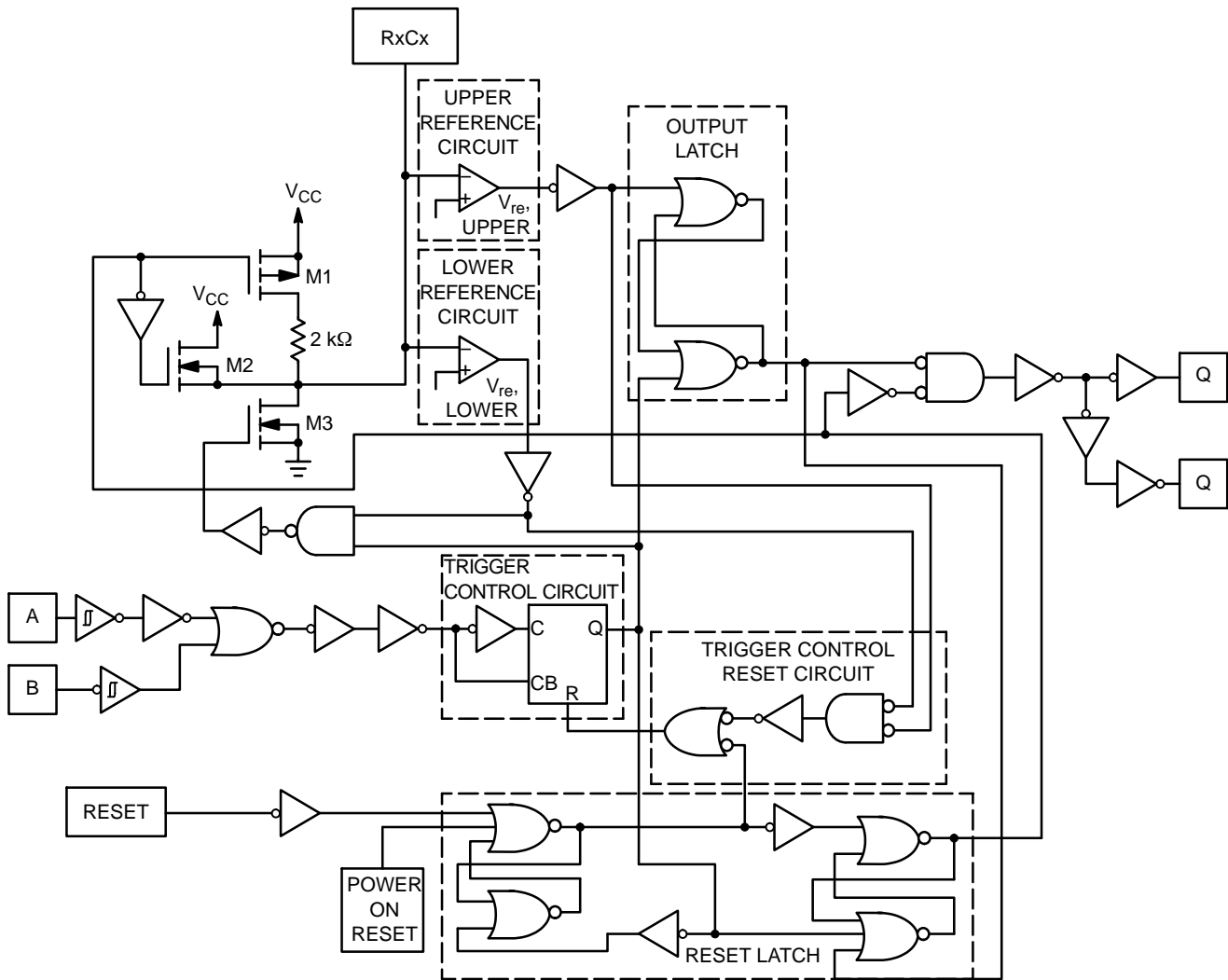


Figure 10. Logic Detail (1/2 the Device)

CIRCUIT OPERATION

Figure 11 shows the HC4538A configured in the retriggerable mode. Briefly, the device operates as follows (refer to Figure 10): In the quiescent state, the external timing capacitor,  $C_x$ , is charged to  $V_{CC}$ . When a trigger occurs, the Q output goes high and  $C_x$  discharges quickly to the lower reference voltage ( $V_{ref\ Lower} \approx 1/3 V_{CC}$ ).  $C_x$  then charges, through  $R_x$ , back up to the upper reference voltage ( $V_{ref\ Upper} \approx 2/3 V_{CC}$ ), at which point the one-shot has timed out and the Q output goes low.

The following, more detailed description of the circuit operation refers to both the logic detail (Figure 10) and the timing diagram (Figure 11).

QUIESCENT STATE

In the quiescent state, before an input trigger appears, the output latch is high and the reset latch is high (#1 in Figure 11). Thus the Q output (pin 6 or 10) of the monostable multivibrator is low (#2, Figure 11).

The output of the trigger-control circuit is low (#3), and transistors M1, M2, and M3 are turned off. The external timing capacitor,  $C_x$ , is charged to  $V_{CC}$  (#4), and both the upper and lower reference circuit has a low output (#5).

In addition, the output of the trigger-control reset circuit is low.

TRIGGER OPERATION

The HC4538A is triggered by either a rising-edge signal at input A (#7) or a falling-edge signal at input B (#8), with the unused trigger input and the Reset input held at the voltage levels shown in the Function Table. Either trigger signal will cause the output of the trigger-control circuit to go high (#9).

The trigger-control circuit going high simultaneously initiates two events. First, the output latch goes low, thus taking the Q output of the HC4538A to a high state (#10). Second, transistor M3 is turned on, which allows the external timing capacitor,  $C_x$ , to rapidly discharge toward ground (#11). (Note that the voltage across  $C_x$  appears at the input of both the upper and lower reference circuit comparator).

When  $C_x$  discharges to the reference voltage of the lower reference circuit (#12), the outputs of both reference circuits will be high (#13). The trigger-control reset circuit goes high, resetting the trigger-control circuit flip-flop to a low state (#14). This turns transistor M3 off again, allowing  $C_x$  to begin to charge back up toward  $V_{CC}$ , with a time constant  $t = R_x C_x$  (#15). Once the voltage across  $C_x$  charges to above the lower reference voltage, the lower reference circuit will go low allowing the monostable multivibrator to be retriggered.

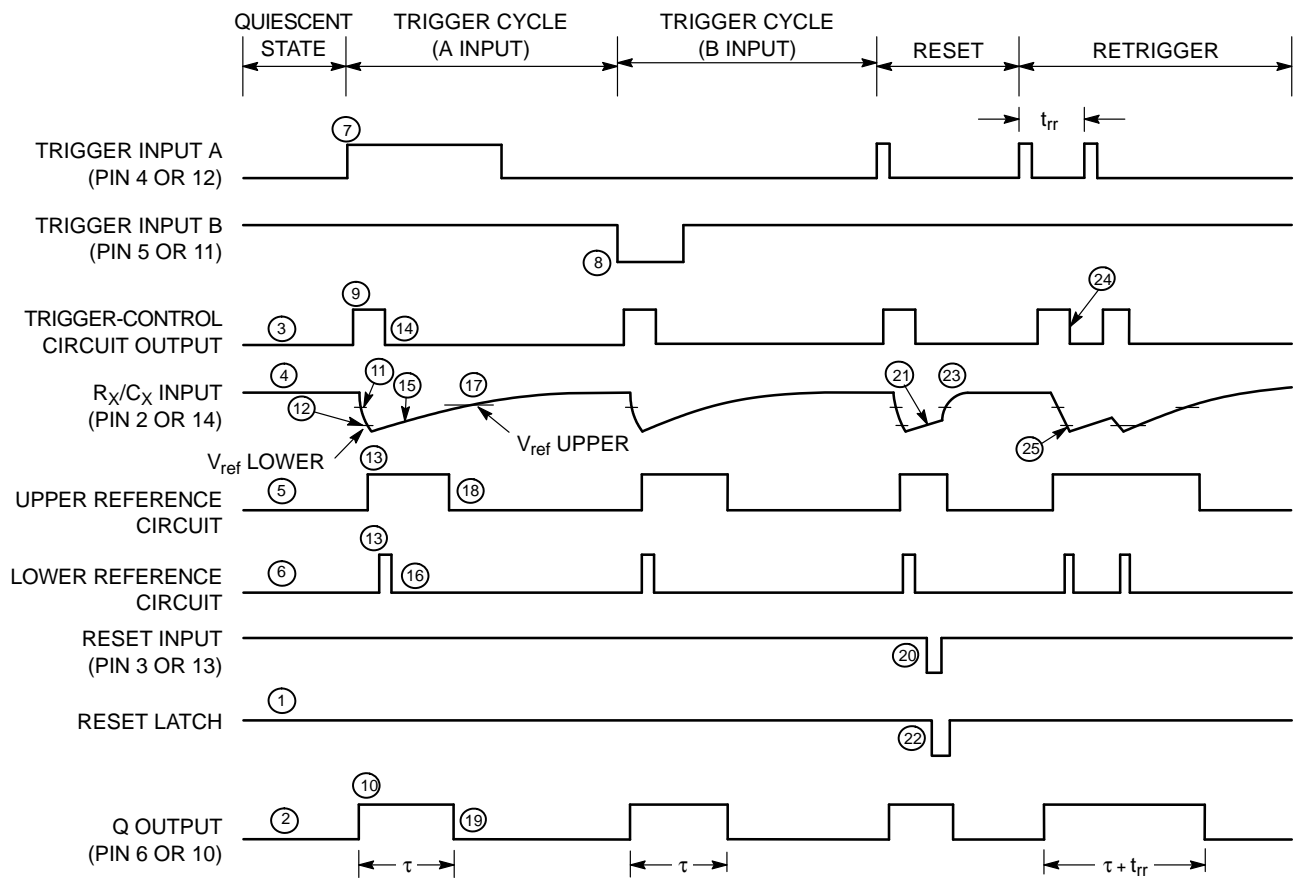


Figure 11. Timing Diagram

## MC74HC4538A

When  $C_x$  charges up to the reference voltage of the upper reference circuit (#17), the output of the upper reference circuit goes low (#18). This causes the output latch to toggle, taking the Q output of the HC4538A to a low state (#19), and completing the time-out cycle.

### POWER-DOWN CONSIDERATIONS

Large values of  $C_x$  may cause problems when powering down the HC4538A because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge from  $V_{CC}$  through the input protection diodes at pin 2 or pin 14. Current through the protection diodes must be limited to 30 mA; therefore, the turn-off time of the  $V_{CC}$  power supply must not be faster than  $t = V_{CC} \bullet C_x / (30 \text{ mA})$ . For example, if  $V_{CC} = 5.0 \text{ V}$  and  $C_x = 15 \mu\text{F}$ , the  $V_{CC}$  supply must turn off no faster than  $t = (5.0 \text{ V}) \bullet (15 \mu\text{F}) / 30 \text{ mA} = 2.5 \text{ ms}$ . This is usually not a problem because power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of  $V_{CC}$  to zero volts occurs, the HC4538A may sustain damage. To avoid this possibility, use an external damping diode,  $D_x$ , connected as shown in Figure 12. Best results can be achieved if diode  $D_x$  is chosen to be a germanium or Schottky type diode able to withstand large current surges.

### RESET AND POWER ON RESET OPERATION

A low voltage applied to the Reset pin always forces the Q output of the HC4538A to a low state.

The timing diagram illustrates the case in which reset occurs (#20) while  $C_x$  is charging up toward the reference voltage of the upper reference circuit (#21). When a reset

occurs, the output of the reset latch goes low (#22), turning on transistor M1. Thus  $C_x$  is allowed to quickly charge up to  $V_{CC}$  (#23) to await the next trigger signal.

On power up of the HC4538A the power-on reset circuit will be high causing a reset condition. This will prevent the trigger-control circuit from accepting a trigger input during this state. The HC4538A's Q outputs are low and the  $\bar{Q}$  not outputs are high.

### RETRIGGER OPERATION

When used in the retriggerable mode (Figure 13), the HC4538A may be retriggered during timing out of the output pulse at any time after the trigger-control circuit flip-flop has been reset (#24), and the voltage across  $C_x$  is above the lower reference voltage. As long as the  $C_x$  voltage is below the lower reference voltage, the reset of the flip-flop is high, disabling any trigger pulse. This prevents M3 from turning on during this period resulting in an output pulse width that is predictable.

The amount of undershoot voltage on  $R_x C_x$  during the trigger mode is a function of loop delay, M3 conductivity, and  $V_{DD}$ . Minimum retrigger time,  $t_{rr}$  (Figure 7), is a function of 1) time to discharge  $R_x C_x$  from  $V_{DD}$  to lower reference voltage ( $T_{\text{discharge}}$ ); 2) loop delay ( $T_{\text{delay}}$ ); 3) time to charge  $R_x C_x$  from the undershoot voltage back to the lower reference voltage ( $T_{\text{charge}}$ ).

Figure 14 shows the device configured in the non-retriggerable mode.

For additional information, please see Application Note (AN1558/D) titled *Characterization of Retrigger Time in the HC4538A Dual Precision Monostable Multivibrator*.

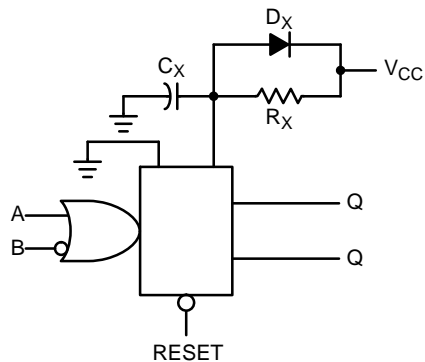


Figure 12. Discharge Protection During Power Down

# MC74HC4538A

## TYPICAL APPLICATIONS

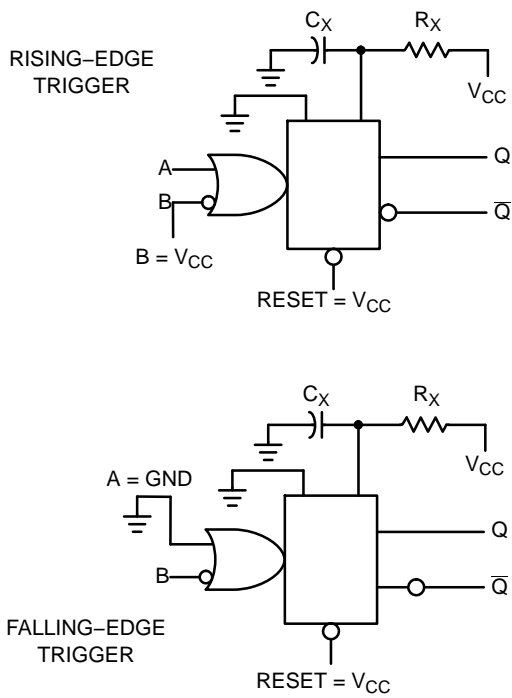


Figure 13. Retriggerable Monostable Circuitry

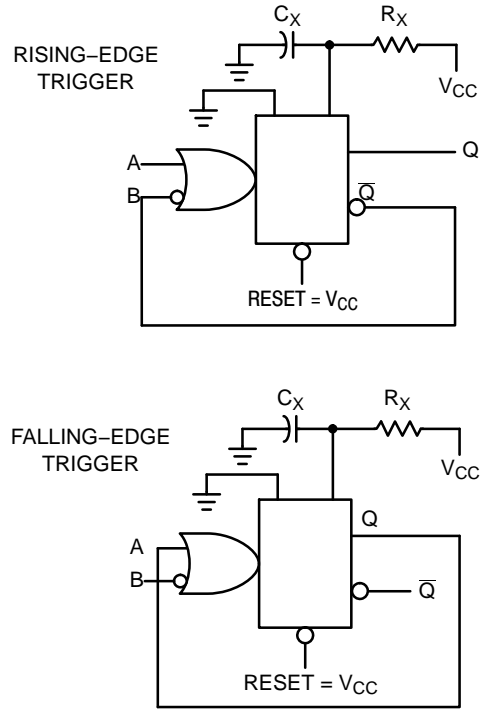


Figure 14. Non-retriggerable Monostable Circuitry

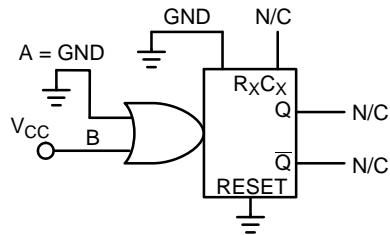
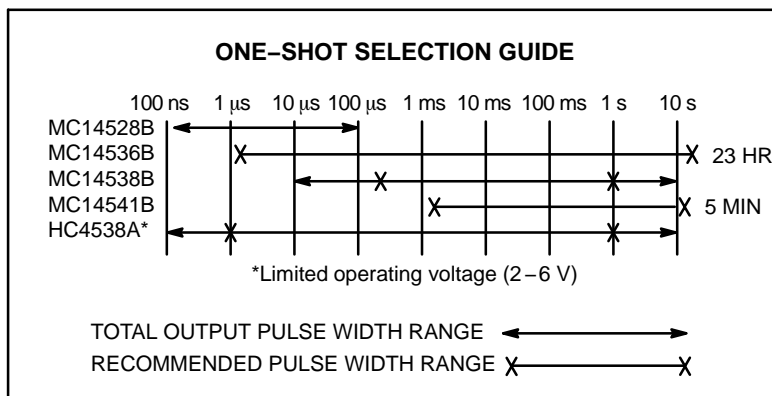
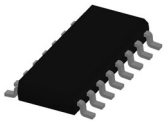


Figure 15. Connection of Unused Section



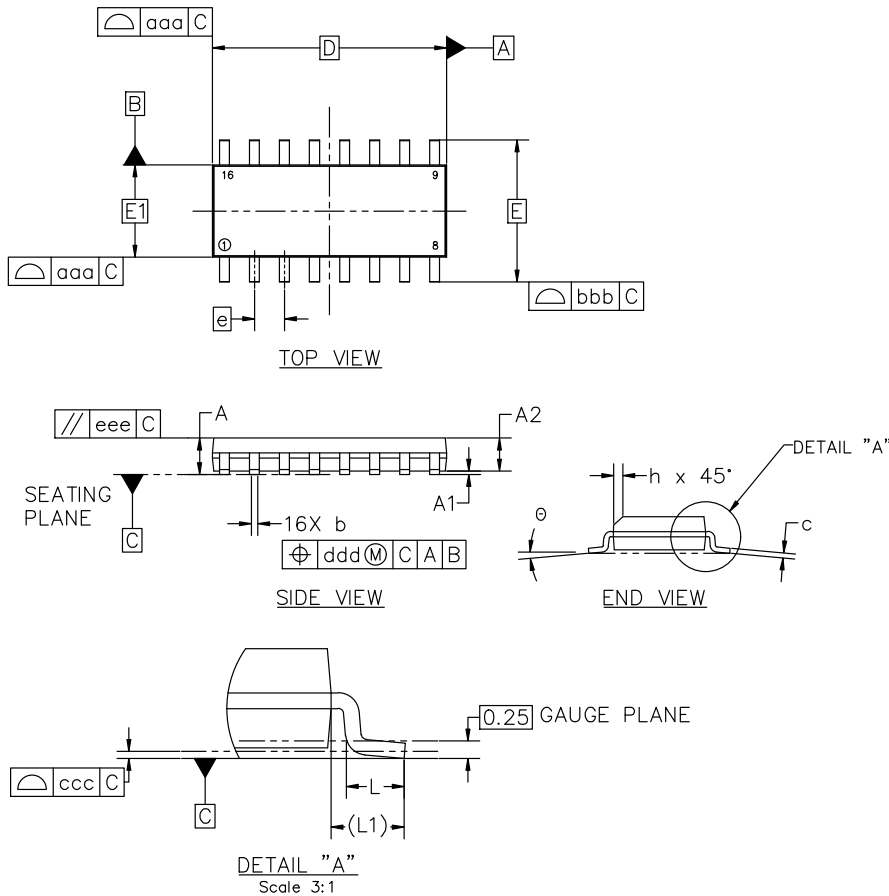


**SOIC-16 9.90x3.90x1.37 1.27P**  
**CASE 751B**  
**ISSUE M**

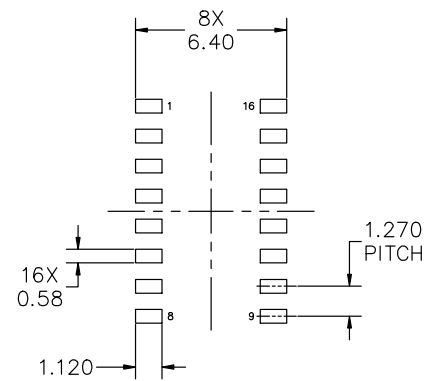
DATE 18 OCT 2024

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



| MILLIMETERS                    |          |      |      |
|--------------------------------|----------|------|------|
| DIM                            | MIN      | NOM  | MAX  |
| A                              | 1.35     | 1.55 | 1.75 |
| A1                             | 0.10     | 0.18 | 0.25 |
| A2                             | 1.25     | 1.37 | 1.50 |
| b                              | 0.35     | 0.42 | 0.49 |
| c                              | 0.19     | 0.22 | 0.25 |
| D                              | 9.90 BSC |      |      |
| E                              | 6.00 BSC |      |      |
| E1                             | 3.90 BSC |      |      |
| e                              | 1.27 BSC |      |      |
| h                              | 0.25     | ---  | 0.50 |
| L                              | 0.40     | 0.83 | 1.25 |
| L1                             | 1.05 REF |      |      |
| θ                              | 0°       | ---  | 7°   |
| TOLERANCE OF FORM AND POSITION |          |      |      |
| aaa                            | 0.10     |      |      |
| bbb                            | 0.20     |      |      |
| ccc                            | 0.10     |      |      |
| ddd                            | 0.25     |      |      |
| eee                            | 0.10     |      |      |



RECOMMENDED MOUNTING FOOTPRINT

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

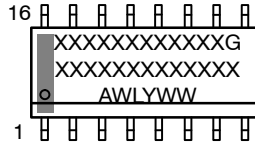
|                         |                                     |  |
|-------------------------|-------------------------------------|--|
| <b>DOCUMENT NUMBER:</b> | <b>98ASB42566B</b>                  | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| <b>DESCRIPTION:</b>     | <b>SOIC-16 9.90X3.90X1.37 1.27P</b> | <b>PAGE 1 OF 2</b>   |

onsemi and onSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**SOIC-16 9.90x3.90x1.37 1.27P**  
**CASE 751B**  
**ISSUE M**

DATE 18 OCT 2024

**GENERIC  
MARKING DIAGRAM\***



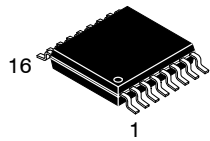
XXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

|   |   |   |   |
|---|---|---|---|
| <p><b>STYLE 1:</b></p> <p>PIN 1. COLLECTOR<br/> 2. BASE<br/> 3. EMITTER<br/> 4. NO CONNECTION<br/> 5. EMITTER<br/> 6. BASE<br/> 7. COLLECTOR<br/> 8. COLLECTOR<br/> 9. BASE<br/> 10. EMITTER<br/> 11. NO CONNECTION<br/> 12. EMITTER<br/> 13. BASE<br/> 14. COLLECTOR<br/> 15. EMITTER<br/> 16. COLLECTOR</p>                           | <p><b>STYLE 2:</b></p> <p>PIN 1. CATHODE<br/> 2. ANODE<br/> 3. NO CONNECTION<br/> 4. CATHODE<br/> 5. CATHODE<br/> 6. NO CONNECTION<br/> 7. ANODE<br/> 8. CATHODE<br/> 9. CATHODE<br/> 10. ANODE<br/> 11. NO CONNECTION<br/> 12. CATHODE<br/> 13. CATHODE<br/> 14. NO CONNECTION<br/> 15. ANODE<br/> 16. CATHODE</p> | <p><b>STYLE 3:</b></p> <p>PIN 1. COLLECTOR, DYE #1<br/> 2. BASE, #1<br/> 3. EMITTER, #1<br/> 4. COLLECTOR, #1<br/> 5. COLLECTOR, #2<br/> 6. BASE, #2<br/> 7. EMITTER, #2<br/> 8. COLLECTOR, #2<br/> 9. COLLECTOR, #3<br/> 10. BASE, #3<br/> 11. EMITTER, #3<br/> 12. COLLECTOR, #3<br/> 13. COLLECTOR, #4<br/> 14. BASE, #4<br/> 15. EMITTER, #4<br/> 16. COLLECTOR, #4</p>   | <p><b>STYLE 4:</b></p> <p>PIN 1. COLLECTOR, DYE #1<br/> 2. COLLECTOR, #1<br/> 3. COLLECTOR, #2<br/> 4. COLLECTOR, #2<br/> 5. COLLECTOR, #3<br/> 6. COLLECTOR, #3<br/> 7. COLLECTOR, #4<br/> 8. COLLECTOR, #4<br/> 9. BASE, #4<br/> 10. EMITTER, #4<br/> 11. BASE, #3<br/> 12. EMITTER, #3<br/> 13. BASE, #2<br/> 14. EMITTER, #2<br/> 15. BASE, #1<br/> 16. EMITTER, #1</p> |
| <p><b>STYLE 5:</b></p> <p>PIN 1. DRAIN, DYE #1<br/> 2. DRAIN, #1<br/> 3. DRAIN, #2<br/> 4. DRAIN, #2<br/> 5. DRAIN, #3<br/> 6. DRAIN, #3<br/> 7. DRAIN, #4<br/> 8. DRAIN, #4<br/> 9. GATE, #4<br/> 10. SOURCE, #4<br/> 11. GATE, #3<br/> 12. SOURCE, #3<br/> 13. GATE, #2<br/> 14. SOURCE, #2<br/> 15. GATE, #1<br/> 16. SOURCE, #1</p> | <p><b>STYLE 6:</b></p> <p>PIN 1. CATHODE<br/> 2. CATHODE<br/> 3. CATHODE<br/> 4. CATHODE<br/> 5. CATHODE<br/> 6. CATHODE<br/> 7. CATHODE<br/> 8. CATHODE<br/> 9. ANODE<br/> 10. ANODE<br/> 11. ANODE<br/> 12. ANODE<br/> 13. ANODE<br/> 14. ANODE<br/> 15. ANODE<br/> 16. ANODE</p>                                 | <p><b>STYLE 7:</b></p> <p>PIN 1. SOURCE N-CH<br/> 2. COMMON DRAIN (OUTPUT)<br/> 3. COMMON DRAIN (OUTPUT)<br/> 4. GATE P-CH<br/> 5. COMMON DRAIN (OUTPUT)<br/> 6. COMMON DRAIN (OUTPUT)<br/> 7. COMMON DRAIN (OUTPUT)<br/> 8. SOURCE P-CH<br/> 9. SOURCE P-CH<br/> 10. COMMON DRAIN (OUTPUT)<br/> 11. COMMON DRAIN (OUTPUT)<br/> 12. COMMON DRAIN (OUTPUT)<br/> 13. GATE N-CH<br/> 14. COMMON DRAIN (OUTPUT)<br/> 15. COMMON DRAIN (OUTPUT)<br/> 16. SOURCE N-CH</p> |   |

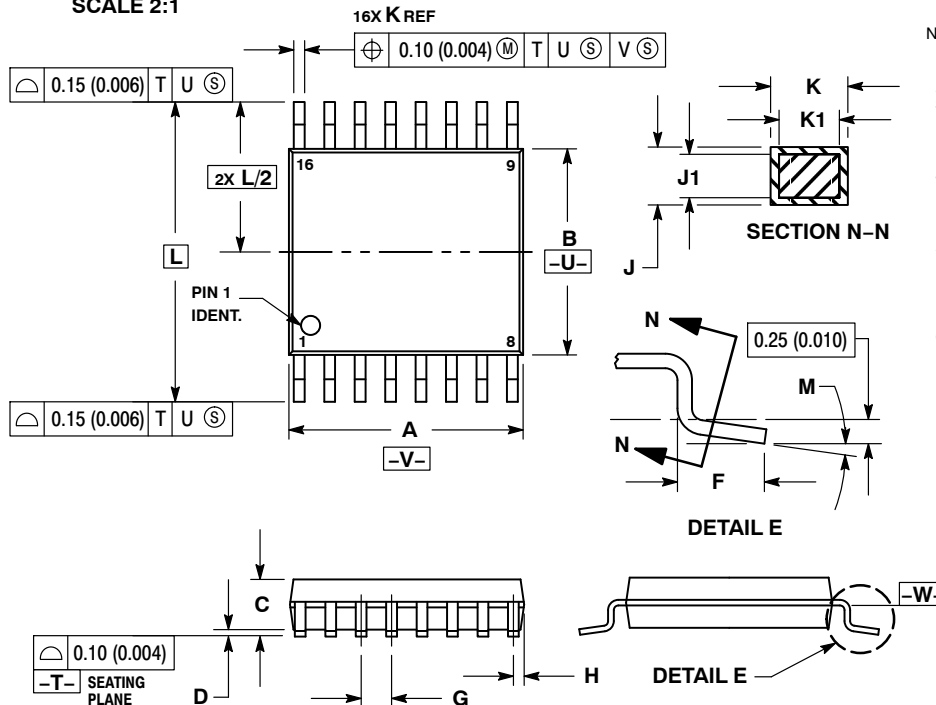
|                         |                                     |   |
|-------------------------|-------------------------------------|---|
| <b>DOCUMENT NUMBER:</b> | <b>98ASB42566B</b>                  | Electronic versions are uncontrolled except when accessed directly from the Document Repository.<br>Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| <b>DESCRIPTION:</b>     | <b>SOIC-16 9.90X3.90X1.37 1.27P</b> | <b>PAGE 2 OF 2</b>  |

**onsemi** and **ONSEMI** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.



TSSOP-16 WB  
CASE 948F  
ISSUE B

DATE 19 OCT 2006

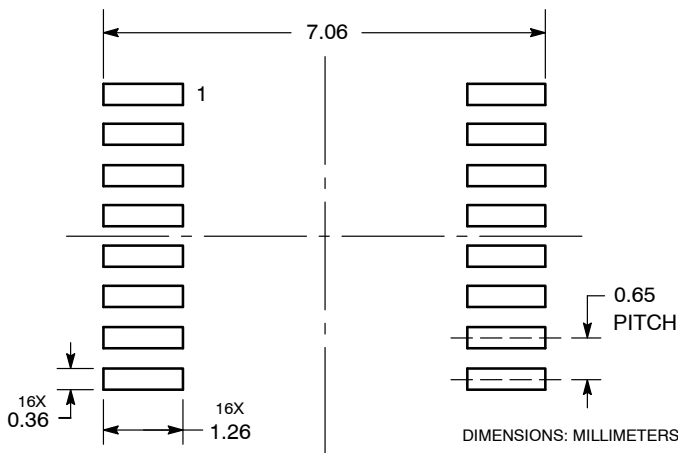


NOTES:

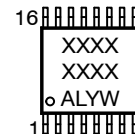
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.18        | 0.28 | 0.007     | 0.011 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

RECOMMENDED  
SOLDERING FOOTPRINT\*



GENERIC  
MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- G or ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

|                  |             |  |
|------------------|-------------|--|
| DOCUMENT NUMBER: | 98ASH70247A | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION:     | TSSOP-16    | PAGE 1 OF 1  |

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)