

# MC74HC393A

## Dual 4-Stage Binary Ripple Counter

### High-Performance Silicon-Gate CMOS

The MC74HC393A is identical in pinout to the LS393. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

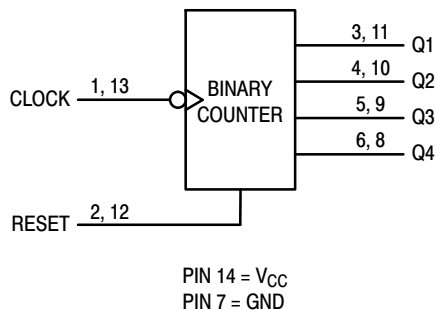
This device consists of two independent 4-bit binary ripple counters with parallel outputs from each counter stage. A ÷ 256 counter can be obtained by cascading the two binary counters.

Internal flip-flops are triggered by high-to-low transitions of the clock input. Reset for the counters is asynchronous and active-high. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or as strobes except when gated with the Clock of the HC393A.

#### Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the JEDEC Standard No. 7 A Requirements
- Chip Complexity: 236 FETs or 59 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

#### LOGIC DIAGRAM



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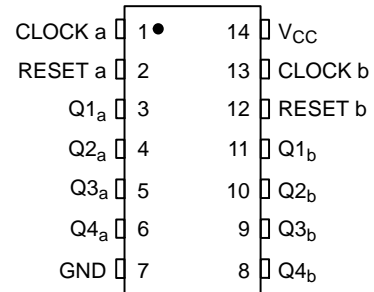


SOIC-14 NB  
D SUFFIX  
CASE 751A

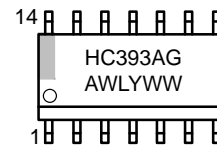


TSSOP-14  
DT SUFFIX  
CASE 948G

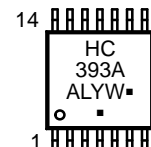
#### PIN ASSIGNMENT



#### MARKING DIAGRAMS



SOIC-14 NB



TSSOP-14

- A = Assembly Location
- L, WL = Wafer Lot
- Y, YY = Year
- W, WW = Work Week
- G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

#### FUNCTION TABLE

| Inputs |       | Outputs               |
|--------|-------|-----------------------|
| Clock  | Reset |                       |
| X      | H     | L                     |
| H      | L     | No Change             |
| L      | L     | No Change             |
|        | L     | No Change             |
|        | L     | Advance to Next State |

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

# MC74HC393A

## MAXIMUM RATINGS

| Symbol    | Parameter  | Value                  | Unit |
|-----------|--|------------------------|------|
| $V_{CC}$  | DC Supply Voltage (Referenced to GND)                                    | -0.5 to +7.0           | V    |
| $V_{in}$  | DC Input Voltage (Referenced to GND)                                     | -0.5 to $V_{CC} + 0.5$ | V    |
| $V_{out}$ | DC Output Voltage (Referenced to GND)                                    | -0.5 to $V_{CC} + 0.5$ | V    |
| $I_{in}$  | DC Input Current, per Pin  | $\pm 20$               | mA   |
| $I_{out}$ | DC Output Current, per Pin   | $\pm 25$               | mA   |
| $I_{CC}$  | DC Supply Current, $V_{CC}$ and GND Pins                                 | $\pm 50$               | mA   |
| $P_D$     | Power Dissipation in Still Air, SOIC Package†<br>TSSOP Package†          | 500<br>450             | mW   |
| $T_{stg}$ | Storage Temperature  | -65 to +150            | °C   |
| $T_L$     | Lead Temperature, 1 mm from Case for 10 Seconds<br>SOIC or TSSOP Package | 260                    | °C   |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating: SOIC Package: -7 mW/°C from 65° to 125°C  
TSSOP Package: -6.1 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

| Symbol            | Parameter  | Min  | Max              | Unit                      |    |
|-------------------|--|--|------------------|---------------------------|----|
| $V_{CC}$          | DC Supply Voltage (Referenced to GND)                | 2.0  | 6.0              | V                         |    |
| $V_{in}, V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0  | $V_{CC}$         | V                         |    |
| $T_A$             | Operating Temperature, All Package Types             | -55  | +125             | °C                        |    |
| $t_r, t_f$        | Input Rise and Fall Time<br>(Figure 1)               | $V_{CC} = 2.0 \text{ V}$<br>$V_{CC} = 3.0 \text{ V}$<br>$V_{CC} = 4.5 \text{ V}$<br>$V_{CC} = 6.0 \text{ V}$ | 0<br>0<br>0<br>0 | 1000<br>600<br>500<br>400 | ns |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol   | Parameter                         | Test Conditions   | $V_{CC}$<br>V | Guaranteed Limit |        |         | Unit |
|----------|-----------------------------------|---|---------------|------------------|--------|---------|------|
|          |                                   |   |               | -55 to<br>25°C   | ≤ 85°C | ≤ 125°C |      |
| $V_{IH}$ | Minimum High-Level Input Voltage  | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$<br>$ I_{out}  \leq 20 \mu\text{A}$   | 2.0           | 1.5              | 1.5    | 1.5     | V    |
|          |                                   |   | 3.0           | 2.1              | 2.1    | 2.1     |      |
|          |                                   |   | 4.5           | 3.15             | 3.15   | 3.15    |      |
|          |                                   |   | 6.0           | 4.2              | 4.2    | 4.2     |      |
| $V_{IL}$ | Maximum Low-Level Input Voltage   | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$<br>$ I_{out}  \leq 20 \mu\text{A}$   | 2.0           | 0.5              | 0.5    | 0.5     | V    |
|          |                                   |   | 3.0           | 0.9              | 0.9    | 0.9     |      |
|          |                                   |   | 4.5           | 1.35             | 1.35   | 1.35    |      |
|          |                                   |   | 6.0           | 1.80             | 1.80   | 1.80    |      |
| $V_{OH}$ | Minimum High-Level Output Voltage | $V_{in} = V_{IH} \text{ or } V_{IL}$<br>$ I_{out}  \leq 20 \mu\text{A}$   | 2.0           | 1.9              | 1.9    | 1.9     | V    |
|          |                                   |   | 4.5           | 4.4              | 4.4    | 4.4     |      |
|          |                                   |   | 6.0           | 5.9              | 5.9    | 5.9     |      |
|          |                                   | $V_{in} = V_{IH} \text{ or } V_{IL}$<br>$ I_{out}  \leq 2.4 \text{ mA}$<br>$ I_{out}  \leq 4.0 \text{ mA}$<br>$ I_{out}  \leq 5.2 \text{ mA}$ | 3.0           | 2.48             | 2.34   | 2.20    |      |
|          |                                   |   | 4.5           | 3.98             | 3.84   | 3.70    |      |
|          |                                   |   | 6.0           | 5.48             | 5.34   | 5.20    |      |

# MC74HC393A

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND) (continued)

| Symbol          | Parameter                                      | Test Conditions  | V <sub>CC</sub><br>V | Guaranteed Limit |        |         | Unit |
|-----------------|--|--|----------------------|------------------|--------|---------|------|
|                 |  |  |                      | -55 to<br>25°C   | ≤ 85°C | ≤ 125°C |      |
| V <sub>OL</sub> | Maximum Low-Level Output Voltage               | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 μA  | 2.0                  | 0.1              | 0.1    | 0.1     | V    |
|                 |  |  | 4.5                  | 0.1              | 0.1    | 0.1     |      |
|                 |  |  | 6.0                  | 0.1              | 0.1    | 0.1     |      |
|                 |  | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 2.4 mA<br> I <sub>out</sub>   ≤ 4.0 mA<br> I <sub>out</sub>   ≤ 5.2 mA | 3.0                  | 0.26             | 0.33   | 0.40    |      |
|                 |  |  | 4.5                  | 0.26             | 0.33   | 0.40    |      |
|                 |  |  | 6.0                  | 0.26             | 0.33   | 0.40    |      |
| I <sub>in</sub> | Maximum Input Leakage Current                  | V <sub>in</sub> = V <sub>CC</sub> or GND   | 6.0                  | ±0.1             | ±1.0   | ±1.0    | μA   |
| I <sub>CC</sub> | Maximum Quiescent Supply Current (per Package) | V <sub>in</sub> = V <sub>CC</sub> or GND<br>I <sub>out</sub> = 0 μA  | 6.0                  | 4                | 40     | 160     | μA   |

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

| Symbol                                 | Parameter   | V <sub>CC</sub><br>V                    | Guaranteed Limit |        |         | Unit |
|--|---|---|------------------|--------|---------|------|
|  |   |   | -55 to<br>25°C   | ≤ 85°C | ≤ 125°C |      |
| f <sub>max</sub>                       | Maximum Clock Frequency (50% Duty Cycle)<br>(Figures 1 and 3)   | 2.0                                     | 10               | 9      | 8       | MHz  |
|  |   | 3.0                                     | 15               | 14     | 12      |      |
|  |   | 4.5                                     | 30               | 28     | 25      |      |
|  |   | 6.0                                     | 50               | 45     | 40      |      |
|  |   |   |                  |        |         |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Clock to Q1<br>(Figures 1 and 3)     | 2.0                                     | 70               | 80     | 90      | ns   |
|  |   | 3.0                                     | 40               | 45     | 50      |      |
|  |   | 4.5                                     | 24               | 30     | 36      |      |
|  |   | 6.0                                     | 20               | 26     | 31      |      |
|  |   |   |                  |        |         |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Clock to Q2<br>(Figures 1 and 3)     | 2.0                                     | 100              | 105    | 180     | ns   |
|  |   | 3.0                                     | 56               | 70     | 100     |      |
|  |   | 4.5                                     | 34               | 45     | 55      |      |
|  |   | 6.0                                     | 20               | 38     | 48      |      |
|  |   |   |                  |        |         |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Clock to Q3<br>(Figures 1 and 3)     | 2.0                                     | 130              | 150    | 180     | ns   |
|  |   | 3.0                                     | 80               | 105    | 130     |      |
|  |   | 4.5                                     | 44               | 55     | 70      |      |
|  |   | 6.0                                     | 37               | 47     | 58      |      |
|  |   |   |                  |        |         |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Clock to Q4<br>(Figures 1 and 3)     | 2.0                                     | 160              | 250    | 300     | ns   |
|  |   | 3.0                                     | 110              | 185    | 210     |      |
|  |   | 4.5                                     | 52               | 65     | 82      |      |
|  |   | 6.0                                     | 44               | 55     | 65      |      |
|  |   |   |                  |        |         |      |
| t <sub>PHL</sub>                       | Maximum Propagation Delay, Reset to any Q<br>(Figures 2 and 3)  | 2.0                                     | 80               | 95     | 110     | ns   |
|  |   | 3.0                                     | 48               | 65     | 75      |      |
|  |   | 4.5                                     | 30               | 38     | 50      |      |
|  |   | 6.0                                     | 26               | 33     | 43      |      |
|  |   |   |                  |        |         |      |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Maximum Output Transition Time, Any Output<br>(Figures 1 and 3) | 2.0                                     | 75               | 95     | 110     | ns   |
|  |   | 3.0                                     | 27               | 32     | 36      |      |
|  |   | 4.5                                     | 15               | 19     | 22      |      |
|  |   | 6.0                                     | 13               | 16     | 19      |      |
|  |   |   |                  |        |         |      |
| C <sub>in</sub>                        | Maximum Input Capacitance                                       | -                                       | 10               | 10     | 10      | pF   |
| C <sub>PD</sub>                        | Power Dissipation Capacitance (Per Counter)*                    | Typical @ 25°C, V <sub>CC</sub> = 5.0 V |                  |        | pF      |      |
|  |   | 35                                      |                  |        |         |      |

\* Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>.

# MC74HC393A

## TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

| Symbol                          | Parameter  | V <sub>CC</sub><br>V | Guaranteed Limit |        |         | Unit |
|---------------------------------|--|----------------------|------------------|--------|---------|------|
|                                 |  |                      | -55 to<br>25°C   | ≤ 85°C | ≤ 125°C |      |
| t <sub>rec</sub>                | Minimum Recovery Time, Reset Inactive to Clock<br>(Figure 2) | 2.0                  | 25               | 30     | 40      | ns   |
|                                 |  | 3.0                  | 15               | 20     | 30      |      |
|                                 |  | 4.5                  | 10               | 13     | 15      |      |
|                                 |  | 6.0                  | 9                | 11     | 13      |      |
| t <sub>w</sub>                  | Minimum Pulse Width, Clock<br>(Figure 1)                     | 2.0                  | 75               | 95     | 110     | ns   |
|                                 |  | 3.0                  | 27               | 32     | 36      |      |
|                                 |  | 4.5                  | 15               | 19     | 22      |      |
|                                 |  | 6.0                  | 13               | 15     | 19      |      |
| t <sub>w</sub>                  | Minimum Pulse Width, Reset<br>(Figure 2)                     | 2.0                  | 75               | 95     | 110     | ns   |
|                                 |  | 3.0                  | 27               | 32     | 36      |      |
|                                 |  | 4.5                  | 15               | 19     | 22      |      |
|                                 |  | 6.0                  | 13               | 15     | 19      |      |
| t <sub>r</sub> , t <sub>f</sub> | Maximum Input Rise and Fall Times<br>(Figure 1)              | 2.0                  | 1000             | 1000   | 1000    | ns   |
|                                 |  | 3.0                  | 800              | 800    | 800     |      |
|                                 |  | 4.5                  | 500              | 500    | 500     |      |
|                                 |  | 6.0                  | 400              | 400    | 400     |      |

## PIN DESCRIPTIONS

### INPUTS

#### Clock (Pins 1, 13)

Clock input. The internal flip-flops are toggled and the counter state advances on high-to-low transitions of the clock input.

### OUTPUTS

#### Q1, Q2, Q3, Q4 (Pins 3, 4, 5, 6, 8, 9, 10, 11)

Parallel binary outputs Q4 is the most significant bit.

### CONTROL INPUTS

#### Reset (Pins 2, 12)

Active-high, asynchronous reset. A separate reset is provided for each counter. A high at the Reset input prevents counting and forces all four outputs low.

# MC74HC393A

## SWITCHING WAVEFORMS

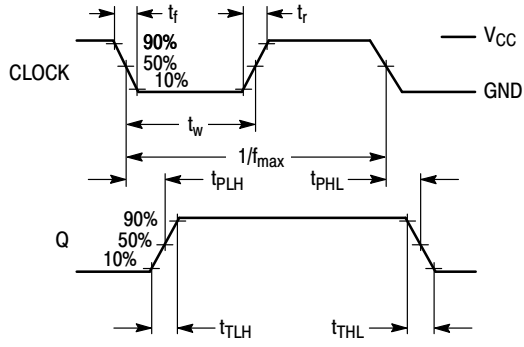


Figure 1.

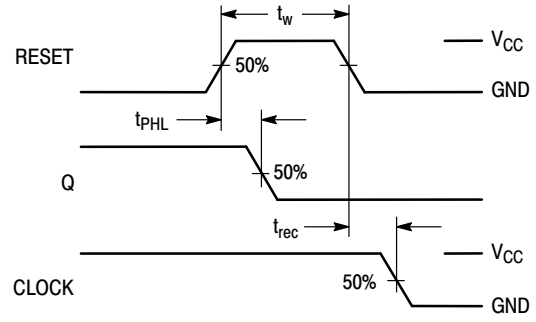
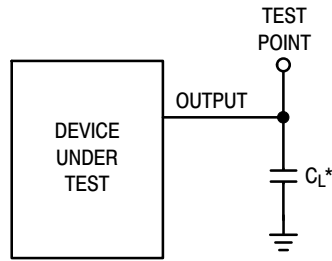


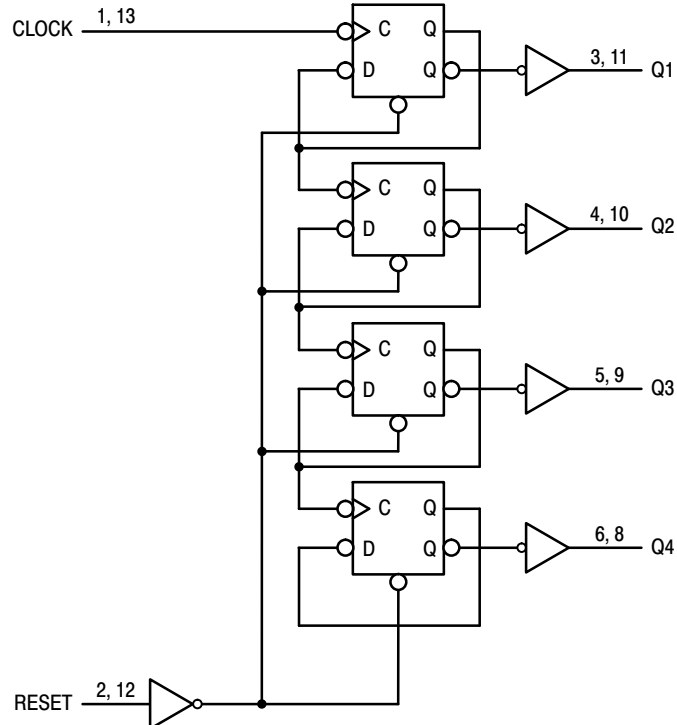
Figure 2.



\*Includes all probe and jig capacitance

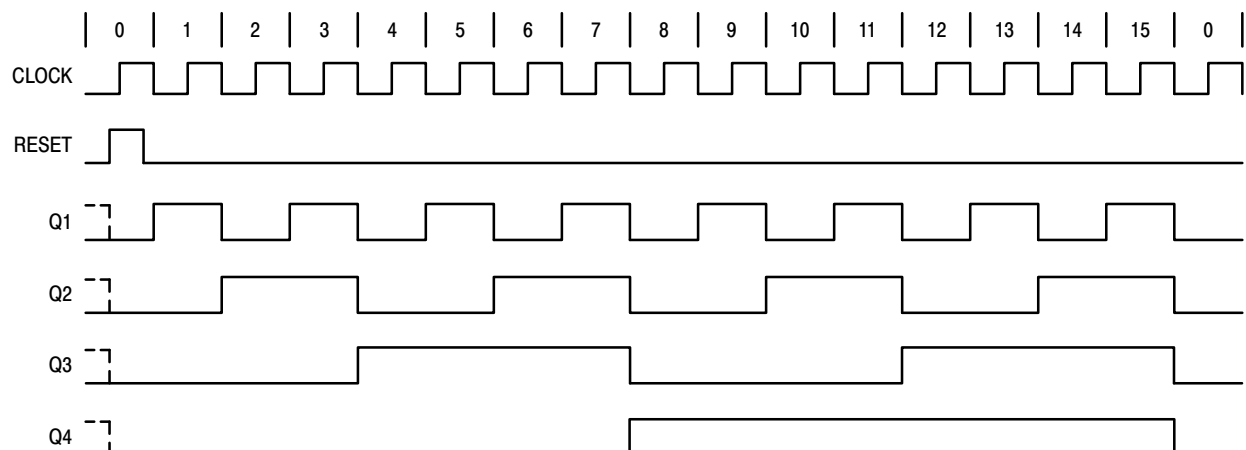
Figure 3. Test Circuit

## EXPANDED LOGIC DIAGRAM



# MC74HC393A

## TIMING DIAGRAM



## COUNT SEQUENCE

| Count | Outputs |    |    |    |
|-------|---------|----|----|----|
|       | Q4      | Q3 | Q2 | Q1 |
| 0     | L       | L  | L  | L  |
| 1     | L       | L  | L  | H  |
| 2     | L       | L  | H  | L  |
| 3     | L       | L  | H  | H  |
| 4     | L       | H  | L  | L  |
| 5     | L       | H  | L  | H  |
| 6     | L       | H  | H  | L  |
| 7     | L       | H  | H  | H  |
| 8     | H       | L  | L  | L  |
| 9     | H       | L  | L  | H  |
| 10    | H       | L  | H  | L  |
| 11    | H       | L  | H  | H  |
| 12    | H       | H  | L  | L  |
| 13    | H       | H  | L  | H  |
| 14    | H       | H  | H  | L  |
| 15    | H       | H  | H  | H  |

## ORDERING INFORMATION

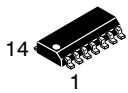
| Device           | Package                 | Shipping†          |
|------------------|-------------------------|--------------------|
| MC74HC393ADG     | SOIC-14 NB<br>(Pb-Free) | 55 Units / Rail    |
| MC74HC393ADR2G   | SOIC-14 NB<br>(Pb-Free) | 2500 / Tape & Reel |
| NLV74HC393ADR2G* | SOIC-14 NB<br>(Pb-Free) | 2500 / Tape & Reel |
| MC74HC393ADTR2G  | TSSOP-14<br>(Pb-Free)   | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

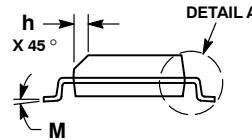
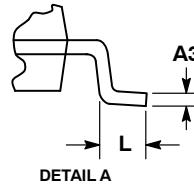
ON Semiconductor®



SCALE 1:1

SOIC-14 NB  
CASE 751A-03  
ISSUE L

DATE 03 FEB 2016

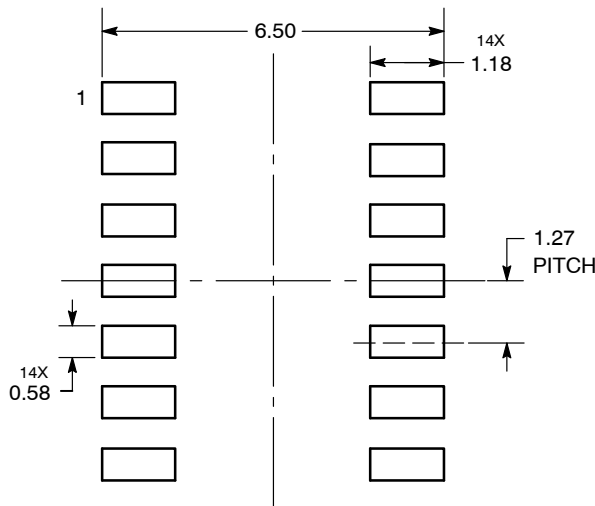


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 1.35        | 1.75 | 0.054     | 0.068 |
| A1  | 0.10        | 0.25 | 0.004     | 0.010 |
| A3  | 0.19        | 0.25 | 0.008     | 0.010 |
| b   | 0.35        | 0.49 | 0.014     | 0.019 |
| D   | 8.55        | 8.75 | 0.337     | 0.344 |
| E   | 3.80        | 4.00 | 0.150     | 0.157 |
| e   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 5.80        | 6.20 | 0.228     | 0.244 |
| h   | 0.25        | 0.50 | 0.010     | 0.019 |
| L   | 0.40        | 1.25 | 0.016     | 0.049 |
| M   | 0°          | 7°   | 0°        | 7°    |

SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

STYLES ON PAGE 2

|                  |             |  |
|------------------|-------------|--|
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| DESCRIPTION:     | SOIC-14 NB  | PAGE 1 OF 2  |

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**SOIC-14**  
**CASE 751A-03**  
**ISSUE L**

DATE 03 FEB 2016

STYLE 1:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. NO CONNECTION  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 2:  
 CANCELLED

STYLE 3:  
 PIN 1. NO CONNECTION  
 2. ANODE  
 3. ANODE  
 4. NO CONNECTION  
 5. ANODE  
 6. NO CONNECTION  
 7. ANODE  
 8. ANODE  
 9. ANODE  
 10. NO CONNECTION  
 11. ANODE  
 12. ANODE  
 13. NO CONNECTION  
 14. COMMON CATHODE

STYLE 4:  
 PIN 1. NO CONNECTION  
 2. CATHODE  
 3. CATHODE  
 4. NO CONNECTION  
 5. CATHODE  
 6. NO CONNECTION  
 7. CATHODE  
 8. CATHODE  
 9. CATHODE  
 10. NO CONNECTION  
 11. CATHODE  
 12. CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 5:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. COMMON ANODE  
 8. COMMON CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 6:  
 PIN 1. CATHODE  
 2. CATHODE  
 3. CATHODE  
 4. CATHODE  
 5. CATHODE  
 6. CATHODE  
 7. CATHODE  
 8. ANODE  
 9. ANODE  
 10. ANODE  
 11. ANODE  
 12. ANODE  
 13. ANODE  
 14. ANODE

STYLE 7:  
 PIN 1. ANODE/CATHODE  
 2. COMMON ANODE  
 3. COMMON CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. COMMON CATHODE  
 12. COMMON ANODE  
 13. ANODE/CATHODE  
 14. ANODE/CATHODE

STYLE 8:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. COMMON ANODE  
 8. COMMON ANODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. NO CONNECTION  
 12. ANODE/CATHODE  
 13. ANODE/CATHODE  
 14. COMMON CATHODE

|                         |                    |   |
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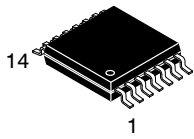
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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



**TSSOP-14 WB**  
CASE 948G  
ISSUE C

DATE 17 FEB 2016

SCALE 2:1



**NOTES:**

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.50        | 0.60 | 0.020     | 0.024 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

**GENERIC MARKING DIAGRAM\***

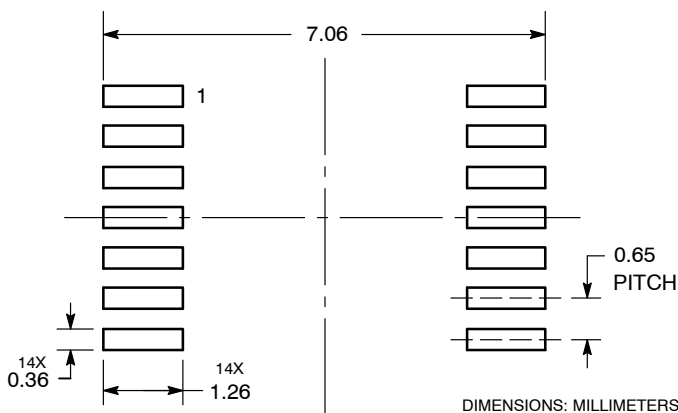


- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

**SOLDERING FOOTPRINT**



|                         |                    |  |
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