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MC74ACT323

8-Input Universal Shift/Storage Register with Synchronous Reset and Common I/O Pins

The MC74ACT323 is an 8-bit universal shift/storage register with3-state outputs. Its function is similar to the MC74ACT299 with the exception of Synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate serial inputs and outputs are provided for Q_0 and Q_7 to allow easy cascading. Four operation modes are possible: hold (store), shift left, shift right and parallel load.

- Common Parallel I/O for Reduced Pin Count
- Additional Serial Inputs and Outputs for Expansion
- Four Operating Modes: Shift Left, Shift Right, Load and Store
- 3-State Outputs for Bus-Oriented Applications
- Outputs Source/Sink 24 mA
- TTL Compatible Inputs

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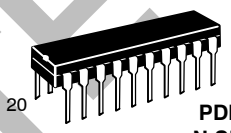
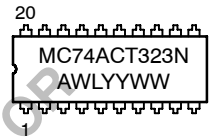
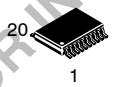
MARKING DIAGRAMS



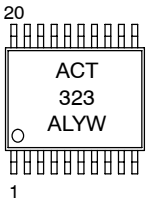
PDIP–20
N SUFFIX
CASE 738



SO–20
DW SUFFIX
CASE 751D



TSSOP–20
DT SUFFIX
CASE 948E



A	=	Assembly Location
L, WL	=	Wafer Lot
Y, YY	=	Year
W, WW	=	Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC74ACT323N	PDIP–20	18 Units/Rail
MC74ACT323DW	SOIC–20	38 Units/Rail
MC74ACT323DWR2	SOIC–20	1000 Tape & Reel
MC74ACT323DT	TSSOP–20	75 Units/Rail
MC74ACT323DTR2	TSSOP–20	2500 Tape & Reel

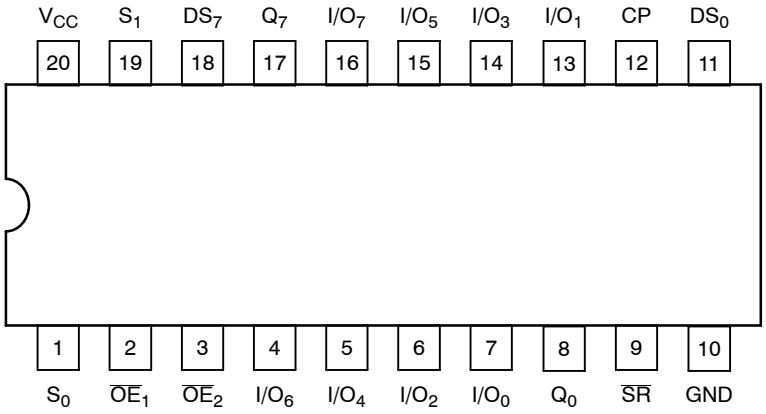


Figure 1. Pinout: 20−Lead Packages Conductors (Top View)

PIN ASSIGNMENT

PIN	FUNCTION
CP	Clock Pulse Input
DS_0	Serial Data Input for Right Shift
DS_7	Serial Data Input for Left Shift
S_0, S_1	Mode Select Inputs
$\overline{SR}$	Synchronous Master Reset
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Inputs
I/O_0–I/O_7	Multipled Parallel Data Inputs or 3-State Parallel Data Outputs
Q_0, Q_7	Serial Outputs

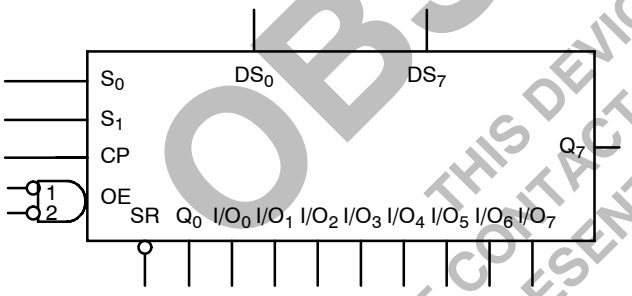
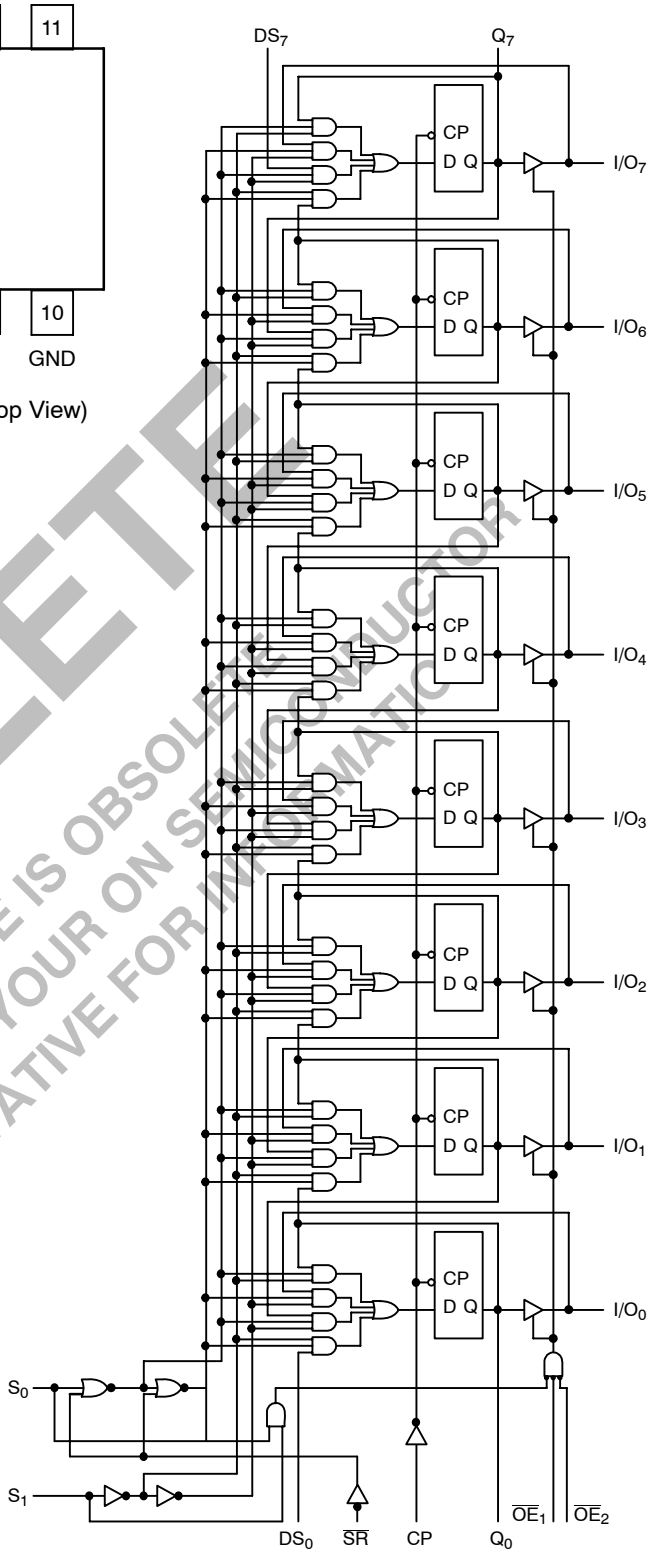


Figure 3. Logic Symbol

TRUTH TABLE

Inputs				Response
$\overline{SR}$	S_1	S_0	CP	
L	X	X	⌐	Synchronous Reset; Q_0 – Q_7 = LOW
H	H	H	⌐	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	⌐	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	⌐	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level X = Immaterial
L = LOW Voltage Level ⌐ = LOW-to-HIGH Clock Transition



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 2. LOGIC DIAGRAM

FUNCTIONAL DESCRIPTION

The MC74ACT323 contains eight edge- triggered D-type flip-flops and the interstage logic necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1 as shown in the Mode Select Table. All flip-flop outputs are brought out through 3 state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{SR}$ overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of CP. All other state changes are also initiated by the LOW-to-HIGH CP transition. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

MAXIMUM RATINGS (Note 1)

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +7.0	V
V_I	DC Input Voltage		$-0.5 \le V_I \le V_{CC} + 0.5$	V
V_O	DC Output Voltage	(Note 2)	$-0.5 \le V_O \le V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current		±20	mA
I_{OK}	DC Output Diode Current		±50	mA
I_O	DC Output Sink/Source Current		±50	mA
I_{CC}	DC Supply Current per Output Pin		±50	mA
I_{GND}	DC Ground Current per Output Pin		±50	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction temperature under Bias		+150	°C
θ_{JA}	Thermal resistance	PDIP SOIC TSSOP	67 96 128	°C/W
P_D	Power Dissipation in Still Air at 85°C	PDIP SOIC TSSOP	750 500 450	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 30% − 35%	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5)	> 2000 > 200 >1000	V
$I_{Latch-Up}$	Latch−Up Performance	Above V_{CC} and Below GND at 85°C (Note 6)	±100	mA

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Extended exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum−rated conditions is not implied.
2. I_O absolute maximum rating must be observed.
3. Tested to EIA/JESD22−A114−A.
4. Tested to EIA/JESD22−A115−A.
5. Tested to JESD22−C101−A.
6. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	DC Input Voltage (Referenced to GND)		4.5		5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0		V_{CC}	V
T_A	Operating Temperature, All Package Types		−40	25	+85	°C
t_r, t_f	Input Rise and Fall Time (Note 8)	V_{CC} = 4.5 V V_{CC} = 5.5 V	0 0	10 8.0	10 8.0	ns/V
T_J	Junction Temperature (PDIP)				140	°C
I_{OH}	Output Current − High				−24	mA
I_{OL}	Output Current − Low				24	mA

7. Unused Inputs may not be left open. All inputs must be tied to a high voltage level or low logic voltage level.
8. V_{in} from 0.8 V to 2.0 V; refer to individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	T_A = +25°C	T_A = −40°C to +85°C	Unit	Conditions
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	V V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	V V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	V V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	V V	*V_{IN} = V_{IL} or V_{IH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	V V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	V V	*V_{IN} = V_{IL} or V_{IH} −24 mA I_{OH} −24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	μA	V_I = V_{CC}, GND
ΔI_{CCT}	Additional Maximum I_{CC}/Input	5.5	0.6		mA	V_I = V_{CC} − 2.1 V
I_{OZ}	Maximum 3−State Current	5.5		±0.5	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD} I_{OHD}	†Minimum Dynamic Output Current	5.5 5.5			mA mA	V_{OLD} = 1.65 V Max V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS $t_r = t_f = 3.0$ ns (For Figures and Waveforms, See Figures 4 and 5.)

Symbol	Parameter	V_{CC}* (V)	T_A = +25°C, C_L = 50 pF			T_A = −40°C to +85°C, C_L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
f_{max}	Maximum Input Frequency	5.0	120	125		110		MHz
t_{PLH}	Propagation Delay CP to Q_0 or Q_7	5.0	5.0	9.0	12.5	4.0	14	ns
t_{PHL}	Propagation Delay CP to Q_0 or Q_7	5.0	5.0	9.0	13.5	4.5	15	ns
t_{PLH}	Propagation Delay CP to I/O_n	5.0	5.0	8.5	12.5	4.5	14.5	ns
t_{PZH}	Output Enable Time	5.0	3.5	7.5	11	3.0	12.5	ns
t_{PZL}	Output Enable Time	5.0	3.5	7.5	11.5	3.0	13	ns
t_{PHZ}	Output Disable Time	5.0	4.0	8.5	12.5	3.0	13.5	ns
t_{PLZ}	Output Disable Time	5.0	3.0	8.0	11.5	2.5	12.5	ns

*Voltage Range 5.0 V is 5.0 V ±0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	T_A = +25°C, C_L = 50 pF		T_A = −40°C to +85°C, C_L = 50 pF	Unit
			Typ	Guaranteed Minimum		
t_s	Setup Time, HIGH or LOW S_0 or S_1 to CP	5.0	2.0	5.0	5.0	ns
t_h	Hold Time, HIGH or LOW S_0 or S_1 to CP	5.0	0	1.5	1.5	ns
t_s	Setup Time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	5.0	1.0	4.0	4.5	ns
t_h	Hold Time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	5.0	0	1.0	1.0	ns
t_s	Setup Time, HIGH or LOW $\overline{SR}$ to CP	5.0	1.0	2.5	2.5	ns
t_h	Hold Time, HIGH or LOW $\overline{SR}$ to CP	5.0	0	1.0	1.0	ns
t_w	CP Pulse Width HIGH or LOW	5.0	2.0	4.0	4.5	ns

*Voltage Range 5.0 V is 5.0 V ±0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	170	pF	V_{CC} = 5.0 V

SWITCHING WAVEFORMS

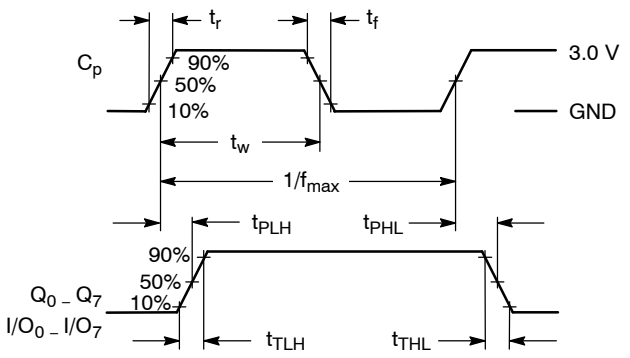


Figure 4.

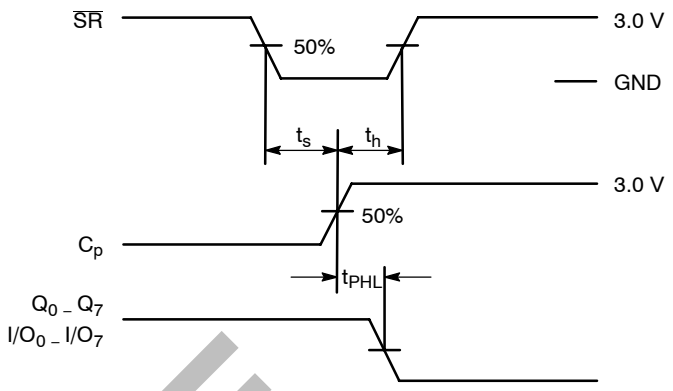


Figure 5.

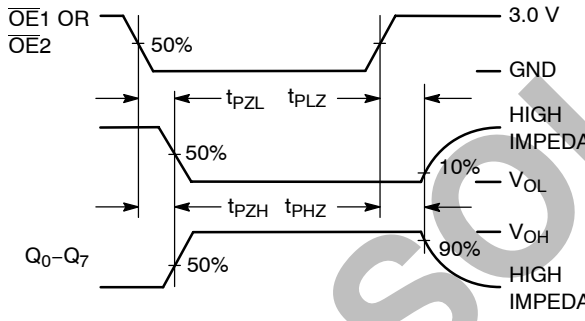
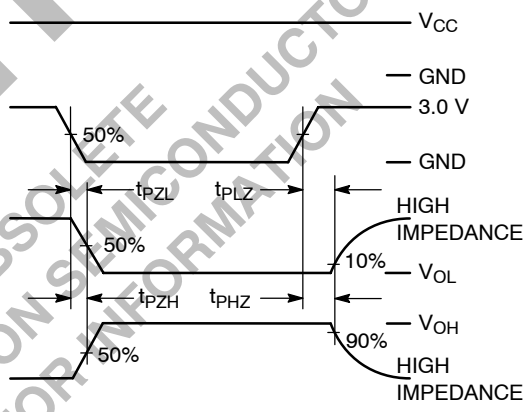


Figure 6.



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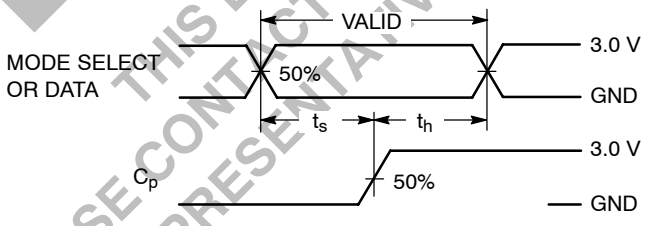
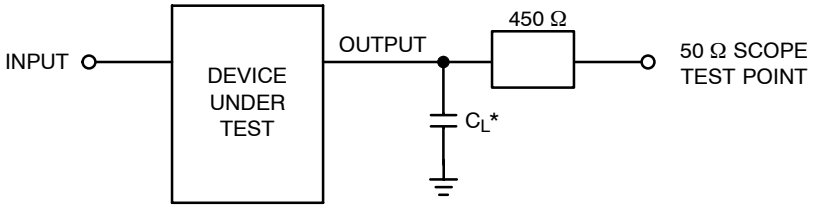


Figure 8.

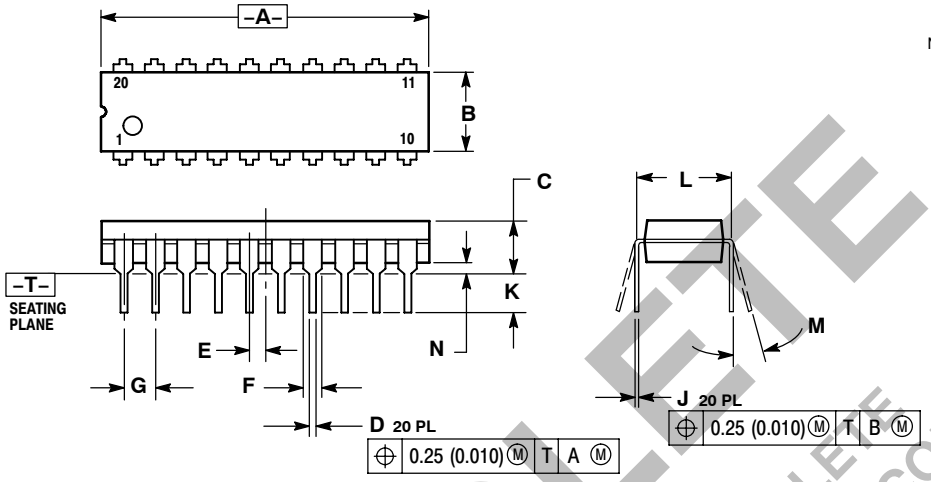


*Includes all probe and jig capacitance

Figure 9. Test Circuit

PACKAGE DIMENSIONS

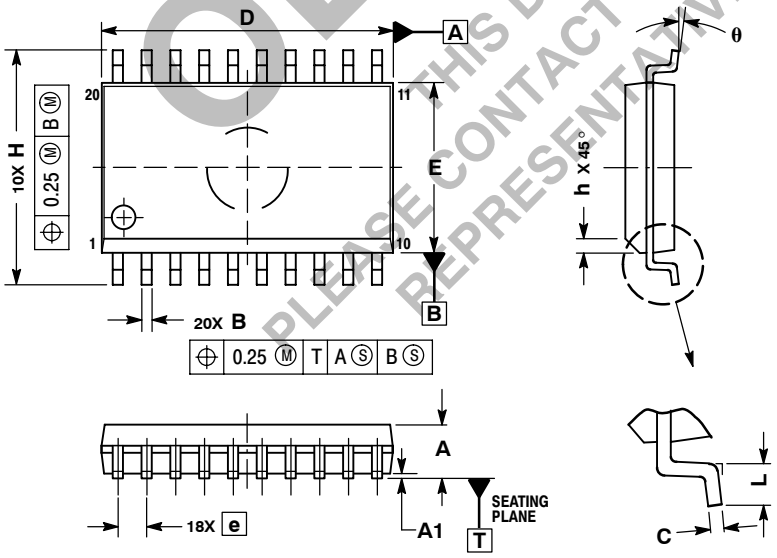
PDIP–20
N SUFFIX
20 PIN PLASTIC DIP PACKAGE
CASE 738–03
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

SO–20
DW SUFFIX
20 PIN PLASTIC SOIC PACKAGE
CASE 751D–05
ISSUE F

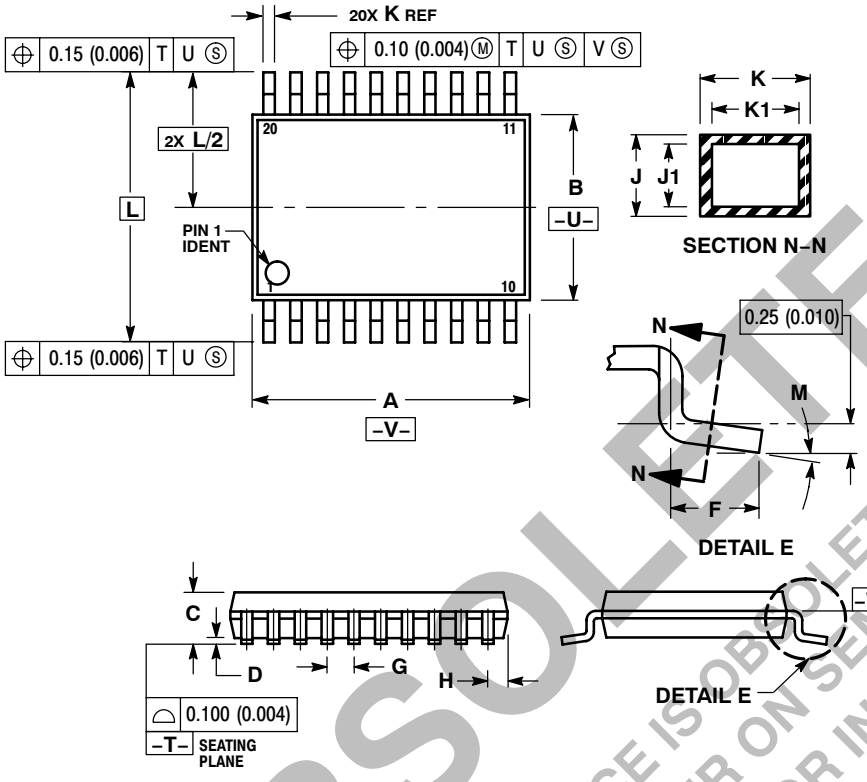


NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

PACKAGE DIMENSIONS

TSSOP−20
DT SUFFIX
20 PIN PLASTIC TSSOP PACKAGE
CASE 948E−02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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