MC34152, MC33152, NCV33152

MOSFET Driver, High Speed, Dual

The MC34152/MC33152 are dual noninverting high speed drivers specifically designed for applications that require low current digital signals to drive large capacitive loads with high slew rates. These devices feature low input current making them CMOS/LSTTL logic compatible, input hysteresis for fast output switching that is independent of input transition time, and two high current totem pole outputs ideally suited for driving power MOSFETs. Also included is an undervoltage lockout with hysteresis to prevent system erratic operation at low supply voltages.

Typical applications include switching power supplies, dc-to-dc converters, capacitor charge pump voltage doublers/inverters, and motor controllers.

This device is available in dual-in-line and surface mount packages.

Features
- Two Independent Channels with 1.5 A Totem Pole Outputs
- Output Rise and Fall Times of 15 ns with 1000 pF Load
- CMOS/LSTTL Compatible Inputs with Hysteresis
- Undervoltage Lockout with Hysteresis
- Low Standby Current
- Efficient High Frequency Operation
- Enhanced System Performance with Common Switching Regulator Control ICs
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Controls
- These are Pb-Free and Halide-Free Devices

Figure 1. Representative Diagram

Figure 1. Representative Diagram
<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Voltage</td>
<td>$V_{CC}$</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>Logic Inputs (Note 1)</td>
<td>$V_{in}$</td>
<td>−0.3 to $+V_{CC}$</td>
<td>V</td>
</tr>
<tr>
<td>Drive Outputs (Note 2)</td>
<td>$I_O$</td>
<td>1.5</td>
<td>A</td>
</tr>
<tr>
<td>Diode Clamp Current (Drive Output to $V_{CC}$)</td>
<td>$I_{O(clamp)}$</td>
<td>1.0</td>
<td>A</td>
</tr>
</tbody>
</table>

**Power Dissipation and Thermal Characteristics**

- **D Suffix, Plastic Package Case 751**
  - Maximum Power Dissipation @ $T_A = 50^\circ C$
  - Thermal Resistance, Junction-to-Air: $P_D, R_{JA}$
- **P Suffix, Plastic Package, Case 626**
  - Maximum Power Dissipation @ $T_A = 50^\circ C$
  - Thermal Resistance, Junction-to-Air: $P_D, R_{JA}$

| Operating Junction Temperature            | $T_J$  | +150  | °C   |
| Operating Ambient Temperature             | $T_A$  | 0 to +70 | °C   |
|                                           |        | −40 to +85 | °C   |
|                                           |        | −40 to +125 | °C   |
| Storage Temperature Range                 | $T_{stg}$ | −65 to +150 | °C   |

**Electrostatic Discharge Sensitivity (ESD) (Note 3)**

- Human Body Model (HBM): ESD = 2000 V
- Machine Model (MM): ESD = 200 V
- Charged Device Model (CDM): ESD = 1500 V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. For optimum switching speed, the maximum input voltage should be limited to 10 V or $V_{CC}$, whichever is less.
2. Maximum package power dissipation limits must be observed.
3. ESD protection per following tests:
   - JEDEC Standard JESD22–A114–F for HBM
   - JEDEC Standard JESD22–A115–A for MM
   - JEDEC Standard JESD22–C101D for CDM.
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ELECTRICAL CHARACTERISTICS (VCC = 12 V, for typical values TA = 25°C, for min/max values TA is the operating ambient temperature range that applies [Note 4], unless otherwise noted.)

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
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<tr>
<td>LOGIC INPUTS</td>
<td></td>
<td></td>
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<tr>
<td>Input Threshold Voltage</td>
<td></td>
<td></td>
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<tr>
<td>Output Transition High–to–Low State</td>
<td>VH</td>
<td>–</td>
<td>1.75</td>
<td>2.6</td>
<td>V</td>
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<tr>
<td>Output Transition Low–to–High State</td>
<td>VL</td>
<td>0.8</td>
<td>1.58</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>Input Current</td>
<td></td>
<td></td>
<td></td>
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<td></td>
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<tr>
<td>High State (VH = 2.6 V)</td>
<td>IH</td>
<td>–</td>
<td>100</td>
<td>300</td>
<td>µA</td>
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<tr>
<td>Low State (VIL = 0.8 V)</td>
<td>IL</td>
<td>–</td>
<td>20</td>
<td>100</td>
<td>µA</td>
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<tr>
<td>DRIVE OUTPUT</td>
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<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Output Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low State (I(H = 10 mA)</td>
<td>V(OH)</td>
<td>–</td>
<td>10.5</td>
<td>10.4</td>
<td>V</td>
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<tr>
<td>(I(H = 50 mA)</td>
<td></td>
<td>–</td>
<td>1.8</td>
<td>1.1</td>
<td>V</td>
</tr>
<tr>
<td>(I(H = 400 mA)</td>
<td></td>
<td>–</td>
<td>0.8</td>
<td>0.8</td>
<td>V</td>
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<tr>
<td>High State (I(L = 10 mA)</td>
<td>V(OL)</td>
<td>–</td>
<td>0.8</td>
<td>1.2</td>
<td>V</td>
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<tr>
<td>(I(L = 50 mA)</td>
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<td>–</td>
<td>1.1</td>
<td>1.5</td>
<td>V</td>
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<tr>
<td>(I(L = 400 mA)</td>
<td></td>
<td>–</td>
<td>2.5</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>Output Pull–Down Resistor</td>
<td>RPD</td>
<td>–</td>
<td>100</td>
<td>–</td>
<td>kΩ</td>
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<tr>
<td>SWITCHING CHARACTERISTICS (TA = 25°C)</td>
<td></td>
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<td></td>
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<tr>
<td>Propagation Delay (CL = 1.0 nF)</td>
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<td></td>
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<td></td>
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<tr>
<td>Logic Input to: Drive Output Rise (10% Input to 10% Output)</td>
<td>IPLH (IN/OUT)</td>
<td>–</td>
<td>55</td>
<td>120</td>
<td>ns</td>
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<tr>
<td>Drive Output Fall (90% Input to 90% Output)</td>
<td>IPHL (IN/OUT)</td>
<td>–</td>
<td>40</td>
<td>120</td>
<td>ns</td>
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<tr>
<td>Drive Output Rise Time (10% to 90%)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CL = 1.0 nF</td>
<td>tR</td>
<td>–</td>
<td>14</td>
<td>30</td>
<td>ns</td>
</tr>
<tr>
<td>CL = 2.5 nF</td>
<td></td>
<td>–</td>
<td>36</td>
<td>–</td>
<td>ns</td>
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<tr>
<td>Drive Output Fall Time (90% to 10%)</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CL = 1.0 nF</td>
<td>tF</td>
<td>–</td>
<td>15</td>
<td>30</td>
<td>ns</td>
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<tr>
<td>CL = 2.5 nF</td>
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<td>–</td>
<td>32</td>
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<td>ns</td>
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<td>TOTAL DEVICE</td>
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<td></td>
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<tr>
<td>Power Supply Current</td>
<td>I(CC)</td>
<td>–</td>
<td>6.0</td>
<td>8.0</td>
<td>mA</td>
</tr>
<tr>
<td>Standby (Logic Inputs Grounded)</td>
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<td>–</td>
<td>10.5</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>Operating (CL = 1.0 nF Drive Outputs 1 and 2, f = 100 kHz)</td>
<td>–</td>
<td>10.5</td>
<td>15</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Voltage</td>
<td>V(CC)</td>
<td>6.1</td>
<td>–</td>
<td>18</td>
<td>V</td>
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<td>UNDERVOLTAGE LOCKOUT</td>
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<td></td>
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<tr>
<td>Startup Threshold</td>
<td>V(IN)</td>
<td>–</td>
<td>5.8</td>
<td>6.1</td>
<td>V</td>
</tr>
<tr>
<td>Minimum Operating Voltage After Turn–On (V(CC))</td>
<td>V(CC(min))</td>
<td>–</td>
<td>5.3</td>
<td>–</td>
<td>V</td>
</tr>
</tbody>
</table>

4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

Tlow = 0°C for MC34152, −40°C for MC33152, −40°C for MC33152V

Thigh = +70°C for MC34152, +85°C for MC33152, +125°C for MC33152V

NCV33152: Tlow = −40°C, Thigh = +125°C. Guaranteed by design.
Figure 2. Switching Characteristics Test Circuit

Figure 3. Switching Waveform Definitions

Figure 4. Logic Input Current versus Input Voltage

Figure 5. Logic Input Threshold Voltage versus Temperature

Figure 6. Drive Output High to Low Propagation Delay versus Logic Input Overdrive Voltage

Figure 7. Drive Output Low to High Propagation Delay versus Logic Input Overdrive Voltage
Figure 8. Drive Output Clamp Voltage versus Clamp Current

Figure 9. Drive Output Saturation Voltage versus Load Current

Figure 10. Drive Output Saturation Voltage versus Temperature

Figure 11. Drive Output Rise Time

Figure 12. Drive Output Fall Time
MC34152, MC33152, NCV33152

APPLICATIONS INFORMATION

Description

The MC34152 is a dual noninverting high speed driver specifically designed to interface low current digital circuitry with power MOSFETs. This device is constructed with Schottky clamped Bipolar Analog technology which offers a high degree of performance and ruggedness in hostile industrial environments.

Input Stage

The Logic Inputs have 170 mV of hysteresis with the input threshold centered at 1.67 V. The input thresholds are insensitive to VCC making this device directly compatible with CMOS and LSTTL logic families over its entire operating voltage range. Input hysteresis provides fast output switching that is independent of the input signal transition time, preventing output oscillations as the input thresholds are crossed. The inputs are designed to accept a signal amplitude ranging from ground to VCC. This allows the output of one channel to directly drive the input of a second channel for master–slave operation. Each input has a 30 kΩ pulldown resistor so that an unconnected open input will cause the associated Drive Output to be in a known low state.

Output Stage

Each totem pole Drive Output is capable of sourcing and sinking up to 1.5 A with a typical ‘on’ resistance of 2.4 Ω at 1.0 A. The low ‘on’ resistance allows high output currents to be attained at a lower VCC than with comparative CMOS drivers. Each output has a 100 kΩ pulldown resistor to keep the MOSFET gate low when VCC is less than 1.4 V. No over current or thermal protection has been designed into the device, so output shorting to VCC or ground must be avoided.

Parasitic inductance in series with the load will cause the driver outputs to ring above VCC during the turn–on transition, and below ground during the turn–off transition. With CMOS drivers, this mode of operation can cause a destructive output latchup condition. The MC34152 is immune to output latchup. The Drive Outputs contain an internal diode to VCC for clamping positive voltage transients. When operating with VCC at 18 V, proper power supply bypassing must be observed to prevent the output ringing from exceeding the maximum 20 V device rating. Negative output transients are clamped by the internal NPN pullup transistor. Since full supply voltage is applied across
the NPN pullup during the negative output transient, power
dissipation at high frequencies can become excessive.
Figures 19, 20, and 21 show a method of using external
Schottky diode clamps to reduce driver power dissipation.

**Undervoltage Lockout**

An undervoltage lockout with hysteresis prevents erratic
system operation at low supply voltages. The UVLO forces
the Drive Outputs into a low state as VCC rises from 1.4 V
to the 5.8 V upper threshold. The lower UVLO threshold
is 5.3 V, yielding about 500 mV of hysteresis.

**Power Dissipation**

Circuit performance and long term reliability are
enhanced with reduced die temperature. Die temperature
increase is directly related to the power that the integrated
circuit must dissipate and the total thermal resistance from
the junction to ambient. The formula for calculating the
junction temperature with the package in free air is:

\[
T_J = T_A + P_D (R_{JA})
\]

where:
- \( T_J \) = Junction Temperature
- \( T_A \) = Ambient Temperature
- \( P_D \) = Power Dissipation
- \( R_{JA} \) = Thermal Resistance Junction to Ambient

There are three basic components that make up total
power to be dissipated when driving a capacitive load with
respect to ground. They are:

\[
P_D = P_Q + P_C + P_T
\]

where:
- \( P_Q \) = Quiescent Power Dissipation
- \( P_C \) = Capacitive Load Power Dissipation
- \( P_T \) = Transition Power Dissipation

The quiescent power supply current depends on the
supply voltage and duty cycle as shown in Figure 16. The
device’s quiescent power dissipation is:

\[
P_Q = V_{CC} (I_{CCL} [1−D] + I_{CCH} [D])
\]

where:
- \( I_{CCL} \) = Supply Current with Low State Drive
  Outputs
- \( I_{CCH} \) = Supply Current with High State Drive
  Outputs
- \( D \) = Output Duty Cycle

The capacitive load power dissipation is directly related
to the load capacitance value, frequency, and Drive Output
to voltage swing. The capacitive load power dissipation per
driver is:

\[
P_C = V_{CC} (V_{OH} − V_{OL}) C_L f
\]

where:
- \( V_{OH} \) = High State Drive Output Voltage
- \( V_{OL} \) = Low State Drive Output Voltage
- \( C_L \) = Load Capacitance
- \( f \) = Frequency

When driving a MOSFET, the calculation of capacitive
load power \( P_C \) is somewhat complicated by the changing
gate to source capacitance \( C_{GS} \) as the device switches. To
aid in this calculation, power MOSFET manufacturers
provide gate charge information on their data sheets.
Figure 17 shows a curve of gate voltage versus gate charge
for the ON Semiconductor MTM15N50. Note that there are
three distinct slopes to the curve representing different
input capacitance values. To completely switch the
MOSFET ‘on,’ the gate must be brought to 10 V with
respect to the source. The graph shows that a gate charge \( Q_g \) of 110 nC is required when operating the MOSFET with
a drain to source voltage \( V_{DS} \) of 400 V.

---

[Figure 17. Gate−to−Source Voltage versus Gate charge]

The capacitive load power dissipation is directly related to
the required gate charge, and operating frequency. The
capacitive load power dissipation per driver is:

\[
P_{C(MOSFET)} = V_{CC} Q_{g} f
\]

The flat region from 10 nC to 55 nC is caused by the
drain−to−gate Miller capacitance, occurring while the
MOSFET is in the linear region dissipating substantial
amounts of power. The high output current capability of the
MC34152 is able to quickly deliver the required gate
current for fast power efficient MOSFET switching. By
operating the MC34152 at a higher VCC, additional charge
can be provided to bring the gate above 10 V. This will
reduce the ‘on’ resistance of the MOSFET at the expense
of higher driver dissipation at a given operating frequency.

The transition power dissipation is due to extremely
short simultaneous conduction of internal circuit nodes
when the Drive Outputs change state. The transition power
dissipation per driver is approximately:

\[
P_T = V_{CC} (1.08 V_{CC} C_L f − 8 \times 10^{-4})
\]

\( P_T \) must be greater than zero.

Switching time characterization of the MC34152 is
performed with fixed capacitive loads. Figure 13 shows
that for small capacitance loads, the switching speed is
limited by transistor turn–on/off time and the slew rate of
the internal nodes. For large capacitance loads, the
switching speed is limited by the maximum output current
capability of the integrated circuit.
High frequency printed circuit layout techniques are imperative to prevent excessive output ringing and overshoot. **Do not attempt to construct the driver circuit on wire-wrap or plug-in prototype boards.** When driving large capacitive loads, the printed circuit board must contain a low inductance ground plane to minimize the voltage spikes induced by the high ground ripple currents. All high current loops should be kept as short as possible using heavy copper runs to provide a low impedance high frequency path. For optimum drive performance, it is recommended that the initial circuit design contains dual power supply bypass capacitors connected with short leads as close to the VCC pin and ground as the layout will permit. Suggested capacitors are a low inductance 0.1 \( \mu \)F ceramic in parallel with a 4.7 \( \mu \)F tantalum. Additional bypass capacitors may be required depending upon Drive Output loading and circuit layout.

Proper printed circuit board layout is extremely critical and cannot be over emphasized.

The MC34152 greatly enhances the drive capabilities of common switching regulators and CMOS/TTL logic devices.

**Figure 18. Enhanced System Performance with Common Switching Regulators**

**Figure 19. MOSFET Parasitic Oscillations**

Series gate resistor \( R_g \) may be needed to damp high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit. \( R_g \) will decrease the MOSFET switching speed. Schottky diode \( D_1 \) can reduce the driver’s power dissipation due to excessive ringing, by preventing the output pin from being driven below ground.

**Figure 20. Direct Transformer Drive**

**Figure 21. Isolated MOSFET Drive**

Output Schottky diodes are recommended when driving inductive loads at high frequencies. The diodes reduce the driver’s power dissipation by preventing the output pins from being driven above VCC and below ground.
In noise sensitive applications, both conducted and radiated EMI can be reduced significantly by controlling the MOSFET’s turn-on and turn-off times.

Figures 22. Controlled MOSFET Drive

The totem-pole outputs can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C1.

Figures 23. Bipolar Transistor Drive

The capacitor’s equivalent series resistance limits the Drive Output Current to 1.5 A. An additional series resistor may be required when using tantalum or other low ESR capacitors.

Figures 24. Dual Charge Pump Converter

<table>
<thead>
<tr>
<th>$I_O$ (mA)</th>
<th>$+V_O$ (V)</th>
<th>$-V_O$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>27.7</td>
<td>-13.3</td>
</tr>
<tr>
<td>1.0</td>
<td>27.4</td>
<td>-12.9</td>
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<tr>
<td>10</td>
<td>26.4</td>
<td>-11.9</td>
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<td>20</td>
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<td>30</td>
<td>24.6</td>
<td>-10.5</td>
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<td>50</td>
<td>22.6</td>
<td>-9.4</td>
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</table>

Output Load Regulation
## ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package</th>
<th>Shipping†</th>
</tr>
</thead>
<tbody>
<tr>
<td>MC34152DG</td>
<td>SOIC−8 (Pb−Free)</td>
<td>98 Units / Rail</td>
</tr>
<tr>
<td>MC34152DR2G</td>
<td>SOIC−8 (Pb−Free)</td>
<td>2500 Tape &amp; Reel</td>
</tr>
<tr>
<td>MC34152PG</td>
<td>PDIP−8 (Pb−Free)</td>
<td>50 Units / Rail</td>
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<tr>
<td>MC33152DG</td>
<td>SOIC−8 (Pb−Free)</td>
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<td>MC33152VDR2G</td>
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<td>NCV33152DR2G*</td>
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<td>2500 Tape &amp; Reel</td>
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</tbody>
</table>

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV prefix is for automotive and other applications requiring site and change control.
NOTES:
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACK-
   AGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH
   OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE
   NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM
   PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR
   TO DATUM C.
6. DIMENSION b2 IS MEASURED AT THE LEAD TIPS WITH THE
   LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE
   LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE
   CORNERS).

<table>
<thead>
<tr>
<th>INCHES</th>
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<td>L</td>
<td>0.355</td>
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<td>M</td>
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**Style 1**:
1. **Pin 1.** AC In
2. **DC + In**
3. **DC – In**
4. **AC In**
5. **Ground**
6. **Output**
7. **Auxiliary**
8. **VCC**

**MARKING DIAGRAM**

XXXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present.

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www.onsemi.com
**NOTES:**

2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

**GENERAL MARKING DIAGRAM***

**SOLDERING FOOTPRINT***

For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**STYLES ON PAGE 2**
### STYLE 1:
- **PIN 1. Emitter**
- **2. Collector**
- **3. Collector**
- **4. Emitter**
- **5. Emitter**
- **6. Base**
- **7. Base**
- **8. Emitter**

### STYLE 2:
- **PIN 1. Collector, Die #1**
- **2. Collector, #1**
- **3. Collector, #2**
- **4. Collector, #2**
- **5. Emitter, #2**
- **6. Emitter, #2**
- **7. Base, #1**
- **8. Emitter, #1**

### STYLE 3:
- **PIN 1. Drain, Die #1**
- **2. Drain, #1**
- **3. Drain, #2**
- **4. Drain, #2**
- **5. Emitter, #2**
- **6. Source, #2**
- **7. Gate, #1**
- **8. Source, #1**

### STYLE 4:
- **PIN 1. Anode**
- **2. Base, #1**
- **3. Anode**
- **4. Anode**
- **5. Collector, #2**
- **6. Collector, #2**
- **7. Emitter, #2**
- **8. Common Cathode**

### STYLE 5:
- **PIN 1. Drain**
- **2. Drain**
- **3. Drain**
- **4. Drain**
- **5. Gate**
- **6. Gate**
- **7. Source**
- **8. Source**

### STYLE 6:
- **PIN 1. Source**
- **2. Drain**
- **3. Drain**
- **4. Source**
- **5. Source**
- **6. Gate**
- **7. Gate**
- **8. Source**

### STYLE 7:
- **PIN 1. Input**
- **2. External Bypass**
- **3. Third Stage Source**
- **4. Ground**
- **5. Drain**
- **6. Gate**
- **7. First Stage Vd**
- **8. Collector, #1**

### STYLE 8:
- **PIN 1. Collector, Die #1**
- **2. Base, #1**
- **3. Collector, #2**
- **4. Collector, #2**
- **5. Emitter, #2**
- **6. Emitter, #2**
- **7. Collector, #1**
- **8. Collector, #1**

### STYLE 9:
- **PIN 1. Emitter, Common**
- **2. Collector, Die #1**
- **3. Collector, Die #2**
- **4. Emitter, Common**
- **5. Emitter, Common**
- **6. Base, Die #2**
- **7. Base, Die #1**
- **8. Emitter, Common**

### STYLE 10:
- **PIN 1. Ground**
- **2. Bias 1**
- **3. Output**
- **4. Ground**
- **5. Ground**
- **6. Bias 2**
- **7. Input**
- **8. Drain**

### STYLE 11:
- **PIN 1. Source 1**
- **2. Gate 1**
- **3. Source 2**
- **4. Gate 2**
- **5. Drain 2**
- **6. Drain 2**
- **7. Drain 1**
- **8. Drain 1**

### STYLE 12:
- **PIN 1. Source**
- **2. Source**
- **3. Source**
- **4. Source**
- **5. Drain**
- **6. Drain**
- **7. Drain**
- **8. Drain**

### STYLE 13:
- **PIN 1. C.C.**
- **2. Source**
- **3. Source**
- **4. Gate**
- **5. Drain**
- **6. Drain**
- **7. Drain**
- **8. Drain**

### STYLE 14:
- **PIN 1. N-Source**
- **2. Source**
- **3. P-Source**
- **4. P-Gate**
- **5. P-Drain**
- **6. P-Drain**
- **7. N-Drain**
- **8. N-Drain**

### STYLE 15:
- **PIN 1. Anode**
- **2. Anode**
- **3. Anode**
- **4. Anode**
- **5. Cathode, Common**
- **6. Cathode, Common**
- **7. Cathode, Common**
- **8. Cathode, Common**

### STYLE 16:
- **PIN 1. Emitter, Die #1**
- **2. Base, Die #1**
- **3. Emitter, Die #2**
- **4. Base, Die #2**
- **5. Collector, Die #2**
- **6. Collector, Die #2**
- **7. Collector, Die #1**
- **8. Collector, Die #1**

### STYLE 17:
- **PIN 1. Vcc**
- **2. V2Out**
- **3. V1Out**
- **4. Txe**
- **5. Rxe**
- **6. Vee**
- **7. Gnd**
- **8. Acc**

### STYLE 18:
- **PIN 1. Anode**
- **2. Anode**
- **3. Anode**
- **4. Anode**
- **5. Cathode, Common**
- **6. Cathode, Common**
- **7. Cathode, Common**
- **8. Cathode, Common**

### STYLE 19:
- **PIN 1. Source (N)**
- **2. Gate (N)**
- **3. Source (P)**
- **4. Gate (P)**
- **5. Drain**
- **6. Drain**
- **7. Drain**
- **8. Drain**

### STYLE 20:
- **PIN 1. Source (N)**
- **2. Gate 1**
- **3. Source 2**
- **4. Gate 2**
- **5. Drain 2**
- **6. Mirror 2**
- **7. Drain 1**
- **8. Mirror 1**

### STYLE 21:
- **PIN 1. Cathode 1**
- **2. Cathode 2**
- **3. Cathode 3**
- **4. Cathode 4**
- **5. Cathode 5**
- **6. Common Anode**
- **7. Common Anode**
- **8. Cathode 6**

### STYLE 22:
- **PIN 1. I/O Line 1**
- **2. Common Cathode/Vcc**
- **3. Common Cathode/Vcc**
- **4. I/O Line 3**
- **5. Common Anode/Gnd**
- **6. I/O Line 4**
- **7. Common Anode/Gnd**
- **8. Common Anode/Gnd**

### STYLE 23:
- **PIN 1. Line 1 IN**
- **2. Common Anode/Gnd**
- **3. Common Anode/Gnd**
- **4. Line 2 IN**
- **5. Line 2 OUT**
- **6. Common Anode/Gnd**
- **7. Common Anode/Gnd**
- **8. Line 1 OUT**

### STYLE 24:
- **PIN 1. Base**
- **2. Emitter**
- **3. Collector/Anode**
- **4. Collector/Anode**
- **5. Cathode**
- **6. Cathode**
- **7. Collector/Anode**
- **8. Collector/Anode**

### STYLE 25:
- **PIN 1. Vin**
- **2. N/C**
- **3. Rext**
- **4. Gnd**
- **5. IOut**
- **6. IOut**
- **7. IOut**
- **8. IOC**

### STYLE 26:
- **PIN 1. Gnd**
- **2. IO Lim**
- **3. Enable**
- **4. I/O Lim**
- **5. Source**
- **6. Source**
- **7. Source**
- **8. Drain**

### STYLE 27:
- **PIN 1. Ilimit**
- **2. Sw To Gnd**
- **3. Dasic Off**
- **4. Dasic Sw Det**
- **5. V_Mon**
- **6. V_Bulk**
- **7. V_Bulk**
- **8. Vin**

### STYLE 28:
- **PIN 1. Sw To Gnd**
- **2. Dasic Off**
- **3. Dasic Sw Det**
- **4. Gnd**
- **5. V_Mon**
- **6. V_Bulk**
- **7. V_Bulk**
- **8. Vin**

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**PAGE:** 2 OF 2

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