Single Supply 3.0 V to 44 V Operational Amplifiers

MC34071,2,4,A
MC33071,2,4,A,
NCV33072,4,A

Quality bipolar fabrication with innovative design concepts are employed for the MC33071/72/74, MC34071/72/74, NCV33072/74A series of monolithic operational amplifiers. This series of operational amplifiers offer 4.5 MHz of gain bandwidth product, 13 V/μs slew rate and fast settling time without the use of JFET device technology. Although this series can be operated from split supplies, it is particularly suited for single supply operation, since the common mode input voltage range includes ground potential (VEE). With a Darlington input stage, this series exhibits high input resistance, low input offset voltage and high gain. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, provides high capacitance drive capability, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source/sink AC frequency response.

The MC33071/72/74, MC34071/72/74, NCV33072/74,A series of devices are available in standard or prime performance (A Suffix) grades and are specified over the commercial, industrial/vehicular or military temperature ranges. The complete series of single, dual and quad operational amplifiers are available in plastic SOIC, QFN and TSSOP surface mount packages.

Features
- Wide Bandwidth: 4.5 MHz
- High Slew Rate: 13 V/μs
- Fast Settling Time: 1.1 μs to 0.1%
- Wide Single Supply Operation: 3.0 V to 44 V
- Wide Input Common Mode Voltage Range: Includes Ground (VEE)
- Low Input Offset Voltage: 3.0 mV Maximum (A Suffix)
- Large Output Voltage Swing: −14.7 V to +14 V (with ±15 V Supplies)
- Large Capacitance Drive Capability: 0 pF to 10,000 pF
- Low Total Harmonic Distortion: 0.02%
- Excellent Phase Margin: 60°
- Excellent Gain Margin: 12 dB
- Output Short Circuit Protection
- ESD Diodes/Clamps Provide Input Protection for Dual and Quad
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant
Figure 1. Representative Schematic Diagram
(Each Amplifier)
MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (from $V_{EE}$ to $V_{CC}$)</td>
<td>$V_S$</td>
<td>+44</td>
<td>V</td>
</tr>
<tr>
<td>Input Differential Voltage Range</td>
<td>$V_{IDR}$</td>
<td>(Note 1)</td>
<td>V</td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td>$V_{IR}$</td>
<td>(Note 1)</td>
<td>V</td>
</tr>
<tr>
<td>Output Short Circuit Duration (Note 2)</td>
<td>$t_{SC}$</td>
<td>Indefinite</td>
<td>Sec</td>
</tr>
<tr>
<td>Operating Junction Temperature</td>
<td>$T_J$</td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$T_{stg}$</td>
<td>–60 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>ESD Capability, Dual and Quad (Note 3)</td>
<td>$ESD_{HBM}$</td>
<td>2000</td>
<td>V</td>
</tr>
<tr>
<td>Human Body Model</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Machine Model</td>
<td>$ESD_{MM}$</td>
<td>200</td>
<td></td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Either or both input voltages should not exceed the magnitude of $V_{CC}$ or $V_{EE}$.
2. Power dissipation must be considered to ensure maximum junction temperature ($T_J$) is not exceeded (see Figure 2).
3. This device series incorporates ESD protection and is tested by the following methods:
   - ESD Human Body Model tested per AEC–Q100–002 (JEDEC standard: JESD22–A114)
   - ESD Machine Model tested per AEC–Q100–003 (JEDEC standard: JESD22–A115)
<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>A Suffix</th>
<th>Non-Suffix</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Offset Voltage ((R_S = 100 \Omega, V_{CM} = 0 \mathrm{V}, V_O = 0 \mathrm{V})) (V_{CC} = +15 \mathrm{V}, V_{EE} = -15 \mathrm{V}, V_O = 0 \mathrm{V}), (T_A = T_{low} \to T_{high})</td>
<td>(V_{IO})</td>
<td>Min</td>
<td>Typ</td>
</tr>
<tr>
<td>Average Temperature Coefficient of Input Offset Voltage (R_S = 10 \Omega, V_{CM} = 0 \mathrm{V}, V_O = 0 \mathrm{V}), (T_A = T_{low} \to T_{high})</td>
<td>(\Delta V_{IO}/\Delta T)</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Input Bias Current ((V_{CM} = 0 \mathrm{V}, V_O = 0 \mathrm{V})) (T_A = +25\degree\mathrm{C}), (T_A = T_{low} \to T_{high})</td>
<td>(I_{IB})</td>
<td>-</td>
<td>100</td>
</tr>
<tr>
<td>Input Offset Current ((V_{CM} = 0 \mathrm{V}, V_O = 0 \mathrm{V})) (T_A = +25\degree\mathrm{C}), (T_A = T_{low} \to T_{high})</td>
<td>(I_{IO})</td>
<td>-</td>
<td>6.0</td>
</tr>
<tr>
<td>Input Common Mode Voltage Range (T_A = +25\degree\mathrm{C}), (T_A = T_{low} \to T_{high})</td>
<td>(V_{ICR})</td>
<td>(V_{EE} \to (V_{CC} - 1.8))</td>
<td>(V_{EE} \to (V_{CC} - 2.2))</td>
</tr>
<tr>
<td>Large Signal Voltage Gain ((V_O = \pm 10 \mathrm{V}, R_L = 2.0 \mathrm{k}\Omega)) (T_A = +25\degree\mathrm{C}), (T_A = T_{low} \to T_{high})</td>
<td>(A_{VOL})</td>
<td>50</td>
<td>100</td>
</tr>
<tr>
<td>Output Voltage Swing ((V_{ID} = \pm 1.0 \mathrm{V})) (V_{CC} = +5.0 \mathrm{V}, V_{EE} = 0 \mathrm{V}, R_L = 2.0 \mathrm{k}\Omega, T_A = +25\degree\mathrm{C}) (V_{CC} = +15 \mathrm{V}, V_{EE} = -15 \mathrm{V}, R_L = 10 \mathrm{k}\Omega, T_A = +25\degree\mathrm{C}) (V_{CC} = +15 \mathrm{V}, V_{EE} = -15 \mathrm{V}, R_L = 2.0 \mathrm{k}\Omega, T_A = T_{low} \to T_{high})</td>
<td>(V_{OH})</td>
<td>-</td>
<td>3.7</td>
</tr>
<tr>
<td>Output Short Circuit Current ((V_{ID} = 1.0 \mathrm{~V}, V_O = 0 \mathrm{~V}, T_A = 25\degree\mathrm{C})) (V_{CC} = +5.0 \mathrm{~V}, V_{EE} = 0 \mathrm{~V}, R_L = 2.0 \mathrm{k}\Omega, T_A = +25\degree\mathrm{C}) (V_{CC} = +15 \mathrm{~V}, V_{EE} = -15 \mathrm{~V}, R_L = 10 \mathrm{k}\Omega, T_A = +25\degree\mathrm{C}) (V_{CC} = +15 \mathrm{~V}, V_{EE} = -15 \mathrm{~V}, R_L = 2.0 \mathrm{k}\Omega, T_A = T_{low} \to T_{high})</td>
<td>(I_{SC})</td>
<td>Source</td>
<td>10</td>
</tr>
<tr>
<td>Common Mode Rejection (R_S \leq 10 \mathrm{k}\Omega, V_{CM} = V_{ICR}, T_A = 25\degree\mathrm{C})</td>
<td>CMR</td>
<td>80</td>
<td>97</td>
</tr>
<tr>
<td>Power Supply Rejection ((R_S = 100 \Omega)) (V_{CC}/V_{EE} = +16.5 \mathrm{~V}/-16.5 \mathrm{~V} \to +13.5 \mathrm{~V}/-13.5 \mathrm{~V}, T_A = 25\degree\mathrm{C})</td>
<td>PSR</td>
<td>80</td>
<td>97</td>
</tr>
<tr>
<td>Power Supply Current (Per Amplifier, No Load) (V_{CC} = +5.0 \mathrm{~V}, V_{EE} = 0 \mathrm{~V}, V_O = +2.5 \mathrm{~V}, T_A = +25\degree\mathrm{C}) (V_{CC} = +15 \mathrm{~V}, V_{EE} = -15 \mathrm{~V}, V_O = 0 \mathrm{~V}, T_A = +25\degree\mathrm{C}) (V_{CC} = +15 \mathrm{~V}, V_{EE} = -15 \mathrm{~V}, V_O = 0 \mathrm{~V}, T_A = T_{low} \to T_{high})</td>
<td>(I_D)</td>
<td>-</td>
<td>1.6</td>
</tr>
<tr>
<td>(T_{low} = -40\degree\mathrm{C} \quad \text{for MC33071,2,4/A, NCV33074/A} \quad T_{high} = +85\degree\mathrm{C} \quad \text{for MC33071,2,4/A, NCV33074/A} ) (= 0\degree\mathrm{C} \quad \text{for MC34071,2,4/A} \quad \text{MC34072,4/V, NCV33072,4A, NCV34074V} ) (= -40\degree\mathrm{C} \quad \text{for MC34072,4/V, NCV33072,4A} \quad = +125\degree\mathrm{C} \quad \text{for MC34072,4/V, NCV33072,4A, NCV34074V} ) Case 510AJ (T_{low}/T_{high}) guaranteed by product characterization.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. \(T_{low} = -40\degree\mathrm{C} \quad \text{for MC33071,2,4/A, NCV33074/A} \quad T_{high} = +85\degree\mathrm{C} \quad \text{for MC33071,2,4/A, NCV33074/A} \) 
\(= 0\degree\mathrm{C} \quad \text{for MC34071,2,4/A} \quad \text{MC34072,4/V, NCV33072,4A, NCV34074V} \) 
\(= -40\degree\mathrm{C} \quad \text{for MC34072,4/V, NCV33072,4A} \quad = +125\degree\mathrm{C} \quad \text{for MC34072,4/V, NCV33072,4A, NCV34074V} \)
AC ELECTRICAL CHARACTERISTICS (VCC = +15 V, VEE = −15 V, RL = connected to ground. TA = +25°C, unless otherwise noted.)

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>A Suffix</th>
<th>Non–Suffix</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
</tr>
<tr>
<td>Slew Rate (Vin = −10 V to +10 V, RL = 2.0 kΩ, C_L = 500 pF)</td>
<td>SR</td>
<td>8.0</td>
<td>10</td>
</tr>
<tr>
<td>AV = +1.0</td>
<td></td>
<td>–</td>
<td>13</td>
</tr>
<tr>
<td>AV = −1.0</td>
<td></td>
<td>–</td>
<td>2.2</td>
</tr>
<tr>
<td>Setting Time (10 V Step, AV = −1.0)</td>
<td>ts</td>
<td>–</td>
<td>1.1</td>
</tr>
<tr>
<td>To 0.1% (+1/2 LSB of 9–Bits)</td>
<td></td>
<td>–</td>
<td>2.2</td>
</tr>
<tr>
<td>To 0.01% (+1/2 LSB of 12–Bits)</td>
<td></td>
<td>–</td>
<td>2.2</td>
</tr>
<tr>
<td>Gain Bandwidth Product (f = 100 kHz)</td>
<td>GBW</td>
<td>3.5</td>
<td>4.5</td>
</tr>
<tr>
<td>Power Bandwidth</td>
<td>BW</td>
<td>–</td>
<td>160</td>
</tr>
<tr>
<td>AV = +1.0, RL = 2.0 kΩ</td>
<td></td>
<td>–</td>
<td>60</td>
</tr>
<tr>
<td>RL = 2.0 kΩ</td>
<td></td>
<td>–</td>
<td>40</td>
</tr>
<tr>
<td>Phase margin</td>
<td>fm</td>
<td>–</td>
<td>12</td>
</tr>
<tr>
<td>R_L = 2.0 kΩ</td>
<td></td>
<td>–</td>
<td>4.0</td>
</tr>
<tr>
<td>Gain Margin</td>
<td>Am</td>
<td>–</td>
<td>32</td>
</tr>
<tr>
<td>R_L = 2.0 kΩ</td>
<td></td>
<td>–</td>
<td>4.0</td>
</tr>
<tr>
<td>Equivalent Input Noise Voltage</td>
<td>e_in</td>
<td>–</td>
<td>0.22</td>
</tr>
<tr>
<td>R_S = 100 Ω, f = 1.0 kHz</td>
<td></td>
<td>–</td>
<td>0.22</td>
</tr>
<tr>
<td>Equivalent Input Noise Current</td>
<td>l_in</td>
<td>–</td>
<td>0.22</td>
</tr>
<tr>
<td>f = 1.0 kHz</td>
<td></td>
<td>–</td>
<td>0.22</td>
</tr>
<tr>
<td>Differential Input Resistance</td>
<td>R_in</td>
<td>–</td>
<td>150</td>
</tr>
<tr>
<td>V_CM = 0 V</td>
<td></td>
<td>–</td>
<td>2.5</td>
</tr>
<tr>
<td>Differential Input Capacitance</td>
<td>C_in</td>
<td>–</td>
<td>0.02</td>
</tr>
<tr>
<td>V_CM = 0 V</td>
<td></td>
<td>–</td>
<td>0.02</td>
</tr>
<tr>
<td>Total Harmonic Distortion</td>
<td>THD</td>
<td>–</td>
<td>0.02</td>
</tr>
<tr>
<td>AV = +10, RL = 2.0 kΩ, 2.0 V_pp ≤ V_O ≤ 20 V_pp, f = 10 kHz</td>
<td></td>
<td>–</td>
<td>120</td>
</tr>
<tr>
<td>Channel Separation (f = 10 kHz)</td>
<td></td>
<td>–</td>
<td>30</td>
</tr>
<tr>
<td>Open Loop Output Impedance (f = 1.0 MHz)</td>
<td></td>
<td>–</td>
<td>30</td>
</tr>
</tbody>
</table>

![Figure 2. Power Supply Configurations](image1)

![Figure 3. Offset Null Circuit](image2)

Offset nulling range is approximately ±80 mV with a 10 kΩ potentiometer (MC33071, MC34071 only).
Figure 4. Maximum Power Dissipation versus Temperature for Package Types

Figure 5. Input Offset Voltage versus Temperature for Representative Units

Figure 6. Input Common Mode Voltage Range versus Temperature

Figure 7. Normalized Input Bias Current versus Temperature

Figure 8. Normalized Input Bias Current versus Input Common Mode Voltage

Figure 9. Split Supply Output Voltage Swing versus Supply Voltage
Figure 10. Split Supply Output Saturation versus Load Current

Figure 11. Single Supply Output Saturation versus Load Resistance to Ground

Figure 12. Single Supply Output Saturation versus Load Resistance to VCC

Figure 13. Output Short Circuit Current versus Temperature

Figure 14. Output Impedance versus Frequency

Figure 15. Output Voltage Swing versus Frequency
Figure 16. Total Harmonic Distortion versus Frequency

Figure 17. Total Harmonic Distortion versus Output Voltage Swing

Figure 18. Open Loop Voltage Gain versus Temperature

Figure 19. Open Loop Voltage Gain and Phase versus Frequency

Figure 20. Open Loop Voltage Gain and Phase versus Frequency

Figure 21. Normalized Gain Bandwidth Product versus Temperature
Figure 22. Percent Overshoot versus Load Capacitance

Figure 23. Phase Margin versus Load Capacitance

Figure 24. Gain Margin versus Load Capacitance

Figure 25. Phase Margin versus Temperature

Figure 26. Gain Margin versus Temperature

Figure 27. Phase Margin and Gain Margin versus Differential Source Resistance
Figure 28. Normalized Slew Rate versus Temperature

Figure 29. Output Settling Time

Figure 30. Small Signal Transient Response

Figure 31. Large Signal Transient Response

Figure 32. Common Mode Rejection versus Frequency

Figure 33. Power Supply Rejection versus Frequency
Although the bandwidth, slew rate, and settling time of the MC34071 amplifier series are similar to op amp products utilizing JFET input devices, these amplifiers offer other additional distinct advantages as a result of the PNP transistor differential input stage and an all NPN transistor output stage.

Since the input common mode voltage range of this input stage includes the VEE potential, single supply operation is feasible to as low as 3.0 V with the common mode input voltage at ground potential.

The input stage also allows differential input voltages up to ±44 V, provided the maximum input voltage range is not exceeded. Specifically, the input voltages must range between VEE and VCC supply voltages as shown by the maximum rating table. In practice, although not recommended, the input voltages can exceed the VCC voltage by approximately 3.0 V and decrease below the VEE voltage by 0.3 V without causing product damage, although output phase reversal may occur. It is also possible to source up to approximately 5.0 mA of current from VEE through either inputs clamping diode without damage or latching, although phase reversal may again occur.

If one or both inputs exceed the upper common mode voltage limit, the amplifier output is readily predictable and may be in a low or high state depending on the existing input bias conditions.

Since the input capacitance associated with the small geometry input device is substantially lower (2.5 pF) than the typical JFET input gate capacitance (5.0 pF), better frequency response for a given input source resistance can be achieved using the MC34071 series of amplifiers. This performance feature becomes evident, for example, in fast settling D−to−A current to voltage conversion applications where the feedback resistance can form an input pole with the input capacitance of the op amp. This input pole creates a 2nd order system with the single pole op amp and is therefore detrimental to its settling time. In this context, lower input capacitance is desirable especially for higher
values of feedback resistances (lower current DACs). This input pole can be compensated for by creating a feedback zero with a capacitance across the feedback resistance, if necessary, to reduce overshoot. For 2.0 kΩ of feedback resistance, the MC34071 series can settle to within 1/2 LSB of 8–bits in 1.0 µs, and within 1/2 LSB of 12–bits in 2.2 µs for a 10 V step. In an inverting unity gain fast settling configuration, the symmetrical slew rate is ±13 V/µs. In the classic noninverting unity gain configuration, the output positive slew rate is +10 V/µs, and the corresponding negative slew rate will exceed the positive slew rate as a function of the fall time of the input waveform.

Since the bipolar input device matching characteristics are superior to that of JFETs, a low untrimmed maximum offset voltage of 3.0 mV prime and 5.0 mV downgrade can be economically offered with high frequency performance characteristics. This combination is ideal for low cost precision, high speed quad op amp applications.

The all NPN output stage, shown in its basic form on the equivalent circuit schematic, offers unique advantages over the more conventional NPN/PNP transistor Class AB output stage. A 10 kΩ output stage can swing within 1.0 V of the positive rail (VCC), and within 0.3 V of the negative rail (VEE), providing a 28.7 Vpp swing from ±15 V supplies. This large output swing becomes most noticeable at lower supply voltages.

The positive swing is limited by the saturation voltage of the current source transistor Q7, and VBE of the NPN pull up transistor Q17, and the voltage drop associated with the short circuit resistance, R7. The negative swing is limited by the saturation voltage of the pull–down transistor Q16, the voltage drop I LR6, and the voltage drop associated with the short circuit resistance R7, where IL is the sink load current. For small valued sink currents, the above voltage drops are negligible, allowing the negative swing voltage to approach within millivolts of VEE. For large valued sink currents (>5.0 mA), diode D3 clamps the voltage across R6, thus limiting the negative swing to the saturation voltage of Q16, plus the forward diode drop of D3 (=VEE +1.0 V). Thus for a given supply voltage, unprecedented peak–to–peak output voltage swing is possible as indicated by the output swing specifications.

If the load resistance is referenced to VCC instead of ground for single supply applications, the maximum possible output swing can be achieved for a given supply voltage. For light load currents, the load resistance will pull the output to VCC during the positive swing and the output will pull the load resistance near ground during the negative swing. The load resistance value should be much less than that of the feedback resistance to maximize pull up capability.

Because the PNP output emitter–follower transistor has been eliminated, the MC34071 series offers a 20 mA minimum current sink capability, typically to an output voltage of (VEE +1.8 V). In single supply applications the output can directly source or sink base current from a common emitter NPN transistor for fast high current switching applications.

In addition, the all NPN transistor output stage is inherently fast, contributing to the bipolar amplifier’s high gain bandwidth product and fast settling capability. The associated high frequency low output impedance (30 Ω typ @ 1.0 MHz) allows capacitive drive capability from 0 pF to 10,000 pF without oscillation in the unity closed loop gain configuration. The 60° phase margin and 12 dB gain margin as well as the general gain and phase characteristics are virtually independent of the source/sink output swing conditions. This allows easier system phase compensation, since output swing will not be a phase consideration. The high frequency characteristics of the MC34071 series also allow excellent high frequency active filter capability, especially for low voltage single supply applications.

Although the single supply specifications is defined at 5.0 V, these amplifiers are functional to 3.0 V @ 25°C although slight changes in parametrics such as bandwidth, slew rate, and DC gain may occur.

If power to this integrated circuit is applied in reverse polarity or if the IC is installed backwards in a socket, large unlimited current surges will occur through the device that may result in device destruction.

Special static precautions are not necessary for these bipolar amplifiers since there are no MOS transistors on the die.

As with most high frequency amplifiers, proper lead dress, component placement, and PC board layout should be exercised for optimum frequency performance. For example, long unshielded input or output leads may result in unwanted input–output coupling. In order to preserve the relatively low input capacitance associated with these amplifiers, resistors connected to the inputs should be immediately adjacent to the input pin to minimize additional stray input capacitance. This not only minimizes the input pole for optimum frequency response, but also minimizes extraneous “pick up” at this node. Supply decoupling with adequate capacitance immediately adjacent to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit great impedance changes over temperature.

The output of any one amplifier is current limited and thus protected from a direct short to ground. However, under such conditions, it is important not to allow the device to exceed the maximum junction temperature rating. Typically for ±15 V supplies, any one output can be shorted continuously to ground without exceeding the maximum temperature rating.
Figure 38. AC Coupled Noninverting Amplifier

Figure 39. AC Coupled Inverting Amplifier

Figure 40. DC Coupled Inverting Amplifier

Figure 41. Unity Gain Buffer TTL Driver

Figure 42. Active High-Q Notch Filter

Figure 43. Active Bandpass Filter
Figure 44. Low Voltage Fast D/A Converter

Figure 45. High Speed Low Voltage Comparator

Figure 46. LED Driver

Figure 47. Transistor Driver

Figure 48. AC/DC Ground Current Monitor

Figure 49. Photovoltaic Cell Amplifier
Figure 50. Low Input Voltage Comparator with Hysteresis

\[ V_{\text{inL}} = \frac{R_1}{R_1 + R_2} (V_{\text{OL}} - V_{\text{ref}}) + V_{\text{ref}} \]
\[ V_{\text{inH}} = \frac{R_1}{R_1 + R_2} (V_{\text{OH}} - V_{\text{ref}}) + V_{\text{ref}} \]
\[ V_H = R_1 \left( \frac{V_{\text{OH}} - V_{\text{OL}}}{R_1 + R} \right) \]

Figure 51. High Compliance Voltage to Sink Current Converter

\[ I_{\text{out}} = \frac{V_{\text{P}+} - V_{\text{IO}}}{R} \]

Figure 52. High Input Impedance Differential Amplifier

\[ R_2 \frac{R_1}{R_1 + R_3} \quad \text{(Critical to CMRR)} \]
\[ V_0 = 1 \left( \frac{R_4}{R_3} \right) \left( V_{\text{P}+} - V_{\text{V1}} \right) \frac{R_4}{R_3} \]
For \( V_{\text{P}+} \geq V_{\text{V1}} \), \( V > 0 \)

Figure 53. Bridge Current Amplifier

\[ t_{\text{OSC}} = \frac{0.85}{R C} \]
\[ + + I_B \quad I_{\text{SC}} \]
\[ + + V_P \quad V_P \quad V_P \]
\[ t_{\text{OSC}} \]
\[ 0 \quad \text{Base Charge Removal} \]
\[ + \quad I_{\text{B}} \quad I_{\text{SC}} \]
\[ + \quad I_{\text{B}} \quad I_{\text{SC}} \]

Figure 54. Low Voltage Peak Detector

Figure 55. High Frequency Pulse Width Modulation
MC34071,2,4,A MC33071,2,4,A, NCV33072,4,A

GENERAL ADDITIONAL APPLICATIONS INFORMATION $V_S = \pm 15.0 \text{ V}$

**Figure 56. Second Order Low−Pass Active Filter**

![Low−Pass Active Filter Circuit](image)

Choose: $f_0$, $H_0$, $C_2$

Then: $C_1 = 2C_2 (H_0+1)$

**Figure 57. Second Order High−Pass Active Filter**

![High−Pass Active Filter Circuit](image)

Choose: $f_0$, $H_0$, $C_1$

Then: $R_1 = \frac{H_0+0.5}{\pi f_0 C_1 \sqrt{2}}$

$R_2 = \frac{2\pi f_0 C_1 (1/H_0+2)}{C_2} = \frac{C}{H_0}$

**Figure 58. Fast Settling Inverter**

![Fast Settling Inverter Circuit](image)

Step $\text{RF}$

$V_0 = 10 \text{ V}$

Uncompensated

$\tau_s = 1.0 \mu \text{s}$

to 1/2 LSB (8-Bits)

Compensated

$\tau_s = 2.2 \mu \text{s}$

to 1/2 LSB (12-Bits)

SR = 13 V/µs

**Figure 59. Basic Inverting Amplifier**

![Basic Inverting Amplifier Circuit](image)

$V_0 = R_2 \left(\frac{R_1}{R_1 + R_2}\right) \frac{V_i}{V_i}$

BW (-3.0 dB) = $\frac{R_1}{R_1 + R_2}$

SR = 13 V/µs

**Figure 60. Basic Noninverting Amplifier**

![Basic Noninverting Amplifier Circuit](image)

$\frac{V_o}{V_i} = \left(1 + \frac{R_2}{R_1}\right)$

BW (-3.0 dB) = $\frac{R_1}{R_1 + R_2}$

SR = 10 V/µs

**Figure 61. Unity Gain Buffer ($A_V = +1.0$)**

![Unity Gain Buffer Circuit](image)

$SR = 13 \text{ V/µs}$

$BW_p = 200 \text{ kHz}$

$V_0 = 20 \text{ Vpp}$

SR = 10 V/µs

www.onsemi.com

16
Example:
Let: $R = R_E = 12 \, k$
Then: $A_V = 3.0$
$BW = 1.5 \, MHz$

$$A_V = 1 + \frac{R}{R_E}$$

Figure 62. High Impedance Differential Amplifier

<table>
<thead>
<tr>
<th>$R_L$</th>
<th>$+V_O$</th>
<th>$-V_O$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\infty$</td>
<td>18.93</td>
<td>-18.78</td>
</tr>
<tr>
<td>10 k</td>
<td>18</td>
<td>-18</td>
</tr>
<tr>
<td>5.0 k</td>
<td>15.4</td>
<td>-15.4</td>
</tr>
</tbody>
</table>

Figure 63. Dual Voltage Doubler
## ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Op Amp Function</th>
<th>Device</th>
<th>Operating Temperature Range</th>
<th>Package</th>
<th>Shipping†</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single</td>
<td>MC34071DR2G</td>
<td>$T_A = 0^\circ$ to +70°C</td>
<td>SOIC–8 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>MC33071DR2G</td>
<td>$T_A = -40^\circ$ to +85°C</td>
<td>SOIC–8 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>MC33071ADR2G</td>
<td></td>
<td>SOIC–8 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>MC34072DR2G</td>
<td>$T_A = 0^\circ$ to +70°C</td>
<td>SOIC–8 (Pb–Free)</td>
<td>2500 Units / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>MC34072ADR2G</td>
<td></td>
<td>SOIC–8 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>MC34072AMTBBG</td>
<td></td>
<td>WQFN10 (Pb–Free)</td>
<td>3000 Units / Tape &amp; Reel</td>
</tr>
<tr>
<td>Dual</td>
<td>MC33072DR2G</td>
<td>$T_A = -40^\circ$ to +85°C</td>
<td>SOIC–8 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>MC33072ADR2G</td>
<td></td>
<td>SOIC–8 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>MC34072VDR2G</td>
<td>$T_A = -40^\circ$ to +125°C</td>
<td>SOIC–8 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>NCV33072DR2G*</td>
<td></td>
<td>SOIC–8 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>MC34074ADR2G</td>
<td>$T_A = 0^\circ$ to +70°C</td>
<td>SOIC–14 (Pb–Free)</td>
<td>2500 Units / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>MC34074DR2G</td>
<td></td>
<td>SOIC–14 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>MC33074DR2G</td>
<td></td>
<td>SOIC–14 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>NCV33074DR2G*</td>
<td></td>
<td>SOIC–14 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>MC33074ADR2G</td>
<td></td>
<td>SOIC–14 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>NCV33074ADR2G*</td>
<td>$T_A = -40^\circ$ to +85°C</td>
<td>SOIC–14 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>MC33074DTBR2G</td>
<td></td>
<td>TSSOP–14 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>MC33074ADTBR2G</td>
<td></td>
<td>TSSOP–14 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>NCV33074ADTBR2G*</td>
<td></td>
<td>TSSOP–14 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>MC34074VDR2G</td>
<td>$T_A = -40^\circ$ to +125°C</td>
<td>SOIC–14 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>NCV34074VDR2G*</td>
<td></td>
<td>SOIC–14 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
</tbody>
</table>

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV prefix for automotive and other applications requiring unique site and control change requirements; AEC–Q100 qualified and PPAP capable.
MARKING DIAGRAMS

SOIC-8
D SUFFIX
CASE 751

8
8
8
8

3x071
3x071
3x072
3x072

ALYW
ALYW
ALYW
ALYW

1
1
1
1

*applies to NCV33072DR2G

SOIC-14
D SUFFIX
CASE 751A

14
14
14
14

MC3x074DG
MC3x074ADG
MC34074VDG
MC33

AWLYWW
AWLYWW
AWLYWW
074

1
1
1
1

*applies to NCV34074VDR2G

TSSOP-14
DTB SUFFIX
CASE 948G

WQFN10
MT SUFFIX
CASE 510AJ

4072

AAYW


x = 3 or 4
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or * = Pb−Free Package
(Note: Microdot may be in either location)
NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION A APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

LOGICAL OR FUNCTIONAL TERMINAL ASSIGNMENT

<table>
<thead>
<tr>
<th>Terminal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>Terminal 1</td>
</tr>
<tr>
<td>A2</td>
<td>Terminal 2</td>
</tr>
<tr>
<td>A3</td>
<td>Terminal 3</td>
</tr>
<tr>
<td>A4</td>
<td>Terminal 4</td>
</tr>
<tr>
<td>A5</td>
<td>Terminal 5</td>
</tr>
<tr>
<td>A6</td>
<td>Terminal 6</td>
</tr>
<tr>
<td>A7</td>
<td>Terminal 7</td>
</tr>
<tr>
<td>A8</td>
<td>Terminal 8</td>
</tr>
<tr>
<td>A9</td>
<td>Terminal 9</td>
</tr>
<tr>
<td>A10</td>
<td>Terminal 10</td>
</tr>
</tbody>
</table>

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.*

**This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " *, may or may not be present.**
NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

<table>
<thead>
<tr>
<th>MILLIMETERS</th>
<th>INCHES</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>4.80</td>
</tr>
<tr>
<td>B</td>
<td>3.60</td>
</tr>
<tr>
<td>C</td>
<td>1.35</td>
</tr>
<tr>
<td>D</td>
<td>0.53</td>
</tr>
<tr>
<td>G</td>
<td>1.27</td>
</tr>
<tr>
<td>H</td>
<td>0.10</td>
</tr>
<tr>
<td>J</td>
<td>0.19</td>
</tr>
<tr>
<td>K</td>
<td>0.40</td>
</tr>
<tr>
<td>M</td>
<td>0</td>
</tr>
<tr>
<td>N</td>
<td>0.25</td>
</tr>
<tr>
<td>S</td>
<td>5.80</td>
</tr>
</tbody>
</table>

**SOLDERING FOOTPRINT**

**GENERIC MARKING DIAGRAM**

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "*", may or may not be present. Some products may not follow the Generic Marking.

**STYLES ON PAGE 2**
NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

SOLDERING FOOTPRINT*

XXXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "*, may or may not be present.

STYLES ON PAGE 2
SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELL ED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 4:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. ANODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON CATHODE
3. COMMON CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. COMMON CATHODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. COMMON CATHODE
13. NO CONNECTION
14. COMMON CATHODE

© Semiconductor Components Industries, LLC, 2019 www.onsemi.com
TSSOP–14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016

NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

SOLDERING FOOTPRINT

DIMENSIONS: MILLIMETERS

GROSS MARKING DIAGRAM*

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, ”G” or microdot “•”, may or may not be present.