Single Supply 3.0 V to 44 V Operational Amplifiers

MC34071,2,4,A
MC33071,2,4,A,
NCV33072,4,A

Quality bipolar fabrication with innovative design concepts are employed for the MC33071/72/74, MC34071/72/74, NCV33072/74A series of monolithic operational amplifiers. This series of operational amplifiers offer 4.5 MHz of gain bandwidth product, 13 V/µs slew rate and fast settling time without the use of JFET device technology. Although this series can be operated from split supplies, it is particularly suited for single supply operation, since the common mode input voltage range includes ground potential (V_{EE}). With a Darlington input stage, this series exhibits high input resistance, low input offset voltage and high gain. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, provides high capacitance drive capability, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source/sink AC frequency response.

The MC33071/72/74, MC34071/72/74, NCV33072/74A series of devices are available in standard or prime performance (A Suffix) grades and are specified over the commercial, industrial/vehicular or military temperature ranges. The complete series of single, dual and quad operational amplifiers are available in plastic SOIC, QFN and TSSOP surface mount packages.

Features
• Wide Bandwidth: 4.5 MHz
• High Slew Rate: 13 V/µs
• Fast Settling Time: 1.1 µs to 0.1%
• Wide Single Supply Operation: 3.0 V to 44 V
• Wide Input Common Mode Voltage Range: Includes Ground (V_{EE})
• Low Input Offset Voltage: 3.0 mV Maximum (A Suffix)
• Large Output Voltage Swing: −14.7 V to +14 V (with ±15 V Supplies)
• Large Capacitance Drive Capability: 0 pF to 10,000 pF
• Low Total Harmonic Distortion: 0.02%
• Excellent Phase Margin: 60°
• Excellent Gain Margin: 12 dB
• Output Short Circuit Protection
• ESD Diodes/Clamps Provide Input Protection for Dual and Quad
• NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
• These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

ORDERING INFORMATION
See detailed ordering and shipping information on page 18 of this data sheet.

DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 19 of this data sheet.
MC34071,2,4,A MC33071,2,4,A, NCV33072,4,A

PIN CONNECTIONS

CASE 751
Offset Null
Inputs
Output
VEE
(Dual, Top View)
Output 1
Inputs 1
VEE
(Dual, Top View)

CASE 751A/ CASE 948G
Output 1
Inputs 1
Input 4
VEE
(Dual, Top View)

CASE 510AJ
Output 1
Inputs 1
Input 4
VEE
(Top View)

Figure 1. Representative Schematic Diagram
(Each Amplifier)
### MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (from $V_{EE}$ to $V_{CC}$)</td>
<td>$V_S$</td>
<td>+44</td>
<td>V</td>
</tr>
<tr>
<td>Input Differential Voltage Range</td>
<td>$V_{IDR}$</td>
<td>(Note 1)</td>
<td>V</td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td>$V_{IR}$</td>
<td>(Note 1)</td>
<td>V</td>
</tr>
<tr>
<td>Output Short Circuit Duration (Note 2)</td>
<td>$t_{SC}$</td>
<td>Indefinite</td>
<td>Sec</td>
</tr>
<tr>
<td>Operating Junction Temperature</td>
<td>$T_J$</td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$T_{stg}$</td>
<td>−60 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>ESD Capability, Dual and Quad (Note 3)</td>
<td>$E_{SD_{HBM}}$</td>
<td>2000</td>
<td>V</td>
</tr>
<tr>
<td>Human Body Model</td>
<td>$E_{SD_{MM}}$</td>
<td>200</td>
<td></td>
</tr>
<tr>
<td>Machine Model</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Either or both input voltages should not exceed the magnitude of $V_{CC}$ or $V_{EE}$.
2. Power dissipation must be considered to ensure maximum junction temperature ($T_J$) is not exceeded (see Figure 2).
3. This device series incorporates ESD protection and is tested by the following methods:
   - ESD Human Body Model tested per AEC–Q100–002 (JEDEC standard: JESD22–A114)
   - ESD Machine Model tested per AEC–Q100–003 (JEDEC standard: JESD22–A115)
## ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = +15 V, V<sub>EE</sub> = −15 V, R<sub>L</sub> = connected to ground, unless otherwise noted. See Note 4 for T<sub>A</sub> = T<sub>low</sub> to T<sub>high</sub>)

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>A Suffix</th>
<th>Non-Suffix</th>
<th>A Suffix</th>
<th>Non-Suffix</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Offset Voltage (R&lt;sub&gt;S&lt;/sub&gt; = 100 Ω, V&lt;sub&gt;CM&lt;/sub&gt; = 0 V, V&lt;sub&gt;O&lt;/sub&gt; = 0 V)</td>
<td>V&lt;sub&gt;IO&lt;/sub&gt;</td>
<td>Min</td>
<td>0.5</td>
<td>3.0</td>
<td>Min</td>
<td>1.0</td>
</tr>
<tr>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = +15 V, V&lt;sub&gt;EE&lt;/sub&gt; = −15 V, T&lt;sub&gt;A&lt;/sub&gt; = +25°C</td>
<td></td>
<td>Typ</td>
<td>0.5</td>
<td>3.0</td>
<td>Typ</td>
<td>1.5</td>
</tr>
<tr>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = +5.0 V, V&lt;sub&gt;EE&lt;/sub&gt; = 0 V, T&lt;sub&gt;A&lt;/sub&gt; = +25°C</td>
<td></td>
<td>Max</td>
<td>–</td>
<td>5.0</td>
<td>Max</td>
<td>–</td>
</tr>
<tr>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = +15 V, V&lt;sub&gt;EE&lt;/sub&gt; = −15 V, T&lt;sub&gt;A&lt;/sub&gt; = T&lt;sub&gt;low&lt;/sub&gt; to T&lt;sub&gt;high&lt;/sub&gt;</td>
<td>–</td>
<td>10</td>
<td>–</td>
<td>10</td>
<td>–</td>
<td>10</td>
</tr>
<tr>
<td>Average Temperature Coefficient of Input Offset Voltage</td>
<td>ΔV&lt;sub&gt;IO&lt;/sub&gt;/ΔT</td>
<td>Min</td>
<td>–</td>
<td>10</td>
<td>Min</td>
<td>–</td>
</tr>
<tr>
<td>R&lt;sub&gt;S&lt;/sub&gt; = 10 Ω, V&lt;sub&gt;CM&lt;/sub&gt; = 0 V, V&lt;sub&gt;O&lt;/sub&gt; = 0 V, T&lt;sub&gt;A&lt;/sub&gt; = T&lt;sub&gt;low&lt;/sub&gt; to T&lt;sub&gt;high&lt;/sub&gt;</td>
<td></td>
<td>Typ</td>
<td>–</td>
<td>700</td>
<td>Typ</td>
<td>–</td>
</tr>
<tr>
<td>Input Bias Current (V&lt;sub&gt;CM&lt;/sub&gt; = 0 V, V&lt;sub&gt;O&lt;/sub&gt; = 0 V)</td>
<td>I&lt;sub&gt;IB&lt;/sub&gt;</td>
<td>Min</td>
<td>–</td>
<td>100</td>
<td>Min</td>
<td>–</td>
</tr>
<tr>
<td>T&lt;sub&gt;A&lt;/sub&gt; = +25°C</td>
<td>Typ</td>
<td>500</td>
<td>Typ</td>
<td>500</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Max</td>
<td>–</td>
<td>700</td>
<td>Max</td>
<td>–</td>
<td>700</td>
</tr>
<tr>
<td>Input Offset Current (V&lt;sub&gt;CM&lt;/sub&gt; = 0 V, V&lt;sub&gt;O&lt;/sub&gt; = 0 V)</td>
<td>I&lt;sub&gt;IO&lt;/sub&gt;</td>
<td>Min</td>
<td>–</td>
<td>6.0</td>
<td>Min</td>
<td>–</td>
</tr>
<tr>
<td>T&lt;sub&gt;A&lt;/sub&gt; = +25°C</td>
<td>Typ</td>
<td>50</td>
<td>Typ</td>
<td>50</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Max</td>
<td>–</td>
<td>300</td>
<td>Max</td>
<td>–</td>
<td>300</td>
</tr>
<tr>
<td>Input Common Mode Voltage Range</td>
<td>V&lt;sub&gt;ICR&lt;/sub&gt;</td>
<td>V&lt;sub&gt;EE&lt;/sub&gt; to (V&lt;sub&gt;CC&lt;/sub&gt; − 1.8)</td>
<td>Min</td>
<td>–</td>
<td>25</td>
<td>Min</td>
</tr>
<tr>
<td>T&lt;sub&gt;A&lt;/sub&gt; = +25°C</td>
<td>V&lt;sub&gt;EE&lt;/sub&gt; to (V&lt;sub&gt;CC&lt;/sub&gt; − 2.2)</td>
<td>Typ</td>
<td>100</td>
<td>Typ</td>
<td>100</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;EE&lt;/sub&gt; to (V&lt;sub&gt;CC&lt;/sub&gt; − 1.8)</td>
<td>Max</td>
<td>–</td>
<td>20</td>
<td>Max</td>
<td>–</td>
</tr>
<tr>
<td>Large Signal Voltage Gain (V&lt;sub&gt;O&lt;/sub&gt; = ±10 V, R&lt;sub&gt;L&lt;/sub&gt; = 2.0 kΩ)</td>
<td>A&lt;sub&gt;VOL&lt;/sub&gt;</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = +15 V, V&lt;sub&gt;EE&lt;/sub&gt; = −15 V, R&lt;sub&gt;L&lt;/sub&gt; = 10 kΩ</td>
<td>Min</td>
<td>–</td>
<td>1.6</td>
<td>Min</td>
</tr>
<tr>
<td>T&lt;sub&gt;A&lt;/sub&gt; = +25°C</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = +15 V, V&lt;sub&gt;EE&lt;/sub&gt; = −15 V, R&lt;sub&gt;L&lt;/sub&gt; = 2.0 kΩ</td>
<td>Typ</td>
<td>2.0</td>
<td>Typ</td>
<td>2.0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Max</td>
<td>–</td>
<td>2.8</td>
<td>Max</td>
<td>–</td>
<td>2.8</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;EE&lt;/sub&gt; = 0 V, R&lt;sub&gt;L&lt;/sub&gt; = 2.0 kΩ, T&lt;sub&gt;A&lt;/sub&gt; = +25°C</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Output Voltage Swing (V&lt;sub&gt;ID&lt;/sub&gt; = ±1.0 V)</td>
<td>V&lt;sub&gt;OH&lt;/sub&gt;</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = +15 V, V&lt;sub&gt;EE&lt;/sub&gt; = −15 V, R&lt;sub&gt;L&lt;/sub&gt; = 10 kΩ</td>
<td>Min</td>
<td>–</td>
<td>3.7</td>
<td>Min</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;ICR&lt;/sub&gt; = V&lt;sub&gt;CM&lt;/sub&gt;, TA = 25°C</td>
<td>Typ</td>
<td>4.0</td>
<td>Typ</td>
<td>4.0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;EE&lt;/sub&gt; = 0 V, R&lt;sub&gt;L&lt;/sub&gt; = 2.0 kΩ</td>
<td>Max</td>
<td>–</td>
<td>13.6</td>
<td>Max</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>T&lt;sub&gt;A&lt;/sub&gt; = T&lt;sub&gt;low&lt;/sub&gt; to T&lt;sub&gt;high&lt;/sub&gt;</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = +15 V, V&lt;sub&gt;EE&lt;/sub&gt; = −15 V, R&lt;sub&gt;L&lt;/sub&gt; = 2.0 kΩ</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>T&lt;sub&gt;A&lt;/sub&gt; = T&lt;sub&gt;low&lt;/sub&gt; to T&lt;sub&gt;high&lt;/sub&gt;</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Output Short Circuit Current (V&lt;sub&gt;ID&lt;/sub&gt; = 1.0 V, V&lt;sub&gt;O&lt;/sub&gt; = 0 V, T&lt;sub&gt;A&lt;/sub&gt; = +25°C)</td>
<td>I&lt;sub&gt;SC&lt;/sub&gt;</td>
<td>Source</td>
<td>Min</td>
<td>10</td>
<td>Min</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>Sink</td>
<td>Min</td>
<td>20</td>
<td>Min</td>
<td>20</td>
<td>–</td>
</tr>
<tr>
<td>Common Mode Rejection</td>
<td>CMR</td>
<td>R&lt;sub&gt;S&lt;/sub&gt; ≤ 10 kΩ, V&lt;sub&gt;CM&lt;/sub&gt; = V&lt;sub&gt;ICR&lt;/sub&gt;, T&lt;sub&gt;A&lt;/sub&gt; = 25°C</td>
<td>80</td>
<td>97</td>
<td>–</td>
<td>70</td>
</tr>
<tr>
<td>Power Supply Rejection (R&lt;sub&gt;S&lt;/sub&gt; = 100 Ω)</td>
<td>PSR</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt;/V&lt;sub&gt;EE&lt;/sub&gt; = +16.5 V/−16.5 V to +13.5 V/−13.5 V, T&lt;sub&gt;A&lt;/sub&gt; = 25°C</td>
<td>80</td>
<td>97</td>
<td>–</td>
<td>70</td>
</tr>
<tr>
<td>Power Supply Current (Per Amplifier, No Load)</td>
<td>I&lt;sub&gt;D&lt;/sub&gt;</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = +5.0 V, V&lt;sub&gt;EE&lt;/sub&gt; = 0 V, V&lt;sub&gt;OD&lt;/sub&gt; = +2.5 V, T&lt;sub&gt;A&lt;/sub&gt; = +25°C</td>
<td>–</td>
<td>1.6</td>
<td>–</td>
<td>1.6</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = +15 V, V&lt;sub&gt;EE&lt;/sub&gt; = −15 V, V&lt;sub&gt;OD&lt;/sub&gt; = 0 V, T&lt;sub&gt;A&lt;/sub&gt; = +25°C</td>
<td>–</td>
<td>2.0</td>
<td>–</td>
<td>2.0</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = +15 V, V&lt;sub&gt;EE&lt;/sub&gt; = −15 V, V&lt;sub&gt;O&lt;/sub&gt; = 0 V, T&lt;sub&gt;A&lt;/sub&gt; = +25°C</td>
<td>–</td>
<td>1.9</td>
<td>–</td>
<td>1.9</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>Max</td>
<td>–</td>
<td>2.8</td>
<td>Max</td>
<td>–</td>
<td>2.8</td>
</tr>
<tr>
<td>Case 510AJ T&lt;sub&gt;low&lt;/sub&gt;/T&lt;sub&gt;high&lt;/sub&gt; guaranteed by product characterization.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
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</table>

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. T<sub>low</sub> = −40°C for MC33071,2,4/A, NCV33074/A T<sub>high</sub> = +85°C for MC33071,2,4/A, NCV33074/A
   = 0°C for MC34071,2,4/A = +70°C for MC34071,2,4/A
   = −40°C for MC34072,4/V, NCV33072,4A = +125°C for MC34072,4/V, NCV33072,4A, NCV34074V
   Case 510AJ T<sub>low</sub>/T<sub>high</sub> guaranteed by product characterization.
AC ELECTRICAL CHARACTERISTICS (VCC = +15 V, VEE = −15 V, RL = connected to ground. TA = +25°C, unless otherwise noted.)

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>A Suffix</th>
<th>Non−Suffix</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slew Rate (Vin = −10 V to +10 V, RL = 2.0 kΩ, CL = 500 pF)</td>
<td>SR</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>AV = +1.0</td>
<td>8.0</td>
<td>10</td>
<td>−</td>
<td>8.0</td>
</tr>
<tr>
<td>AV = −1.0</td>
<td>−</td>
<td>13</td>
<td>−</td>
<td>−</td>
</tr>
<tr>
<td>Setting Time (10 V Step, AV = −1.0)</td>
<td>ts</td>
<td>−</td>
<td>1.1</td>
<td>−</td>
</tr>
<tr>
<td>To 0.1% (+1/2 LSB of 9−Bits)</td>
<td>−</td>
<td>2.2</td>
<td>−</td>
<td>2.2</td>
</tr>
<tr>
<td>To 0.01% (+1/2 LSB of 12−Bits)</td>
<td>−</td>
<td>2.2</td>
<td>−</td>
<td>2.2</td>
</tr>
<tr>
<td>Gain Bandwidth Product (f = 100 kHz)</td>
<td>GBW</td>
<td>3.5</td>
<td>4.5</td>
<td>−</td>
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<tr>
<td>Power Bandwidth</td>
<td>BW</td>
<td>−</td>
<td>160</td>
<td>−</td>
</tr>
<tr>
<td>Phase margin</td>
<td>fm</td>
<td>−</td>
<td>60</td>
<td>−</td>
</tr>
<tr>
<td>RL = 2.0 kΩ</td>
<td>−</td>
<td>40</td>
<td>−</td>
<td>−</td>
</tr>
<tr>
<td>Gain Margin</td>
<td>Am</td>
<td>−</td>
<td>12</td>
<td>−</td>
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<tr>
<td>RL = 2.0 kΩ</td>
<td>−</td>
<td>4.0</td>
<td>−</td>
<td>−</td>
</tr>
<tr>
<td>Equivalent Input Noise Voltage</td>
<td>en</td>
<td>−</td>
<td>32</td>
<td>−</td>
</tr>
<tr>
<td>Rs = 100 Ω, f = 1.0 kHz</td>
<td>−</td>
<td>0.22</td>
<td>−</td>
<td>−</td>
</tr>
<tr>
<td>Equivalent Input Noise Current</td>
<td>in</td>
<td>−</td>
<td>0.22</td>
<td>−</td>
</tr>
<tr>
<td>f = 1.0 kHz</td>
<td>−</td>
<td>−</td>
<td>−</td>
<td>−</td>
</tr>
<tr>
<td>Differential Input Resistance</td>
<td>Rin</td>
<td>−</td>
<td>150</td>
<td>−</td>
</tr>
<tr>
<td>VCM = 0 V</td>
<td>−</td>
<td>−</td>
<td>−</td>
<td>−</td>
</tr>
<tr>
<td>Differential Input Capacitance</td>
<td>Cin</td>
<td>−</td>
<td>2.5</td>
<td>−</td>
</tr>
<tr>
<td>VCM = 0 V</td>
<td>−</td>
<td>−</td>
<td>−</td>
<td>−</td>
</tr>
<tr>
<td>Total Harmonic Distortion</td>
<td>THD</td>
<td>−</td>
<td>0.02</td>
<td>−</td>
</tr>
<tr>
<td>AV = +10, RL = 2.0 kΩ, 2.0 Vpp ≤ VO ≤ 20 Vpp, f = 10 kHz</td>
<td>−</td>
<td>−</td>
<td>120</td>
<td>−</td>
</tr>
<tr>
<td>Channel Separation (f = 10 kHz)</td>
<td>−</td>
<td>−</td>
<td>120</td>
<td>−</td>
</tr>
<tr>
<td>Open Loop Output Impedance (f = 1.0 MHz)</td>
<td></td>
<td>−</td>
<td>30</td>
<td>−</td>
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</table>

Single Supply
3.0 V to 44 V

Split Supplies
VCC+VEE≤44 V

Figure 2. Power Supply Configurations

Figure 3. Offset Null Circuit

Offset nulling range is approximately ±80 mV with a 10 k potentiometer (MC33071, MC34071 only).
Figure 4. Maximum Power Dissipation versus Temperature for Package Types

Figure 5. Input Offset Voltage versus Temperature for Representative Units

Figure 6. Input Common Mode Voltage Range versus Temperature

Figure 7. Normalized Input Bias Current versus Temperature

Figure 8. Normalized Input Bias Current versus Input Common Mode Voltage

Figure 9. Split Supply Output Voltage Swing versus Supply Voltage
1. Phase \( RL = 2.0 \, k \)
2. Phase \( RL = 2.0 \, k, \, CL = 300 \, pF \)
3. Gain \( RL = 2.0 \, k \)
4. Gain \( RL = 2.0 \, k, \, CL = 300 \, pF \)

\( V_{CC} = 15 \, V \)
\( V_{EE} = 15 \, V \)
\( V_{O} = 0 \, V \)
\( RL = 2.0 \, k \)
\( TA = 25^\circ C \)

**Figure 16. Total Harmonic Distortion versus Frequency**

**Figure 17. Total Harmonic Distortion versus Output Voltage Swing**

**Figure 18. Open Loop Voltage Gain versus Temperature**

**Figure 19. Open Loop Voltage Gain and Phase versus Frequency**

**Figure 20. Open Loop Voltage Gain and Phase versus Frequency**

**Figure 21. Normalized Gain Bandwidth Product versus Temperature**
Figure 22. Percent Overshoot versus Load Capacitance

Figure 23. Phase Margin versus Load Capacitance

Figure 24. Gain Margin versus Load Capacitance

Figure 25. Phase Margin versus Temperature

Figure 26. Gain Margin versus Temperature

Figure 27. Phase Margin and Gain Margin versus Differential Source Resistance
Figure 28. Normalized Slew Rate versus Temperature

Figure 29. Output Settling Time

Figure 30. Small Signal Transient Response

Figure 31. Large Signal Transient Response

Figure 32. Common Mode Rejection versus Frequency

Figure 33. Power Supply Rejection versus Frequency
MC34071,2,4,A MC33071,2,4,A, NCV33072,4,A

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Figure 34. Supply Current versus Supply Voltage

Figure 35. Power Supply Rejection versus Temperature

Figure 36. Channel Separation versus Frequency

Figure 37. Input Noise versus Frequency

APPLICATIONS INFORMATION
CIRCUIT DESCRIPTION/PERFORMANCE FEATURES

Although the bandwidth, slew rate, and settling time of the MC34071 amplifier series are similar to op amp products utilizing JFET input devices, these amplifiers offer other additional distinct advantages as a result of the PNP transistor differential input stage and an all NPN transistor output stage.

Since the input common mode voltage range of this input stage includes the VEE potential, single supply operation is feasible to as low as 3.0 V with the common mode input voltage at ground potential.

The input stage also allows differential input voltages up to ±44 V, provided the maximum input voltage range is not exceeded. Specifically, the input voltages must range between VEE and VCC supply voltages as shown by the maximum rating table. In practice, although not recommended, the input voltages can exceed the VCC voltage by approximately 3.0 V and decrease below the VEE voltage by 0.3 V without causing product damage, although output phase reversal may occur. It is also possible to source up to approximately 5.0 mA of current from VEE through either inputs clamping diode without damage or latching, although phase reversal may again occur.

If one or both inputs exceed the upper common mode voltage limit, the amplifier output is readily predictable and may be in a low or high state depending on the existing input bias conditions.

Since the input capacitance associated with the small geometry input device is substantially lower (2.5 pF) than the typical JFET input gate capacitance (5.0 pF), better frequency response for a given input source resistance can be achieved using the MC34071 series of amplifiers. This performance feature becomes evident, for example, in fast settling D→A current to voltage conversion applications where the feedback resistance can form an input pole with the input capacitance of the op amp. This input pole creates a 2nd order system with the single pole op amp and is therefore detrimental to its settling time. In this context, lower input capacitance is desirable especially for higher
values of feedback resistances (lower current DACs). This
input pole can be compensated for by creating a feedback
zero with a capacitance across the feedback resistance, if
necessary, to reduce overshoot. For 2.0 kΩ of feedback
resistance, the MC34071 series can settle to within 1/2 LSB
of 8–bits in 1.0 μs, and within 1/2 LSB of 12–bits in 2.2 μs
for a 10 V step. In an inverting unity gain fast settling
configuration, the symmetrical slew rate is ±13 V/μs. In the
classic noninverting unity gain configuration, the output
positive slew rate is +10 V/μs, and the corresponding
negative slew rate will exceed the positive slew rate as a
function of the fall time of the input waveform.

Since the bipolar input device matching characteristics
are superior to that of JFETs, a low untrimmed maximum
offset voltage of 3.0 mV prime and 5.0 mV downgrade can
be economically offered with high frequency performance
characteristics. This combination is ideal for low cost
precision, high speed quad op amp applications.

The all NPN output stage, shown in its basic form on the
equivalent circuit schematic, offers unique advantages over
the more conventional NPN/PNP transistor Class AB output
stage. A 10 kΩ load resistance can swing within 1.0 V of
the positive rail (VCC), and within 0.3 V of the negative rail
(VEE), providing a 28.7 Vpp swing from ±15 V supplies.
This large output swing becomes most noticeable at lower
supply voltages.

The positive swing is limited by the saturation voltage of
the current source transistor Q7, and VBE of the NPN pull up
transistor Q17, and the voltage drop associated with the short
circuit resistance, R7. The negative swing is limited by the
saturation voltage of the pull–down transistor Q16, the
voltage drop ILR6, and the voltage drop associated with
resistance R7, where IL is the sink load current. For small
valued sink currents, the above voltage drops are negligible,
allowing the negative swing voltage to approach within
millivolts of VEE. For large valued sink currents (>5.0 mA),
diode D3 clamps the voltage across R6, thus limiting the
eegative swing to the saturation voltage of Q16, plus the
forward diode drop of D3 (≈VEE +1.0 V). Thus for a given
supply voltage, unprecedented peak-to-peak output voltage
swing is possible as indicated by the output swing
specifications.

If the load resistance is referenced to VCC instead of
ground for single supply applications, the maximum
possible output swing can be achieved for a given supply
voltage. For light load currents, the load resistance will pull
the output to VCC during the positive swing and the output
will pull the load resistance near ground during the negative
swing. The load resistance value should be much less than
that of the feedback resistance to maximize pull up
capability.

Because the PNP output emitter–follower transistor has
been eliminated, the MC34071 series offers a 20 mA
minimum current sink capability, typically to an output
voltage of (VEE +1.8 V). In single supply applications the
output can directly source or sink base current from a
common emitter NPN transistor for fast high current
switching applications.

In addition, all NPN transistor output stage is
inherently fast, contributing to the bipolar amplifiers’ high
gain bandwidth product and fast settling capability. The
associated high frequency low output impedance (30 Ω typ
at 1.0 MHz) allows capacitive drive capability from 0 pF to
10,000 pF without oscillation in the unity closed loop gain
configuration. The 60°C phase margin and 12 dB gain margin
as well as the general gain and phase characteristics are
virtually independent of the source/sink output swing
conditions. This allows easier system phase compensation,
since output swing will not be a phase consideration. The
high frequency characteristics of the MC34071 series also
allow excellent high frequency active filter capability,
especially for low voltage single supply applications.

Although the single supply specifications is defined at
5.0 V, these amplifiers are functional to 3.0 V @ 25°C
although slight changes in parametrics such as bandwidth,
slew rate, and DC gain may occur.

If power to this integrated circuit is applied in reverse
polarity or if the IC is installed backwards in a socket, large
unlimited current surges will occur through the device that
can result in device destruction.

Special static precautions are not necessary for these
bipolar amplifiers since there are no MOS transistors on the
die.

As with most high frequency amplifiers, proper lead
dress, component placement, and PC board layout should be
exercised for optimum frequency performance. For example,
long unshielded input or output leads may result in
unwanted input–output coupling. In order to preserve the
relatively low input capacitance associated with these
amplifiers, resistors connected to the inputs should be
immediately adjacent to the input pin to minimize additional
stray input capacitance. This not only minimizes the input
pole for optimum frequency response, but also minimizes
extraneous “pick up” at this node. Supply decoupling with
adequate capacitance immediately adjacent to the supply pin
is also important, particularly over temperature, since many
types of decoupling capacitors exhibit great impedance
changes over temperature.

The output of any one amplifier is current limited and thus
protected from a direct short to ground. However, under
such conditions, it is important not to allow the device to
exceed the maximum junction temperature rating. Typically
for ±15 V supplies, any one output can be shorted
continuously to ground without exceeding the maximum
temperature rating.
MC34071,2,4,A, MC33071,2,4,A, NCV33072,4,A

(Typical Single Supply Applications $V_{CC} = 5.0$ V)

Figure 38. AC Coupled Noninverting Amplifier

Figure 39. AC Coupled Inverting Amplifier

Figure 40. DC Coupled Inverting Amplifier

Figure 41. Unity Gain Buffer TTL Driver

Figure 42. Active High-Q Notch Filter

Figure 43. Active Bandpass Filter

- $V_{CC} = 5.1$ M
- $C_{in} = 1.0$ M
- $A_V = 101$
- $BW (-3.0$ dB$) = 45$ kHz

- $V_{CC} = 3.7$ Vpp
- $R_L = 10$ k
- $C_{in} = 10$ k
- $A_V = 10$
- $BW (-3.0$ dB$) = 450$ kHz

- $V_{CC} = 2.63$ V
- $4.75$ Vpp
- $91$ k
- $5.1$ k
- $R_L = 100$ k
- $A_V = 10$
- $BW (-3.0$ dB$) = 450$ kHz

- $V_{in} = 2.5$ V
- $0$ to $10,000$ pF
- Cable
- TTL Gate

- $V_{in} = 0$
- $0.01$
- $32$ k
- $2.0$ R
- $16$ k
- $R = 0.047$
- $2.0$ C
- $0.02$
- $R = 0.047$
- $2.0$ C
- $0.02$

- $V_{in} = 3.6$ Vpp
- $R = 0.047$
- $2.0$ C
- $0.02$

- $V_{in} = 2.5$ V
- $0.01$
- $32$ k
- $2.0$ R
- $16$ k

- $V_{in} = 0$
- $16$ k
- $2.0$ C
- $0.02$
- $R = 0.047$
- $2.0$ C
- $0.02$

- $R_L = 100$ k
- $C_{in} = 68$ k
- $C_{in} = 10$ k

- $V_{in} = 370$ mVpp
- $100$ k
- $A_V = 10$
- $BW (-3.0$ dB$) = 450$ kHz

- $V_{CC} = 3.7$ Vpp
- $0$
- $100$ k
- $A_V = 10$
- $BW (-3.0$ dB$) = 450$ kHz

- $V_{in} = 2.5$ V
- $0.01$
- $32$ k
- $2.0$ R
- $16$ k

- $V_{in} = 0$
- $16$ k
- $2.0$ C
- $0.02$
- $R = 0.047$
- $2.0$ C
- $0.02$

- $V_{in} = 3.6$ Vpp
- $R = 0.047$
- $2.0$ C
- $0.02$

- $V_{in} = 2.5$ V
- $0.01$
- $32$ k
- $2.0$ R
- $16$ k

- $V_{in} = 0$
- $16$ k
- $2.0$ C
- $0.02$
- $R = 0.047$
- $2.0$ C
- $0.02$

- $R_L = 100$ k
- $C_{in} = 68$ k
- $C_{in} = 10$ k

- $V_{in} = 370$ mVpp
- $100$ k
- $A_V = 10$
- $BW (-3.0$ dB$) = 450$ kHz

- $V_{in} = 2.5$ V
- $0.01$
- $32$ k
- $2.0$ R
- $16$ k

- $V_{in} = 0$
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- $2.0$ C
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- $100$ k
- $A_V = 10$
- $BW (-3.0$ dB$) = 450$ kHz

- $V_{in} = 2.5$ V
- $0.01$
- $32$ k
- $2.0$ R
- $16$ k

- $V_{in} = 0$
- $16$ k
- $2.0$ C
- $0.02$
- $R = 0.047$
- $2.0$ C
- $0.02$
Figure 44. Low Voltage Fast D/A Converter

Figure 45. High Speed Low Voltage Comparator

Figure 46. LED Driver

Figure 47. Transistor Driver

Figure 48. AC/DC Ground Current Monitor

Figure 49. Photovoltaic Cell Amplifier
Figure 50. Low Input Voltage Comparator with Hysteresis

\[
\begin{align*}
V_{\text{INL}} &= \frac{R_1}{R_1+R_2} (V_{\text{OL}}-V_{\text{ref}}) + V_{\text{ref}} \\
V_{\text{INH}} &= \frac{R_1}{R_1+R_2} (V_{\text{OH}}-V_{\text{ref}}) + V_{\text{ref}} \\
V_H &= \frac{R_1}{R_1+R} (V_{\text{OH}}-V_{\text{OL}})
\end{align*}
\]

Figure 51. High Compliance Voltage to Sink Current Converter

\[
I_{\text{OUT}} = \frac{V_{\text{IN}}-V_{\text{IO}}}{R}
\]

Figure 52. High Input Impedance Differential Amplifier

\[
V_O = 1 + \frac{R_2}{R_1} \left( V_2 - V_1 \right) \quad \left( \frac{R_2}{R_1} \text{ Critical to CMRR} \right)
\]

For \( V_2 \geq V_1 \), \( V > 0 \)

Figure 53. Bridge Current Amplifier

\[
V_O = V_{\text{ref}} - \frac{\Delta R}{2R^2} R_F \quad \left( V_O \geq 0.1 \text{ V} \right)
\]

Figure 54. Low Voltage Peak Detector

\[
V_O = V_{\text{IN}} (\text{pk})
\]

Figure 55. High Frequency Pulse Width Modulation

\[
I_{\text{OSC}} = \frac{0.85}{R_C}
\]

Base Charge Removal

Pulse Width Control Group
GENERAL ADDITIONAL APPLICATIONS INFORMATION VS = ±15.0 V

Figure 56. Second Order Low-Pass Active Filter

```
Choose: f_o, H_o, C2
Then: C1 = 2C2 (H_o+1)
```

```
R2 = \frac{\sqrt{2}}{4\pi f_o C2}
R3 = \frac{R2}{H_o+1}
R1 = \frac{R2}{H_o}
```

Figure 57. Second Order High-Pass Active Filter

```
Choose: f_o, H_o, C1
Then: R1 = \frac{H_o+0.5}{\pi f_o C1 \sqrt{2}}
R2 = \frac{\sqrt{2}}{2\pi f_o C1 (1/H_o+2)}
C2 = \frac{C}{H_o}
```

Figure 58. Fast Settling Inverter

```
I
\text{Uncompensated: } t_s = 1.0 \mu s
\text{to 1/2 LSB (8-Bits)}
\text{Compensated: } t_s = 2.2 \mu s
\text{to 1/2 LSB (12-Bits)}
SR = 13 V/\mu s
```

Figure 59. Basic Inverting Amplifier

```
\frac{V_o}{V_{in}} = \frac{R_2}{R_1}
BW (-3.0 \text{ dB}) = GBW \left[ \frac{R_1}{R_1 + R_2} \right]
SR = 13 V/\mu s
```

Figure 60. Basic Noninverting Amplifier

```
\frac{V_o}{V_{in}} = \left( 1 + \frac{R_2}{R_1} \right)
BW (-3.0 \text{ dB}) = GBW \left[ \frac{R_1}{R_1 + R_2} \right]
```

Figure 61. Unity Gain Buffer (A_V = +1.0)
Example:

Let: \( R = R_E = 12 \, k \Omega \)

Then: \( A_V = 3.0 \)

\[ BW = 1.5 \, MHz \]

\[ A_V = \frac{1 + 2 \cdot \frac{R}{R_E}}{} \]

**Figure 62. High Impedance Differential Amplifier**

**Figure 63. Dual Voltage Doubler**
## ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Op Amp Function</th>
<th>Device</th>
<th>Operating Temperature Range</th>
<th>Package</th>
<th>Shipping†</th>
</tr>
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<tbody>
<tr>
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<td>MC34071DR2G</td>
<td>$T_A = 0^\circ$ to +70°C</td>
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†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV prefix for automotive and other applications requiring unique site and control change requirements; AEC–Q100 qualified and PPAP capable.
MARKING DIAGRAMS

SOIC-8
D SUFFIX
CASE 751

SOIC-14
D SUFFIX
CASE 751A

TSSOP-14
DTB SUFFIX
CASE 948G

WQFN10
MT SUFFIX
CASE 510AJ

x = 3 or 4
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or * = Pb-Free Package
(Note: Microdot may be in either location)
NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

SOLDERING FOOTPRINT*

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

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*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “∗”, may or may not be present. Some products may not follow the Generic Marking.

**SOLDERING FOOTPRINT**

**DISCRETE**

**IC**

**IC (Pb−Free)**

**IC**

**DISCRETE (Pb−Free)**

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5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

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**Document Number:** 98ASB42564B

**Description:** SOIC-8 NB

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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

SOLDERING FOOTPRINT*

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:  
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PAGE 2 OF 2  
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**MECHANICAL CASE OUTLINE**

**PACKAGE DIMENSIONS**

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**TSSOP-14 WB**

**CASE 948G**

**ISSUE C**

**DATE** 17 FEB 2016

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**NOTES:**

2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
   INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.
8. DIMENSIONS: MILLIMETERS

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**SCALE 2:1**

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**SECTION N-N**

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**SOLDERING FOOTPRINT**

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**DIMENSIONS: MILLIMETERS**

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**GENDER MARKING DIAGRAM**

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**NOTES:**

- This information is generic. Please refer to device data sheet for actual part marking.
- Pb-Free indicator, "G" or microdot "C0071", may or may not be present.
- The generic marking diagram is shown for reference.

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**DOCUMENT NUMBER:** 98ASH70246A

**DESCRIPTION:** TSSOP-14 WB

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