MC34063A, MC33063A, SC34063A, SC33063A, NCV33063A

Inverting Regulator - Buck, Boost, Switching

1.5 A

The MC34063A Series is a monolithic control circuit containing the primary functions required for DC–to–DC converters. These devices consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in Step–Down and Step–Up and Voltage–Inverting applications with a minimum number of external components. Refer to Application Notes AN920A/D and AN954/D for additional design information.

Features
- Operation from 3.0 V to 40 V Input
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.5 A
- Output Voltage Adjustable
- Frequency Operation to 100 kHz
- Precision 2% Reference
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

This device contains 79 active transistors.

Figure 1. Representative Schematic Diagram

ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.
Figure 2. Pin Connections

MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Voltage</td>
<td>(V_{CC})</td>
<td>40</td>
<td>Vdc</td>
</tr>
<tr>
<td>Comparator Input Voltage Range</td>
<td>(V_{IR})</td>
<td>−0.3 to +40</td>
<td>Vdc</td>
</tr>
<tr>
<td>Switch Collector Voltage</td>
<td>(V_{C(switch)})</td>
<td>40</td>
<td>Vdc</td>
</tr>
<tr>
<td>Switch Emitter Voltage ((V_{Pin;1} = 40;V))</td>
<td>(V_{E(switch)})</td>
<td>40</td>
<td>Vdc</td>
</tr>
<tr>
<td>Switch Collector to Emitter Voltage</td>
<td>(V_{CE(switch)})</td>
<td>40</td>
<td>Vdc</td>
</tr>
<tr>
<td>Driver Collector Voltage</td>
<td>(V_{C(driver)})</td>
<td>40</td>
<td>Vdc</td>
</tr>
<tr>
<td>Driver Collector Current (\text{(Note 1)})</td>
<td>(I_{C(driver)})</td>
<td>100</td>
<td>mA</td>
</tr>
<tr>
<td>Switch Current</td>
<td>(I_{SW})</td>
<td>1.5</td>
<td>A</td>
</tr>
<tr>
<td>Power Dissipation and Thermal Characteristics</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Plastic Package, P, P1 Suffix</td>
<td>(P_{D})</td>
<td>1.25</td>
<td>W</td>
</tr>
<tr>
<td>Thermal Resistance</td>
<td>(R_{IUJ})</td>
<td>115</td>
<td>°C/W</td>
</tr>
<tr>
<td>SOIC Package, D Suffix</td>
<td>(P_{D})</td>
<td>625</td>
<td>mW</td>
</tr>
<tr>
<td>Thermal Resistance</td>
<td>(R_{IUJ})</td>
<td>160</td>
<td>°C/W</td>
</tr>
<tr>
<td>Thermal Resistance</td>
<td>(R_{IUC})</td>
<td>45</td>
<td>°C/W</td>
</tr>
<tr>
<td>DFN Package</td>
<td>(P_{D})</td>
<td>1.25</td>
<td>mW</td>
</tr>
<tr>
<td>Thermal Resistance</td>
<td>(R_{IUJ})</td>
<td>80</td>
<td>°C/W</td>
</tr>
<tr>
<td>Operating Junction Temperature</td>
<td>(T_J)</td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td>Operating Ambient Temperature Range</td>
<td>(T_A)</td>
<td>0 to +70</td>
<td>°C</td>
</tr>
<tr>
<td>MC34063A, SC34063A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MC33063AV, NCV33063A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MC33063A, SC33063A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>(T_{stg})</td>
<td>−65 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Maximum package power dissipation limits must be observed.
2. This device series contains ESD protection and exceeds the following tests: Human Body Model 4000 V per MIL-STD-883, Method 3015. Machine Model Method 400 V.
3. NCV prefix is for automotive and other applications requiring site and change control.
### ELECTRICAL CHARACTERISTICS

(VCC = 5.0 V, TA = Tlow to THigh [Note 4], unless otherwise specified.)

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>OSCILLATOR</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequency (VPin 5 = 0 V, CT = 1.0 nF, TA = 25°C)</td>
<td>fosc</td>
<td>24</td>
<td>33</td>
<td>42</td>
<td>kHz</td>
</tr>
<tr>
<td>Charge Current (VCC = 5.0 V to 40 V, TA = 25°C)</td>
<td>Ichg</td>
<td>24</td>
<td>35</td>
<td>42</td>
<td>µA</td>
</tr>
<tr>
<td>Discharge Current (VCC = 5.0 V to 40 V, TA = 25°C)</td>
<td>Idischg</td>
<td>140</td>
<td>220</td>
<td>260</td>
<td>µA</td>
</tr>
<tr>
<td>Discharge to Charge Current Ratio (Pin 7 to VCC, TA = 25°C)</td>
<td>Idischg/Ichg</td>
<td>5.2</td>
<td>6.5</td>
<td>7.5</td>
<td>–</td>
</tr>
<tr>
<td>Current Limit Sense Voltage (Ichg = Idischg, TA = 25°C)</td>
<td>Vipk(sense)</td>
<td>250</td>
<td>300</td>
<td>350</td>
<td>mV</td>
</tr>
<tr>
<td><strong>OUTPUT SWITCH</strong> (Note 5)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Saturation Voltage, Darlington Connection (Isw = 1.0 A, Pins 1, 8 connected)</td>
<td>VCE(sat)</td>
<td>–</td>
<td>1.0</td>
<td>1.3</td>
<td>V</td>
</tr>
<tr>
<td>Saturation Voltage (Note 6) (Isw = 1.0 A, RPin 8 = 82 Ω to VCC, Forced β = 20)</td>
<td>VCE(sat)</td>
<td>–</td>
<td>0.45</td>
<td>0.7</td>
<td>V</td>
</tr>
<tr>
<td>DC Current Gain (Isw = 1.0 A, VCE = 5.0 V, TA = 25°C)</td>
<td>hFE</td>
<td>50</td>
<td>75</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Collector Off–State Current (VCE = 40 V)</td>
<td>ICOff</td>
<td>–</td>
<td>0.01</td>
<td>100</td>
<td>µA</td>
</tr>
<tr>
<td><strong>COMPARATOR</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Threshold Voltage</td>
<td>Vth</td>
<td>1.225</td>
<td>1.25</td>
<td>1.275</td>
<td>V</td>
</tr>
<tr>
<td>Threshold Voltage Line Regulation (VCC = 3.0 V to 40 V)</td>
<td>Regline</td>
<td>–</td>
<td>1.4</td>
<td>5.0</td>
<td>mV</td>
</tr>
<tr>
<td>MC33063, MC34063</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MC33063V, NCV33063</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Bias Current (Vin = 0 V)</td>
<td>IIB</td>
<td>–</td>
<td>–20</td>
<td>–400</td>
<td>nA</td>
</tr>
<tr>
<td><strong>TOTAL DEVICE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Current (VCC = 5.0 V to 40 V, CT = 1.0 nF, Pin 7 = VCC, VPin 5 &gt; VIL, Pin 2 = GND, remaining pins open)</td>
<td>ICC</td>
<td>–</td>
<td>–</td>
<td>4.0</td>
<td>mA</td>
</tr>
</tbody>
</table>

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Tlow = 0°C for MC34063, SC34063; –40°C for MC33063, SC33063, MC33063V, NCV33063
   THigh = +70°C for MC34063, SC34063; +85°C for MC33063, SC33063; +125°C for MC33063V, NCV33063
5. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.
6. If the output switch is driven into hard saturation (non–Darlington configuration) at low switch currents (≤ 300 mA) and high driver currents (≥ 30 mA), it may take up to 2.0 µs for it to come out of saturation. This condition will shorten the off time at frequencies ≥ 30 kHz, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non–Darlington configuration is used, the following output drive condition is recommended:
   Forced β of output switch: $I_{C\text{ output}}/I_{C\text{ driver}} \geq 10$

* The 100 Ω resistor in the emitter of the driver device requires about 7.0 mA before the output switch conducts.
Figure 3. Oscillator Frequency

VCC = 5.0 V, Pin 7 = VCC
Pin 5 = GND, TA = 25°C

Figure 4. Timing Capacitor Waveform

Vcc = 5V, Ct = 1.0 nF, Ta = 25°C
Pins 1, 5, 8 = open, Pin7 = Vcc, Pin2 = GND

Figure 5. Emitter Follower Configuration Output
Saturation Voltage versus Emitter Current

VCC = 5.0 V
Pins 1, 7, 8 = VCC
Pins 3, 5 = GND
TA = 25°C
(See Note 7)

Figure 6. Common Emitter Configuration Output
Switch Saturation Voltage versus Collector Current

Darlington Connection
Forced β = 20

Figure 7. Current Limit Sense Voltage versus Temperature

VCC = 5.0 V
Ichg = Idischg

Figure 8. Standby Supply Current versus Supply Voltage

Ct = 1.0 nF
Pin 7 = VCC
Pin 2 = GND

7. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.
<table>
<thead>
<tr>
<th>Test</th>
<th>Conditions</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line Regulation</td>
<td>$V_{\text{in}} = 8.0 \text{ V to 16 V, } I_{\text{O}} = 175 \text{ mA}$</td>
<td>$30 \text{ mV} = \pm 0.05%$</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>$V_{\text{in}} = 12 \text{ V, } I_{\text{O}} = 75 \text{ mA to 175 mA}$</td>
<td>$10 \text{ mV} = \pm 0.017%$</td>
</tr>
<tr>
<td>Output Ripple</td>
<td>$V_{\text{in}} = 12 \text{ V, } I_{\text{O}} = 175 \text{ mA}$</td>
<td>$400 \text{ mVpp}$</td>
</tr>
<tr>
<td>Efficiency</td>
<td>$V_{\text{in}} = 12 \text{ V, } I_{\text{O}} = 175 \text{ mA}$</td>
<td>$87.7%$</td>
</tr>
<tr>
<td>Output Ripple With Optional Filter</td>
<td>$V_{\text{in}} = 12 \text{ V, } I_{\text{O}} = 175 \text{ mA}$</td>
<td>$40 \text{ mVpp}$</td>
</tr>
</tbody>
</table>

**Figure 9. Step-Up Converter**
Figure 10. External Current Boost Connections for \( I_C \) Peak Greater than 1.5 A

9a. External NPN Switch

9b. External NPN Saturated Switch

(See Note 8)

8. If the output switch is driven into hard saturation (non-Darlington configuration) at low switch currents \( \leq 300 \text{ mA} \) and high driver currents \( \geq 30 \text{ mA} \), it may take up to 2.0 \( \mu s \) to come out of saturation. This condition will shorten the off time at frequencies \( \geq 30 \text{ kHz} \), and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non-Darlington configuration is used, the following output drive condition is recommended.
MC34063A, MC33063A, SC34063A, SC33063A, NCV33063A

<table>
<thead>
<tr>
<th>Test</th>
<th>Conditions</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line Regulation</td>
<td>$V_{in} = 15$ V to 25 V, $I_O = 500$ mA</td>
<td>12 mV = ±0.12%</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>$V_{in} = 25$ V, $I_O = 50$ mA to 500 mA</td>
<td>3.0 mV = ±0.03%</td>
</tr>
<tr>
<td>Output Ripple</td>
<td>$V_{in} = 25$ V, $I_O = 500$ mA</td>
<td>120 mVpp</td>
</tr>
<tr>
<td>Short Circuit Current</td>
<td>$V_{in} = 25$ V, $R_L = 0.1$ Ω</td>
<td>1.1 A</td>
</tr>
<tr>
<td>Efficiency</td>
<td>$V_{in} = 25$ V, $I_O = 500$ mA</td>
<td>83.7%</td>
</tr>
<tr>
<td>Output Ripple With Optional Filter</td>
<td>$V_{in} = 25$ V, $I_O = 500$ mA</td>
<td>40 mVpp</td>
</tr>
</tbody>
</table>

**Figure 11. Step-Down Converter**

**Figure 12. External Current Boost Connections for $I_C$ Peak Greater than 1.5 A**

11a. External NPN Switch

11b. External PNP Saturated Switch
### Test Conditions

<table>
<thead>
<tr>
<th>Test</th>
<th>Conditions</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line Regulation</td>
<td>$V_{in} = 4.5 \text{ V to } 6.0 \text{ V}, I_O = 100 \text{ mA}$</td>
<td>$3.0 \text{ mV} = \pm 0.012%$</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>$V_{in} = 5.0 \text{ V}, I_O = 10 \text{ mA} \text{ to } 100 \text{ mA}$</td>
<td>$0.022 \text{ V} = \pm 0.09%$</td>
</tr>
<tr>
<td>Output Ripple</td>
<td>$V_{in} = 5.0 \text{ V}, I_O = 100 \text{ mA}$</td>
<td>$500 \text{ mVpp}$</td>
</tr>
<tr>
<td>Short Circuit Current</td>
<td>$V_{in} = 5.0 \text{ V}, R_L = 0.1 \Omega$</td>
<td>$910 \text{ mA}$</td>
</tr>
<tr>
<td>Efficiency</td>
<td>$V_{in} = 5.0 \text{ V}, I_O = 100 \text{ mA}$</td>
<td>$62.2%$</td>
</tr>
<tr>
<td>Output Ripple With Optional Filter</td>
<td>$V_{in} = 5.0 \text{ V}, I_O = 100 \text{ mA}$</td>
<td>$70 \text{ mVpp}$</td>
</tr>
</tbody>
</table>

Figure 13. Voltage Inverting Converter

Figure 14. External Current Boost Connections for $I_C$ Peak Greater than 1.5 A

13a. External NPN Switch

13b. External PNP Saturated Switch
**INDUCTOR DATA**

<table>
<thead>
<tr>
<th>Converter</th>
<th>Inductance (μH)</th>
<th>Turns/Wire</th>
</tr>
</thead>
<tbody>
<tr>
<td>Step–Up</td>
<td>170</td>
<td>38 Turns of #22 AWG</td>
</tr>
<tr>
<td>Step–Down</td>
<td>220</td>
<td>48 Turns of #22 AWG</td>
</tr>
<tr>
<td>Voltage–Inverting</td>
<td>88</td>
<td>28 Turns of #22 AWG</td>
</tr>
</tbody>
</table>

All inductors are wound on Magnetics Inc. 55117 toroidal core.
Figure 16. Printed Circuit Board for DFN Device
### MC34063A, MC33063A, SC34063A, SC33063A, NCV33063A

#### Calculation Table

<table>
<thead>
<tr>
<th>Calculation</th>
<th>Step-Up</th>
<th>Step-Down</th>
<th>Voltage-Inverting</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{on}/t_{off} )</td>
<td>( V_{out} + V_F - V_{in(min)} ) ( V_{in(min)} - V_{sat} )</td>
<td>( V_{out} + V_F ) ( V_{in(min)} - V_{sat} - V_{out} )</td>
<td>(</td>
</tr>
<tr>
<td>( t_{on} + t_{off} )</td>
<td>( 1/T )</td>
<td>( 1/T )</td>
<td>( 1/T )</td>
</tr>
<tr>
<td>( t_{off} )</td>
<td>( t_{on} + t_{off} ) ( t_{off} + 1 )</td>
<td>( t_{on} + t_{off} ) ( t_{off} + 1 )</td>
<td>( t_{on} + t_{off} ) ( t_{off} + 1 )</td>
</tr>
<tr>
<td>( t_{on} )</td>
<td>( (t_{on} + t_{off}) - t_{off} )</td>
<td>( (t_{on} + t_{off}) - t_{off} )</td>
<td>( (t_{on} + t_{off}) - t_{off} )</td>
</tr>
<tr>
<td>( C_T )</td>
<td>( 4.0 \times 10^{-5} t_{on} )</td>
<td>( 4.0 \times 10^{-5} t_{on} )</td>
<td>( 4.0 \times 10^{-5} t_{on} )</td>
</tr>
<tr>
<td>( I_{pk(switch)} )</td>
<td>( 2I_{out(max)} \left( \frac{t_{on}}{t_{off}} + 1 \right) )</td>
<td>( 2I_{out(max)} )</td>
<td>( 2I_{out(max)} \left( \frac{t_{on}}{t_{off}} + 1 \right) )</td>
</tr>
<tr>
<td>( R_{sc} )</td>
<td>( 0.3/I_{pk(switch)} )</td>
<td>( 0.3/I_{pk(switch)} )</td>
<td>( 0.3/I_{pk(switch)} )</td>
</tr>
<tr>
<td>( L_{(min)} )</td>
<td>( \left( \frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}} \right) t_{on(max)} )</td>
<td>( \left( \frac{V_{in(min)} - V_{sat} - V_{out}}{I_{pk(switch)}} \right) t_{on(max)} )</td>
<td>( \left( \frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}} \right) t_{on(max)} )</td>
</tr>
<tr>
<td>( C_O )</td>
<td>( \frac{9I_{out(ton)}}{V_{ripple(pp)}} )</td>
<td>( \frac{I_{pk(switch)}(t_{on} + t_{off})}{8V_{ripple(pp)}} )</td>
<td>( \frac{9I_{out(ton)}}{V_{ripple(pp)}} )</td>
</tr>
</tbody>
</table>

**Note:**

- \( V_{sat} = \) Saturation voltage of the output switch.
- \( V_F = \) Forward voltage drop of the output rectifier.

**The following power supply characteristics must be chosen:**

- \( V_{in} = \) Nominal input voltage.
- \( V_{out} = \) Desired output voltage, \( |V_{out}| = 1.25 \left( 1 + \frac{R_2}{R_1} \right) \)
- \( I_{out} = \) Desired output current.
- \( f_{min} = \) Minimum desired output switching frequency at the selected values of \( V_{in} \) and \( I_{out} \).
- \( V_{ripple(pp)} = \) Desired peak-to-peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

**NOTE:**

For further information refer to Application Note AN920A/D and AN954/D.

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**Figure 17. Design Formula Table**
# ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package</th>
<th>Shipping</th>
</tr>
</thead>
<tbody>
<tr>
<td>MC33063ADG</td>
<td>SOIC–8 (Pb–Free)</td>
<td>98 Units / Rail</td>
</tr>
<tr>
<td>MC33063ADR2G</td>
<td>SOIC–8 (Pb–Free)</td>
<td>2500 Units / Tape &amp; Reel</td>
</tr>
<tr>
<td>SC33063ADR2G</td>
<td>SOIC–8 (Pb–Free)</td>
<td>2500 Units / Tape &amp; Reel</td>
</tr>
<tr>
<td>MC33063AP1G</td>
<td>PDIP–8 (Pb–Free)</td>
<td>50 Units / Rail</td>
</tr>
<tr>
<td>MC33063AVDG</td>
<td>SOIC–8 (Pb–Free)</td>
<td>98 Units / Rail</td>
</tr>
<tr>
<td>MC33063AVDR2G</td>
<td>SOIC–8 (Pb–Free)</td>
<td>2500 Units / Tape &amp; Reel</td>
</tr>
<tr>
<td>NCV33063AVDR2G*</td>
<td>SOIC–8 (Pb–Free)</td>
<td>2500 Units / Tape &amp; Reel</td>
</tr>
<tr>
<td>MC33063AVPG</td>
<td>PDIP–8 (Pb–Free)</td>
<td>50 Units / Rail</td>
</tr>
<tr>
<td>MC34063ADG</td>
<td>SOIC–8 (Pb–Free)</td>
<td>98 Units / Rail</td>
</tr>
<tr>
<td>MC34063ADR2G</td>
<td>SOIC–8 (Pb–Free)</td>
<td>2500 Units / Tape &amp; Reel</td>
</tr>
<tr>
<td>SC34063ADR2G</td>
<td>SOIC–8 (Pb–Free)</td>
<td>2500 Units / Tape &amp; Reel</td>
</tr>
<tr>
<td>MC34063AP1G</td>
<td>PDIP–8 (Pb–Free)</td>
<td>50 Units / Rail</td>
</tr>
<tr>
<td>SC34063AP1G</td>
<td>PDIP–8 (Pb–Free)</td>
<td>50 Units / Rail</td>
</tr>
<tr>
<td>MC33063MNTXG</td>
<td>DFN8 (Pb–Free)</td>
<td>4000 Units / Tape &amp; Reel</td>
</tr>
</tbody>
</table>

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*Ncv33063A: \( T_{\text{low}} = -40^\circ\text{C}, T_{\text{high}} = +125^\circ\text{C} \). Guaranteed by design. NCV prefix is for automotive and other applications requiring site and change control.
# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

**DFN8, 4x4**  
**CASE 488AF-01**  
**ISSUE C**

### NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DETAILS A AND B SHOW OPTIONAL CONSTRUCTIONS FOR TERMINALS.

### DIMENSIONS: MILLIMETERS

<table>
<thead>
<tr>
<th>DIM</th>
<th>MIN</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.80</td>
<td>1.00</td>
</tr>
<tr>
<td>A1</td>
<td>0.00</td>
<td>0.05</td>
</tr>
<tr>
<td>A3</td>
<td>0.20</td>
<td>REF</td>
</tr>
<tr>
<td>b</td>
<td>0.25</td>
<td>0.35</td>
</tr>
<tr>
<td>D</td>
<td>4.00</td>
<td>BSC</td>
</tr>
<tr>
<td>D2</td>
<td>1.91</td>
<td>2.21</td>
</tr>
<tr>
<td>E</td>
<td>4.00</td>
<td>BSC</td>
</tr>
<tr>
<td>E2</td>
<td>2.09</td>
<td>2.38</td>
</tr>
<tr>
<td>e</td>
<td>0.80</td>
<td>BSC</td>
</tr>
<tr>
<td>K</td>
<td>0.20</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>0.30</td>
<td>0.50</td>
</tr>
<tr>
<td>L1</td>
<td>0.15</td>
<td></td>
</tr>
</tbody>
</table>

### GENERIC MARKING DIAGRAM*

```
<table>
<thead>
<tr>
<th>XXXX</th>
<th>XXXX</th>
<th>ALYW*</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "*", may or may not be present.

---

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.*

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**DOCUMENT NUMBER:** 98AON15232D  
**DESCRIPTION:** DFN8, 4X4, 0.8P  
**PAGE 1 OF 1**

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PDIP-8
CASE 626–05
ISSUE P

DATE 22 APR 2015

NOTES:
2. CONTROLLING DIMENSION: INCHES.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION b2 IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

### GENERIC MARKING DIAGRAM*

- XXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot "*", may or may not be present.

**MECHANICAL CASE OUTLINE**

**PACKAGE DIMENSIONS**

<table>
<thead>
<tr>
<th>DIM MIN</th>
<th>MAX INCHES</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.015</td>
<td>0.38</td>
</tr>
<tr>
<td>A1</td>
<td>0.115</td>
<td>2.92</td>
</tr>
<tr>
<td>b</td>
<td>0.014</td>
<td>0.35</td>
</tr>
<tr>
<td>b2</td>
<td>0.000 TYP</td>
<td>1.52</td>
</tr>
<tr>
<td>C</td>
<td>0.008</td>
<td>0.20</td>
</tr>
<tr>
<td>D</td>
<td>0.355</td>
<td>9.02</td>
</tr>
<tr>
<td>D1</td>
<td>0.005</td>
<td>0.13</td>
</tr>
<tr>
<td>E</td>
<td>0.300</td>
<td>7.62</td>
</tr>
<tr>
<td>E1</td>
<td>0.240</td>
<td>6.10</td>
</tr>
<tr>
<td>e</td>
<td>0.100 BSC</td>
<td>2.54 BSC</td>
</tr>
<tr>
<td>eB</td>
<td>0.115</td>
<td>2.92</td>
</tr>
<tr>
<td>L</td>
<td>0.115</td>
<td>2.92</td>
</tr>
<tr>
<td>M</td>
<td>0.250</td>
<td>6.35</td>
</tr>
</tbody>
</table>

### STYLE 1:

- PIN 1. AC IN
- 2. DC + IN
- 3. DC – IN
- 4. AC IN
- 5. GROUND
- 6. OUTPUT
- 7. AUXILIARY
- 8. V CC

**DOCUMENT NUMBER:** 98ASB42420B

**DESCRIPTION:** PDIP-8

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**MECHANICAL CASE OUTLINE**

**PACKAGE DIMENSIONS**

**SOIC-8 NB**

**CASE 751-07**

**ISSUE AK**

**DATE 16 FEB 2011**

**NOTES:**

2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

**DIMENSIONS IN MILLIMETERS:**

<table>
<thead>
<tr>
<th>DIM</th>
<th>MIN</th>
<th>MAX</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>4.80</td>
<td>5.00</td>
<td>0.189 0.197</td>
</tr>
<tr>
<td>B</td>
<td>3.80</td>
<td>4.00</td>
<td>0.150 0.157</td>
</tr>
<tr>
<td>C</td>
<td>1.35</td>
<td>1.75</td>
<td>0.053 0.063</td>
</tr>
<tr>
<td>D</td>
<td>0.53</td>
<td>0.51</td>
<td>0.020</td>
</tr>
<tr>
<td>G</td>
<td>1.27</td>
<td>1.52</td>
<td>0.050</td>
</tr>
<tr>
<td>H</td>
<td>0.10</td>
<td>0.25</td>
<td>0.004 0.010</td>
</tr>
<tr>
<td>J</td>
<td>0.19</td>
<td>0.26</td>
<td>0.007 0.010</td>
</tr>
<tr>
<td>K</td>
<td>0.40</td>
<td>1.27</td>
<td>0.016 0.050</td>
</tr>
<tr>
<td>M</td>
<td>0</td>
<td>8</td>
<td>0  8</td>
</tr>
<tr>
<td>N</td>
<td>0.25</td>
<td>0.50</td>
<td>0.010 0.020</td>
</tr>
<tr>
<td>S</td>
<td>5.80</td>
<td>6.20</td>
<td>0.228 0.244</td>
</tr>
</tbody>
</table>

**SCALE 1:1**

**NOTES:**

- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
- 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

**SCALE 6:1**

**SOLDERING FOOTPRINT**

**GENERIC MARKING DIAGRAM**

**GENERAL INFORMATION:**

- **IC:** Specific Device Code
- **IC (Pb-Free):** Specific Device Code
- **Discrete:** Specific Device Code
- **Discrete (Pb-Free):** Specific Device Code

**STYLES ON PAGE 2**

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**STYLE 1:**
- **PIN 1. Emitter**
- **2. Source**
- **3. Collector**
- **4. Emitter**
- **5. Base**
- **6. Base**
- **7. Base**
- **8. Emitter**

**STYLE 2:**
- **PIN 1. Collector, Die #1**
- **2. Collector, Die #1**
- **3. Collector, Die #2**
- **4. Collector, Die #2**
- **5. Emitter, Common**
- **6. Emitter, #2**
- **7. Base, #1**
- **8. Emitter, #1**

**STYLE 3:**
- **PIN 1. Drain, Die #1**
- **2. Drain, Die #1**
- **3. Drain, #2**
- **4. Drain, #2**
- **5. Base, #2**
- **6. Source, #2**
- **7. Gate, #1**
- **8. Source, #1**

**STYLE 4:**
- **PIN 1. Anode**
- **2. Base, Die #1**
- **3. Base, Die #2**
- **4. Collector, Die #2**
- **5. Collector, #2**
- **6. Emitter, #2**
- **7. Anode**
- **8. Common Cathode**

**STYLE 5:**
- **PIN 1. Drain**
- **2. Drain**
- **3. Drain**
- **4. Drain**
- **5. Gate**
- **6. Gate**
- **7. Source**
- **8. Source**

**STYLE 6:**
- **PIN 1. Source**
- **2. Drain**
- **3. Drain**
- **4. Source**
- **5. Source**
- **6. Gate**
- **7. Gate**
- **8. Source**

**STYLE 7:**
- **PIN 1. Input**
- **2. External Bypass**
- **3. Third Stage Source**
- **4. Ground**
- **5. Drain**
- **6. Gate**
- **7. Second Stage Vd**
- **8. First Stage Vd**

**STYLE 8:**
- **PIN 1. Collector, Die #1**
- **2. Base, #1**
- **3. Base, #2**
- **4. Collector, #2**
- **5. Collector, #2**
- **6. Emitter, #2**
- **7. Anode**
- **8. Drain**

**STYLE 9:**
- **PIN 1. Emitter, Common**
- **2. Collector, Die #1**
- **3. Collector, Die #2**
- **4. Emitter, Common**
- **5. Emitter, Common**
- **6. Base, Die #2**
- **7. Base, Die #1**
- **8. Emitter, Common**

**STYLE 10:**
- **PIN 1. Ground**
- **2. Bias 1**
- **3. Output**
- **4. Ground**
- **5. Gate**
- **6. Gate**
- **7. Input**
- **8. Drain**

**STYLE 11:**
- **PIN 1. Source**
- **2. Gate**
- **3. Source**
- **4. Gate**
- **5. Drain**
- **6. Drain**
- **7. Drain**
- **8. Drain**

**STYLE 12:**
- **PIN 1. Source**
- **2. Gate**
- **3. Source**
- **4. Gate**
- **5. Drain**
- **6. Drain**
- **7. Drain**
- **8. Drain**

**STYLE 13:**
- **PIN 1. N.C.**
- **2. Source**
- **3. Source**
- **4. Gate**
- **5. Drain**
- **6. Gate**
- **7. Drain**
- **8. Drain**

**STYLE 14:**
- **PIN 1. N-Source**
- **2. Source**
- **3. P-Source**
- **4. P-Gate**
- **5. P-Drain**
- **6. P-Drain**
- **7. N-Drain**
- **8. N-Drain**

**STYLE 15:**
- **PIN 1. Anode**
- **2. Anode**
- **3. Anode**
- **4. Anode**
- **5. Cathode, Common**
- **6. Cathode, Common**
- **7. Cathode, Common**
- **8. Collector, Die #1**

**STYLE 16:**
- **PIN 1. Collector, Die #1**
- **2. Base, Die #1**
- **3. Emitter, Die #2**
- **4. Base, Die #2**
- **5. Collector, Die #2**
- **6. Collector, Die #2**
- **7. Collector, Die #1**
- **8. Collector, Die #1**

**STYLE 17:**
- **PIN 1. Vcc**
- **2. V2Out**
- **3. V1Out**
- **4. Txe**
- **5. Rx**
- **6. Yee**
- **7. Gnd**
- **8. Acc**

**STYLE 18:**
- **PIN 1. Anode**
- **2. Gate**
- **3. Source**
- **4. Gate**
- **5. Drain**
- **6. Mirror**
- **7. Drain**
- **8. Drain**

**STYLE 19:**
- **PIN 1. Source**
- **2. Gate**
- **3. Source**
- **4. Gate**
- **5. Drain**
- **6. Drain**
- **7. Drain**
- **8. Drain**

**STYLE 20:**
- **PIN 1. Source (N)**
- **2. Gate (N)**
- **3. Source (P)**
- **4. Gate (P)**
- **5. Drain**
- **6. Drain**
- **7. Drain**
- **8. Drain**

**STYLE 21:**
- **PIN 1. Cathode 1**
- **2. Cathode 2**
- **3. Cathode 3**
- **4. Cathode 4**
- **5. Cathode 5**
- **6. Common Anode**
- **7. Common Anode**
- **8. Cathode 6**

**STYLE 22:**
- **PIN 1. I/O Line 1**
- **2. Common Cathode/Vcc**
- **3. Common Cathode/Vcc**
- **4. Line 2**
- **5. Line 2**
- **6. Line 4**
- **7. Line 5**
- **8. Common Anode/Gnd**

**STYLE 23:**
- **PIN 1. Line 1 In**
- **2. Common Anode/Gnd**
- **3. Common Anode/Gnd**
- **4. Line 2 In**
- **5. Line 2 Out**
- **6. Common Anode/Gnd**
- **7. Common Anode/Gnd**
- **8. Line 1 Out**

**STYLE 24:**
- **PIN 1. Base**
- **2. Emitter**
- **3. Collector/Anode**
- **4. Collector/Anode**
- **5. Cathode**
- **6. Cathode**
- **7. Collector/Anode**
- **8. Collector/Anode**

**STYLE 25:**
- **PIN 1. Vin**
- **2. N/C**
- **3. Rext**
- **4. Gnd**
- **5. Iout**
- **6. Iout**
- **7. Iout**
- **8. Iout**

**STYLE 26:**
- **PIN 1. Gnd**
- **2. Avdd**
- **3. Ena**
- **4. Ilimit**
- **5. Source**
- **6. Source**
- **7. Source**
- **8. Drain**

**STYLE 27:**
- **PIN 1. Ilimit**
- **2. Ovlo**
- **3. Uvlo**
- **4. Input**
- **5. Source**
- **6. Source**
- **7. Source**
- **8. Drain**

**STYLE 28:**
- **PIN 1. Sw_to_Gnd**
- **2. Basic Off**
- **3. Basic SW Det**
- **4. Gnd**
- **5. V_mon**
- **6. V_bulb**
- **7. V_bulb**
- **8. Vin**

**DOCUMENT NUMBER:** 98ASB42564B **DESCRIPTION:** SOIC–8 NB

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