Low Voltage, Rail-to-Rail Operational Amplifiers

MC33201, MC33202, MC33204, NCV33201, NCV33202, NCV33204

The MC33201/2/4 family of operational amplifiers provide rail–to–rail operation on both the input and output. The inputs can be driven as high as 200 mV beyond the supply rails without phase reversal on the outputs, and the output can swing within 50 mV of each rail. This rail–to–rail operation enables the user to make full use of the supply voltage range available. It is designed to work at very low supply voltages (± 0.9 V) yet can operate with a supply of up to +12 V and ground. Output current boosting techniques provide a high output current capability while keeping the drain current of the amplifier to a minimum. Also, the combination of low noise and distortion with a high slew rate and drive capability make this an ideal amplifier for audio applications.

Features
- Low Voltage, Single Supply Operation (+1.8 V and Ground to +12 V and Ground)
- Input Voltage Range Includes both Supply Rails
- Output Voltage Swings within 50 mV of both Rails
- No Phase Reversal on the Output for Over–driven Input Signals
- High Output Current (I_{SC} = 80 mA, Typ)
- Low Supply Current (I_{P} = 0.9 mA, Typ)
- 600 Ω Output Drive Capability
- Extended Operating Temperature Ranges (−40° to +105°C and −55° to +125°C)
- Typical Gain Bandwidth Product = 2.2 MHz
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
- These Devices are Pb–Free and are RoHS Compliant

ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 10 of this data sheet.
This device contains 70 active transistors (each amplifier).

Figure 1. Circuit Schematic
(Each Amplifier)
### MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (VCC to VEE)</td>
<td>V_S</td>
<td>+13 V</td>
<td>V</td>
</tr>
<tr>
<td>Input Differential Voltage Range</td>
<td>V_IDR</td>
<td>Note 1</td>
<td>V</td>
</tr>
<tr>
<td>Common Mode Input Voltage Range (Note 2)</td>
<td>V_CM</td>
<td>V_CC + 0.5 V to V_EE − 0.5 V</td>
<td>V</td>
</tr>
<tr>
<td>Output Short Circuit Duration</td>
<td>t_s</td>
<td>Note 3</td>
<td>sec</td>
</tr>
<tr>
<td>Maximum Junction Temperature</td>
<td>T_J</td>
<td>+150 °C</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>T_stg</td>
<td>−65 to +150 °C</td>
<td></td>
</tr>
<tr>
<td>Maximum Power Dissipation</td>
<td>P_D</td>
<td>Note 3</td>
<td>mW</td>
</tr>
</tbody>
</table>

### DC ELECTRICAL CHARACTERISTICS (TA = 25°C)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>V_CC = 2.0 V</th>
<th>V_CC = 3.3 V</th>
<th>V_CC = 5.0 V</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Offset Voltage VIO (max)</td>
<td>± 8.0 V</td>
<td>± 8.0 V</td>
<td>± 6.0 V</td>
<td>mV</td>
</tr>
<tr>
<td>MC33201, NCV33201V</td>
<td>± 10 V</td>
<td>± 10 V</td>
<td>± 8.0 V</td>
<td></td>
</tr>
<tr>
<td>MC33202, NCV33202, V</td>
<td>± 12 V</td>
<td>± 12 V</td>
<td>± 10 V</td>
<td></td>
</tr>
<tr>
<td>Output Voltage Swing VOH (RL = 10 kΩ)</td>
<td>1.9 V</td>
<td>3.15 V</td>
<td>4.85 V</td>
<td>V_max</td>
</tr>
<tr>
<td>VOL (RL = 10 kΩ)</td>
<td>0.10 V</td>
<td>0.15 V</td>
<td>0.15 V</td>
<td>V_min</td>
</tr>
<tr>
<td>Power Supply Current per Amplifier (I_D)</td>
<td>1.125 mA</td>
<td>1.125 mA</td>
<td>1.125 mA</td>
<td></td>
</tr>
</tbody>
</table>

Specifications at V_CC = 3.3 V are guaranteed by the 2.0 V and 5.0 V tests. V_EE = GND.

### DC ELECTRICAL CHARACTERISTICS (V_CC = +5.0 V, V_EE = Ground, TA = 25°C, unless otherwise noted.)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Figure</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Offset Voltage (V_CM = 1.0 V to 5.0 V)</td>
<td>3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MC33201: T_A = +25°C</td>
<td>-</td>
<td>-</td>
<td>6.0</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>MC33201: T_A = −40° to +105°C</td>
<td>-</td>
<td>-</td>
<td>9.0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MC33202: T_A = −55° to +125°C</td>
<td>-</td>
<td>-</td>
<td>13</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MC33202: T_A = +25°C</td>
<td>-</td>
<td>-</td>
<td>8.0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MC33202: T_A = −40° to +105°C</td>
<td>-</td>
<td>-</td>
<td>11</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MC33202V: T_A = −55° to +125°C (Note 4)</td>
<td>-</td>
<td>-</td>
<td>14</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MC33204: T_A = +25°C</td>
<td>-</td>
<td>-</td>
<td>10</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MC33204: T_A = −40° to +105°C</td>
<td>-</td>
<td>-</td>
<td>13</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MC33204V: T_A = −55° to +125°C (Note 4)</td>
<td>-</td>
<td>-</td>
<td>17</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Offset Voltage Temperature Coefficient (R_S = 50 Ω)</td>
<td>4</td>
<td></td>
<td>2.0</td>
<td>2.0</td>
<td></td>
<td>mV/°C</td>
</tr>
<tr>
<td>T_A = −40° to +105°C</td>
<td>-</td>
<td>-</td>
<td>9.0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T_A = −55° to +125°C</td>
<td>-</td>
<td>-</td>
<td>11</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Bias Current (V_CM = 0 V to 0.5 V)</td>
<td>5, 6</td>
<td></td>
<td>80</td>
<td>200</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>T_A = +25°C</td>
<td>-</td>
<td>-</td>
<td>100</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T_A = −40° to +105°C</td>
<td>-</td>
<td>-</td>
<td>250</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T_A = −55° to +125°C</td>
<td>-</td>
<td>-</td>
<td>500</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The differential input voltage of each amplifier is limited by two internal parallel back−back diodes. For additional differential input voltage range, use current limiting resistors in series with the input pins.
2. The input common mode voltage range is limited by internal diodes connected from the inputs to both supply rails. Therefore, the voltage on either input must not exceed either supply rail by more than 500 mV.
3. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded. (See Figure 2)
4. All NCV devices are qualified for Automotive use.
### DC ELECTRICAL CHARACTERISTICS (cont.)

**(VCC = + 5.0 V, VEE = Ground, TA = 25°C, unless otherwise noted.)**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Figure</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Offset Current (VCM = 0 V to 0.5 V, VCM = 1.0 V to 5.0 V)</td>
<td></td>
<td>IIO</td>
<td>⌈</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>TA = + 25°C</td>
<td></td>
<td></td>
<td>5.0</td>
<td>50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TA = − 40° to +105°C</td>
<td></td>
<td></td>
<td>10</td>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TA = − 55° to +125°C</td>
<td></td>
<td></td>
<td>200</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Common Mode Input Voltage Range</td>
<td></td>
<td>VCR</td>
<td>VEE</td>
<td>VCC</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Large Signal Voltage Gain (VCC = + 5.0 V, VEE = − 5.0 V)</td>
<td>7</td>
<td>AVOL</td>
<td>50</td>
<td>300</td>
<td></td>
<td>kV/V</td>
</tr>
<tr>
<td>RL = 10 kΩ</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RL = 600 Ω</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Voltage Swing (VID = ± 0.2 V)</td>
<td>8, 9, 10</td>
<td>VOH</td>
<td>4.85</td>
<td>4.95</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>RL = 10 kΩ</td>
<td></td>
<td></td>
<td>0.05</td>
<td>0.15</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RL = 600 Ω</td>
<td></td>
<td></td>
<td>4.75</td>
<td>4.85</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RL = 600 Ω</td>
<td></td>
<td></td>
<td>0.15</td>
<td>0.25</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Common Mode Rejection (Vin = 0 V to 5.0 V)</td>
<td>11</td>
<td>CMR</td>
<td>60</td>
<td>90</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Power Supply Rejection Ratio</td>
<td>12</td>
<td>PSRR</td>
<td>500</td>
<td>25</td>
<td></td>
<td>μV/V</td>
</tr>
<tr>
<td>VCC/VEE = 5.0 V/GND to 3.0 V/GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Short Circuit Current (Source and Sink)</td>
<td>13, 14</td>
<td>ISC</td>
<td>50</td>
<td>80</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Power Supply Current per Amplifier (VO = 0 V)</td>
<td>15</td>
<td>ID</td>
<td></td>
<td>0.9</td>
<td>1.125</td>
<td>mA</td>
</tr>
<tr>
<td>TA = − 40° to +105°C</td>
<td></td>
<td></td>
<td></td>
<td>0.9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TA = − 55° to +125°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### AC ELECTRICAL CHARACTERISTICS

**(VCC = + 5.0 V, VEE = Ground, TA = 25°C, unless otherwise noted.)**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Figure</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slew Rate (VS = ± 2.5 V, VO = − 2.0 V to + 2.0 V, RL = 2.0 kΩ, AV = +1.0)</td>
<td>16, 26</td>
<td>SR</td>
<td>0.5</td>
<td>1.0</td>
<td></td>
<td>V/μs</td>
</tr>
<tr>
<td>Gain Bandwidth Product (f = 100 kHz)</td>
<td>17</td>
<td>GBW</td>
<td></td>
<td>2.2</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Gain Margin (RL = 600 Ω, CL = 0 pF)</td>
<td>20, 21, 22</td>
<td>AM</td>
<td></td>
<td>12</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Phase Margin (RL = 600 Ω, CL = 0 pF)</td>
<td>20, 21, 22</td>
<td>PM</td>
<td></td>
<td>65</td>
<td></td>
<td>Deg</td>
</tr>
<tr>
<td>Channel Separation (f = 1.0 Hz to 20 kHz, AV = 100)</td>
<td>23</td>
<td>CS</td>
<td></td>
<td>90</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Power Bandwidth (VO = 4.0 Vpp, RL = 600 Ω, THD ≤ 1 %)</td>
<td>23</td>
<td>BW</td>
<td></td>
<td>28</td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>Total Harmonic Distortion (RL = 600 Ω, VO = 1.0 Vpp, AV = 1.0)</td>
<td>24</td>
<td>THD</td>
<td></td>
<td>0.002</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>f = 1.0 kHz</td>
<td></td>
<td></td>
<td></td>
<td>0.008</td>
<td></td>
<td></td>
</tr>
<tr>
<td>f = 10 kHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Open Loop Output Impedance (VO = 0 V, f = 2.0 MHz, AV = 10)</td>
<td></td>
<td>ZO</td>
<td></td>
<td>100</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Differential Input Resistance (VCM = 0 V)</td>
<td></td>
<td>Rin</td>
<td></td>
<td>200</td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td>Differential Input Capacitance (VCM = 0 V)</td>
<td></td>
<td>Cin</td>
<td></td>
<td>8.0</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Equivalent Input Noise Voltage (RS = 100 Ω)</td>
<td>25</td>
<td>e</td>
<td>n</td>
<td></td>
<td>25</td>
<td></td>
</tr>
<tr>
<td>f = 10 Hz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>f = 1.0 kHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Equivalent Input Noise Current</td>
<td>25</td>
<td>In</td>
<td></td>
<td>0.8</td>
<td></td>
<td>pA/√Hz</td>
</tr>
<tr>
<td>f = 10 Hz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>f = 1.0 kHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Figure 2. Maximum Power Dissipation versus Temperature

Figure 3. Input Offset Voltage Distribution

Figure 4. Input Offset Voltage Temperature Coefficient Distribution

Figure 5. Input Bias Current versus Temperature

Figure 6. Input Bias Current versus Common Mode Voltage

Figure 7. Open Loop Voltage Gain versus Temperature
Figure 14. Output Short Circuit Current versus Temperature

Figure 15. Supply Current per Amplifier versus Supply Voltage with No Load

Figure 16. Slew Rate versus Temperature

Figure 17. Gain Bandwidth Product versus Temperature

Figure 18. Voltage Gain and Phase versus Frequency

Figure 19. Voltage Gain and Phase versus Frequency
Figure 20. Gain and Phase Margin versus Temperature

Figure 21. Gain and Phase Margin versus Differential Source Resistance

Figure 22. Gain and Phase Margin versus Capacitive Load

Figure 23. Channel Separation versus Frequency

Figure 24. Total Harmonic Distortion versus Frequency

Figure 25. Equivalent Input Noise Voltage and Current versus Frequency
DETAILED OPERATING DESCRIPTION

General Information

The MC33201/2/4 family of operational amplifiers are unique in their ability to swing rail-to-rail on both the input and the output with a completely bipolar design. This offers low noise, high output current capability and a wide common mode input voltage range even with low supply voltages. Operation is guaranteed over an extended temperature range and at supply voltages of 2.0 V, 3.3 V and 5.0 V and ground.

Since the common mode input voltage range extends from \( V_{CC} \) to \( V_{EE} \), it can be operated with either single or split voltage supplies. The MC33201/2/4 are guaranteed not to latch or phase reverse over the entire common mode range, however, the inputs should not be allowed to exceed maximum ratings.

Circuit Information

Rail-to-rail performance is achieved at the input of the amplifiers by using parallel NPN–PNP differential input stages. When the inputs are within 800 mV of the negative rail, the PNP stage is on. When the inputs are more than 800 mV greater than \( V_{EE} \), the NPN stage is on. This switching of input pairs will cause a reversal of input bias currents (see Figure 6). Also, slight differences in offset voltage may be noted between the NPN and PNP pairs. Cross-coupling techniques have been used to keep this change to a minimum.

In addition to its rail-to-rail performance, the output stage is current boosted to provide 80 mA of output current, enabling the op amp to drive 600 \( \Omega \) loads. Because of this high output current capability, care should be taken not to exceed the 150\(^\circ\)C maximum junction temperature.

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self-align when subjected to a solder reflow process.
## ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Operational Amplifier Function</th>
<th>Device</th>
<th>Operating Temperature Range</th>
<th>Package</th>
<th>Shipping†</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single</td>
<td>MC33201DR2G</td>
<td>$T_A = -40^\circ$ to $+105^\circ$C</td>
<td>SOIC–8 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>MC33201VDR2G</td>
<td>$T_A = -55^\circ$ to $+125^\circ$C</td>
<td>SOIC–8 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>NCV33201VDR2G</td>
<td></td>
<td>SOIC–8 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td>Dual</td>
<td>MC33202DR2G</td>
<td>$T_A = -40^\circ$ to $+105^\circ$C</td>
<td>Micro–8 (Pb–Free)</td>
<td>4000 / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>MC33202DMR2G</td>
<td></td>
<td>Micro–8 (Pb–Free)</td>
<td>4000 / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>NCV33202DMR2G*</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>MC33202VDR2G</td>
<td>$T_A = -55^\circ$ to $+125^\circ$C</td>
<td>SOIC–8 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>NCV33202VDR2G*</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Quad</td>
<td>MC33204DR2G</td>
<td>$T_A = -40^\circ$ to $+105^\circ$C</td>
<td>SO–14 (Pb–Free)</td>
<td>2500 Units / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>MC33204DTBR2G</td>
<td></td>
<td>SO–14 (Pb–Free)</td>
<td>2500 Units / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>NCV33204DR2G*</td>
<td></td>
<td>SO–14 (Pb–Free)</td>
<td>2500 Units / Tape &amp; Reel</td>
</tr>
<tr>
<td></td>
<td>NCV33204DTBR2G*</td>
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</tbody>
</table>

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable.

### MARKING DIAGRAMS

- **SOIC–8**
  - D SUFFIX
    - CASE 751
  - VD SUFFIX
    - CASE 751

- **TSSOP–14**
  - DTB SUFFIX
    - CASE 948G

- **Micro–8**
  - DM SUFFIX
    - CASE 846A

- **SO–14**
  - D SUFFIX
    - CASE 751A

- **SO–14**
  - VD SUFFIX
    - CASE 751A

---

x = 1 or 2  
A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G = Pb–Free Package  
* = Pb–Free Package  
(Note: Microdot may be in either location)

*This marking diagram applies to NCV3320xV  
**This marking diagram applies to NCV33202DMR2G
**NOTES:**

2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

**SOLDERING FOOTPRINT**

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “*”, may or may not be present. Some products may not follow the Generic Marking.

**GENERIC MARKING DIAGRAM**

**STYLES ON PAGE 2**
## Description

**SOIC–8 NB**  
CASE 751–07  
ISSUE AK  

**Date:** 16 FEB 2011

### Pin Configuration

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### Document Information

**Document Number:** 98ASB42564B  
**Page:** 2 of 2  
**Description:** SOIC–8 NB  
**Printed Version:** Uncontrolled except when stamped “CONTROLLED COPY” in red.
NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2
## STYLE 1:
- **PIN 1. COMMON CATHODE**
- 2. ANODE/CATHODE
- 3. ANODE/CATHODE
- 4. NO CONNECTION
- 5. ANODE/CATHODE
- 6. NO CONNECTION
- 7. ANODE/CATHODE
- 8. ANODE/CATHODE
- 9. ANODE/CATHODE
- 10. NO CONNECTION
- 11. ANODE/CATHODE
- 12. ANODE/CATHODE
- 13. NO CONNECTION
- 14. COMMON ANODE

## STYLE 2:
- CANCELLED

## STYLE 3:
- **PIN 1. NO CONNECTION**
- 2. ANODE
- 3. CATHODE
- 4. NO CONNECTION
- 5. ANODE
- 6. NO CONNECTION
- 7. ANODE
- 8. CATHODE
- 9. ANODE
- 10. NO CONNECTION
- 11. ANODE
- 12. CATHODE
- 13. NO CONNECTION
- 14. COMMON CATHODE

## STYLE 4:
- **PIN 1. NO CONNECTION**
- 2. ANODE
- 3. CATHODE
- 4. NO CONNECTION
- 5. ANODE
- 6. NO CONNECTION
- 7. ANODE
- 8. CATHODE
- 9. ANODE
- 10. NO CONNECTION
- 11. ANODE
- 12. CATHODE
- 13. NO CONNECTION
- 14. COMMON CATHODE

## STYLE 5:
- **PIN 1. COMMON CATHODE**
- 2. ANODE/CATHODE
- 3. ANODE/CATHODE
- 4. NO CONNECTION
- 5. ANODE/CATHODE
- 6. NO CONNECTION
- 7. COMMON CATHODE
- 8. COMMON CATHODE
- 9. ANODE/CATHODE
- 10. NO CONNECTION
- 11. ANODE/CATHODE
- 12. ANODE/CATHODE
- 13. NO CONNECTION
- 14. COMMON ANODE

## STYLE 6:
- **PIN 1. CATHODE**
- 2. CATHODE
- 3. CATHODE
- 4. NO CONNECTION
- 5. CATHODE
- 6. NO CONNECTION
- 7. CATHODE
- 8. CATHODE
- 9. CATHODE
- 10. NO CONNECTION
- 11. CATHODE
- 12. CATHODE
- 13. NO CONNECTION
- 14. COMMON ANODE

## STYLE 7:
- **PIN 1. ANODE/CATHODE**
- 2. COMMON ANODE
- 3. ANODE/CATHODE
- 4. ANODE/CATHODE
- 5. ANODE/CATHODE
- 6. ANODE/CATHODE
- 7. COMMON CATHODE
- 8. COMMON CATHODE
- 9. ANODE/CATHODE
- 10. ANODE/CATHODE
- 11. COMMON CATHODE
- 12. COMMON CATHODE
- 13. ANODE/CATHODE
- 14. ANODE/CATHODE

## STYLE 8:
- **PIN 1. COMMON CATHODE**
- 2. ANODE/CATHODE
- 3. ANODE/CATHODE
- 4. NO CONNECTION
- 5. ANODE/CATHODE
- 6. ANODE/CATHODE
- 7. COMMON ANODE
- 8. COMMON ANODE
- 9. ANODE/CATHODE
- 10. ANODE/CATHODE
- 11. NO CONNECTION
- 12. ANODE/CATHODE
- 13. ANODE/CATHODE
- 14. COMMON CATHODE
**MECHANICAL CASE OUTLINE**

**PACKAGE DIMENSIONS**

**DATE 16 JUL 2020**

**CASE 846A−02**

**ISSUE K**

---

**NOTES:**

2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION h DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE ± 0.01 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURNS. MOLD FLASH, PROTRUSIONS, OR GATE BURNS SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

---

**DIM**

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**GENERAL MARKING DIAGRAM**

**RECOMMENDED MOUNTING FOOTPRINT**

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

---

**DOCUMENT NUMBER:** 98ASB14087C

**DESCRIPTION:** MICRO8

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**MECHANICAL CASE OUTLINE**

**PACKAGE DIMENSIONS**

**TSSOP–14 WB**

**CASE 948G**

**ISSUE C**

**DATE 17 FEB 2016**

**NOTES:**

2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-. 

**SOLDERING FOOTPRINT**

**DIMENSIONS: MILLIMETERS**

**NOTES:**

- 0.15 (0.006) T U 
- 0.10 (0.004) T U 
- 0.10 (0.004) T U

**SCALE 2:1**

**ON Semiconductor**

**DOCUMENT NUMBER:** 98ASH70246A

**DESCRIPTION:** TSSOP–14 WB

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