Hex Level Shifter for TTL to CMOS or CMOS to CMOS

MC14504B

The MC14504B is a hex non–inverting level shifter using CMOS technology. The level shifter will shift a TTL signal to CMOS logic levels for any CMOS supply voltage between 5 and 15 volts. A control input also allows interface from CMOS to CMOS at one logic level to another logic level: Either up or down level translating is accomplished by selection of power supply levels VDD and VCC. The VCC level sets the input signal levels while VDD selects the output voltage levels.

Features

- UP Translates from a Low to a High Voltage or DOWN Translates from a High to a Low Voltage
- Input Threshold Can Be Shifted for TTL Compatibility
- No Sequencing Required on Power Supplies or Inputs for Power Up or Power Down
- 3 to 18 Vdc Operation for VDD and VCC
- Diode Protected Inputs to VSS
- Capable of Driving Two Low–Power TTL Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
- These Devices are Pb–Free and are RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to VSS)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>DC Supply Voltage Range</td>
<td>-0.5 to +18.0</td>
<td>V</td>
</tr>
<tr>
<td>VDD</td>
<td>DC Supply Voltage Range</td>
<td>-0.5 to +18.0</td>
<td>V</td>
</tr>
<tr>
<td>Vin</td>
<td>Input Voltage Range (DC or Transient)</td>
<td>-0.5 to +18.0</td>
<td>V</td>
</tr>
<tr>
<td>Vout</td>
<td>Output Voltage Range (DC or Transient)</td>
<td>-0.5 to VDD + 0.5</td>
<td>V</td>
</tr>
<tr>
<td>Iin, Iout</td>
<td>Input or Output Current (DC or Transient) per Pin</td>
<td>±10</td>
<td>mA</td>
</tr>
<tr>
<td>PD</td>
<td>Power Dissipation, per Package (Note 1)</td>
<td>500</td>
<td>mW</td>
</tr>
<tr>
<td>TA</td>
<td>Ambient Temperature Range</td>
<td>-55 to +125</td>
<td>°C</td>
</tr>
<tr>
<td>Tstg</td>
<td>Storage Temperature Range</td>
<td>-65 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>TL</td>
<td>Lead Temperature (8–Second Soldering)</td>
<td>260</td>
<td>°C</td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Packages: -7.0 mW/°C From 65°C To 125°C.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, Vin and Vout should be constrained to the range VSS ≤ (Vin or Vout) ≤ VDD.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.
**MC14504B**

**LOGIC DIAGRAM**

![Logic Diagram](image)

<table>
<thead>
<tr>
<th>Mode Select</th>
<th>Input Logic Levels</th>
<th>Output Logic Levels</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 ((V_{CC}))</td>
<td>TTL</td>
<td>CMOS</td>
</tr>
<tr>
<td>0 ((V_{SS}))</td>
<td>CMOS</td>
<td>CMOS</td>
</tr>
</tbody>
</table>

1/6 of package shown.

**ORDERING INFORMATION**

<table>
<thead>
<tr>
<th>Device</th>
<th>Package</th>
<th>Shipping†</th>
</tr>
</thead>
<tbody>
<tr>
<td>MC14504BDG</td>
<td>SOIC–16 (Pb–Free)</td>
<td>48 Units / Rail</td>
</tr>
<tr>
<td>MC14504BDR2G</td>
<td>SOIC–16 (Pb–Free)</td>
<td>2500 Units / Tape &amp; Reel</td>
</tr>
<tr>
<td>NLV14504BDR2G*</td>
<td>TSSOP–16 (Pb–Free)</td>
<td>96 Units / Rail</td>
</tr>
<tr>
<td>MC14504BDTR2G</td>
<td>TSSOP–16 (Pb–Free)</td>
<td>2500 Units / Tape &amp; Reel</td>
</tr>
<tr>
<td>NLV14504BDTR2G*</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011.D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable.
## ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>VCC</th>
<th>VDD</th>
<th>– 55°C</th>
<th>25°C</th>
<th>125°C</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Voltage</td>
<td></td>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>V&lt;sub&gt;in&lt;/sub&gt; = 0 V</td>
<td>V&lt;sub&gt;OL&lt;/sub&gt;</td>
<td>–5.0</td>
<td>–0.05</td>
<td></td>
<td>0</td>
<td>0.05</td>
<td>–0.05</td>
</tr>
<tr>
<td>V&lt;sub&gt;in&lt;/sub&gt; = V&lt;sub&gt;CC&lt;/sub&gt;</td>
<td>V&lt;sub&gt;OH&lt;/sub&gt;</td>
<td>–5.0</td>
<td>4.95</td>
<td>–4.95</td>
<td>5.0</td>
<td>–4.95</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td></td>
<td>–10</td>
<td>9.95</td>
<td>–9.95</td>
<td>10</td>
<td>9.95</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td></td>
<td>–15</td>
<td>14.95</td>
<td>–14.95</td>
<td>15</td>
<td>14.95</td>
<td>–</td>
</tr>
<tr>
<td>Input Voltage</td>
<td></td>
<td>V&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>–5.0</td>
<td>2.0</td>
<td>–2.0</td>
<td>1.5</td>
<td>–2.0</td>
</tr>
<tr>
<td>(V&lt;sub&gt;IL&lt;/sub&gt; = 1.0 Vdc) TTL–CMOS</td>
<td>–5.0</td>
<td>10</td>
<td>0.8</td>
<td>–1.3</td>
<td>0.8</td>
<td>–0.8</td>
<td>–</td>
</tr>
<tr>
<td>(V&lt;sub&gt;IL&lt;/sub&gt; = 1.5 Vdc) CMOS–CMOS</td>
<td>–5.0</td>
<td>15</td>
<td>1.5</td>
<td>–2.25</td>
<td>1.5</td>
<td>–1.4</td>
<td>–</td>
</tr>
<tr>
<td>(V&lt;sub&gt;IL&lt;/sub&gt; = 1.5 Vdc) CMOS–CMOS</td>
<td>–5.0</td>
<td>15</td>
<td>1.5</td>
<td>–2.25</td>
<td>1.5</td>
<td>–1.4</td>
<td>–</td>
</tr>
<tr>
<td>(V&lt;sub&gt;IL&lt;/sub&gt; = 1.5 Vdc) CMOS–CMOS</td>
<td>–5.0</td>
<td>15</td>
<td>3.0</td>
<td>–4.5</td>
<td>3.0</td>
<td>–2.9</td>
<td>–</td>
</tr>
<tr>
<td>Output Voltage</td>
<td></td>
<td>V&lt;sub&gt;IH&lt;/sub&gt;</td>
<td>–5.0</td>
<td>7.0</td>
<td>–7.0</td>
<td>5.5</td>
<td>–7.0</td>
</tr>
<tr>
<td>(V&lt;sub&gt;OH&lt;/sub&gt; = 9.0 Vdc) TTL–CMOS</td>
<td>–5.0</td>
<td>10</td>
<td>1.5</td>
<td>–2.0</td>
<td>1.5</td>
<td>–2.0</td>
<td>–</td>
</tr>
<tr>
<td>(V&lt;sub&gt;OH&lt;/sub&gt; = 9.0 Vdc) CMOS–CMOS</td>
<td>–5.0</td>
<td>10</td>
<td>3.6</td>
<td>–3.5</td>
<td>2.75</td>
<td>–3.5</td>
<td>–</td>
</tr>
<tr>
<td>(V&lt;sub&gt;OH&lt;/sub&gt; = 13.5 Vdc) CMOS–CMOS</td>
<td>–5.0</td>
<td>15</td>
<td>3.6</td>
<td>–3.5</td>
<td>2.75</td>
<td>–3.5</td>
<td>–</td>
</tr>
<tr>
<td>(V&lt;sub&gt;OH&lt;/sub&gt; = 13.5 Vdc) CMOS–CMOS</td>
<td>–5.0</td>
<td>15</td>
<td>7.1</td>
<td>–7.0</td>
<td>5.5</td>
<td>–7.0</td>
<td>–</td>
</tr>
<tr>
<td>Output Drive Current</td>
<td></td>
<td>I&lt;sub&gt;OH&lt;/sub&gt;</td>
<td>–5.0</td>
<td>3.0</td>
<td>–2.4</td>
<td>–4.2</td>
<td>–1.7</td>
</tr>
<tr>
<td>(V&lt;sub&gt;OH&lt;/sub&gt; = 2.5 Vdc) Source</td>
<td>–5.0</td>
<td>10</td>
<td>0.64</td>
<td>–0.51</td>
<td>–0.88</td>
<td>–0.36</td>
<td>–</td>
</tr>
<tr>
<td>(V&lt;sub&gt;OH&lt;/sub&gt; = 4.6 Vdc) Sink</td>
<td>–5.0</td>
<td>10</td>
<td>1.6</td>
<td>–1.3</td>
<td>2.25</td>
<td>–0.9</td>
<td>–</td>
</tr>
<tr>
<td>(V&lt;sub&gt;OH&lt;/sub&gt; = 1.6 Vdc) Sink</td>
<td>–5.0</td>
<td>15</td>
<td>4.2</td>
<td>–3.4</td>
<td>8.8</td>
<td>–2.4</td>
<td>–</td>
</tr>
<tr>
<td>Input Current</td>
<td></td>
<td>I&lt;sub&gt;in&lt;/sub&gt;</td>
<td>–15</td>
<td>±0.1</td>
<td>±0.00001</td>
<td>±0.1</td>
<td>±1.0</td>
</tr>
<tr>
<td>Input Capacitance (V&lt;sub&gt;in&lt;/sub&gt; = 0)</td>
<td>C&lt;sub&gt;in&lt;/sub&gt;</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>5.0</td>
<td>7.5</td>
<td>–</td>
</tr>
<tr>
<td>Quiescent Current (Per Package)</td>
<td>I&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>–5.0</td>
<td>0.05</td>
<td>–</td>
<td>0.0005</td>
<td>0.05</td>
<td>–</td>
</tr>
<tr>
<td>CMOS–CMOS Mode</td>
<td>I&lt;sub&gt;CC&lt;/sub&gt;</td>
<td>–10</td>
<td>0.10</td>
<td>–</td>
<td>0.0010</td>
<td>0.10</td>
<td>–</td>
</tr>
<tr>
<td>Quiescent Current (Per Package)</td>
<td>I&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>–5.0</td>
<td>0.5</td>
<td>–</td>
<td>0.0005</td>
<td>0.5</td>
<td>–</td>
</tr>
<tr>
<td>TTL–CMOS Mode</td>
<td>I&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>–5.0</td>
<td>1.0</td>
<td>–</td>
<td>0.0010</td>
<td>1.0</td>
<td>–</td>
</tr>
<tr>
<td>Quiescent Current (Per Package)</td>
<td>I&lt;sub&gt;CC&lt;/sub&gt;</td>
<td>–5.0</td>
<td>1.0</td>
<td>–</td>
<td>0.0015</td>
<td>2.0</td>
<td>–</td>
</tr>
<tr>
<td>TTL–CMOS Mode</td>
<td>I&lt;sub&gt;CC&lt;/sub&gt;</td>
<td>–5.0</td>
<td>5.0</td>
<td>–</td>
<td>2.5</td>
<td>5.0</td>
<td>–</td>
</tr>
</tbody>
</table>

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
### SWITCHING CHARACTERISTICS (C\textsubscript{L} = 50 pF, T\textsubscript{A} = 25°C)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Shifting Mode</th>
<th>V\textsubscript{CC} V\textsubscript{d}c</th>
<th>V\textsubscript{DD} V\textsubscript{d}c</th>
<th>Limits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Propagation Delay, High to Low</td>
<td>t\textsubscript{PHL}</td>
<td>TTL – CMOS V\textsubscript{DD} &gt; V\textsubscript{CC}</td>
<td>5.0 10</td>
<td>–</td>
<td>140 280</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CMOS – CMOS V\textsubscript{DD} &gt; V\textsubscript{CC}</td>
<td>5.0 10</td>
<td>–</td>
<td>120 240</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V\textsubscript{DD} &gt; V\textsubscript{CC}</td>
<td>10 15</td>
<td>–</td>
<td>70 140</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CMOS – CMOS V\textsubscript{CC} &gt; V\textsubscript{DD}</td>
<td>10 5.0</td>
<td>–</td>
<td>185 370</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V\textsubscript{CC} &gt; V\textsubscript{DD}</td>
<td>15 10</td>
<td>–</td>
<td>175 350</td>
</tr>
<tr>
<td>Propagation Delay, Low to High</td>
<td>t\textsubscript{PLH}</td>
<td>TTL – CMOS V\textsubscript{DD} &gt; V\textsubscript{CC}</td>
<td>5.0 10</td>
<td>–</td>
<td>170 340</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V\textsubscript{DD} &gt; V\textsubscript{CC}</td>
<td>5.0 15</td>
<td>–</td>
<td>160 320</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CMOS – CMOS V\textsubscript{DD} &gt; V\textsubscript{CC}</td>
<td>5.0 10</td>
<td>–</td>
<td>170 340</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V\textsubscript{DD} &gt; V\textsubscript{CC}</td>
<td>10 15</td>
<td>–</td>
<td>100 200</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CMOS – CMOS V\textsubscript{CC} &gt; V\textsubscript{DD}</td>
<td>10 5.0</td>
<td>–</td>
<td>275 550</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V\textsubscript{CC} &gt; V\textsubscript{DD}</td>
<td>15 10</td>
<td>–</td>
<td>145 290</td>
</tr>
<tr>
<td>Output Rise and Fall Time</td>
<td>t\textsubscript{TH}, t\textsubscript{TLH}</td>
<td>ALL</td>
<td>–</td>
<td>5.0 – 100 200</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>–</td>
<td>10 – 50 100</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>–</td>
<td>15 – 40 80</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

3. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

![Figure 1. Input Switchpoint CMOS to CMOS Mode](image1)

![Figure 2. Input Switchpoint TTL to CMOS Mode](image2)

![Figure 3. Operating Boundary CMOS to CMOS Mode](image3)

![Figure 4. Operating Boundary TTL to CMOS Mode](image4)
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. Emitter
4. NO CONNECTION
5. Emitter
6. BASE
7. COLLECTOR
8. Emitter
9. BASE
10. Emitter
11. NO CONNECTION
12. Emitter
13. BASE
14. COLLECTOR
15. Emitter
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. BASE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. CATHODE
10. CATHODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. CATHODE
15. CATHODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, #1
2. BASE, #1
3. Emitter, #1
4. COLLECTOR, #1
5. COLLECTOR, #1
6. BASE, #2
7. Emitter, #2
8. COLLECTOR, #2
9. COLLECTOR, #2
10. BASE, #3
11. Emitter, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. Emitter, #4
16. COLLECTOR, #4

STYLE 4:
PIN 1. COLLECTOR, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. Emitter, #4
11. Emitter, #4
12. Emitter, #3
13. BASE, #3
14. Emitter, #3
15. Emitter, #2
16. Emitter, #2

STYLE 5:
PIN 1. DRAIN, #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. ANODE
10. DRAIN, #4
11. ANODE
12. SOURCE, #4
13. SOURCE, #4
14. SOURCE, #3
15. SOURCE, #3
16. SOURCE, #2

STYLE 6:
PIN 1. CATHODE
2. NO CONNECTION
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. CATHODE
10. CATHODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. CATHODE
15. CATHODE
16. CATHODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. ANODE
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIMENSIONS: MILLIMETERS

- A: 1.27
- B: 0.49
- C: 0.25
- D: 0.35
- E: 0.15
- F: 0.10
- G: 0.10
- H: 0.25
- I: 0.10
- J: 0.05
- K: 0.10
- L: 0.25
- M: 0.50
- N: 0.05
- O: 0.18
- P: 0.10
- Q: 0.05
- R: 0.10

RECOMMENDED SOLDERING FOOTPRINT*

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER: 98ASB42566B
DESCRIPTION: SOIC-16
PAGE 1 OF 1
**TSSOP–16 WB**
CASE 948F
ISSUE B

**DATE 19 OCT 2006**

**NOTES:**
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
   INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION.
   ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS
   OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

<table>
<thead>
<tr>
<th>DIM</th>
<th>MIN</th>
<th>MAX</th>
<th>MIN</th>
<th>MAX</th>
</tr>
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**RECOMMENDED SOLDERING FOOTPRINT**

**GENERIC MARKING DIAGRAM**

*For additional information on our Pb–Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.*

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