MC14029B

Binary/Decade Up/Down Counter

The MC14029B Binary/Decade up/down counter is constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. The counter consists of type D flip−flop stages with a gating structure to provide toggle flip−flop capability. The counter can be used in either Binary or BCD operation. This complementary MOS counter finds primary use in up/down and difference counting and frequency synthesizer applications where low power dissipation and/or high noise immunity is desired. It is also useful in A/D and D/A conversion and for magnitude and sign generation.

Features

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Speed
- Logic Edge−Clocked Design − Count Occurs on Positive Going Edge of Clock
- Asynchronous Preset Enable Operation
- Capable of Driving Two Low−Power TTL Loads or One Low−Power Schottky TTL Load Over the Rated Temperature Range
- Pin for Pin Replacement for CD4029B
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This Device is Pb−Free and is RoHS Compliant

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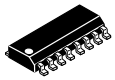
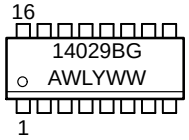


SOIC−16
D SUFFIX
CASE 751B

MARKING DIAGRAM



A	= Assembly Location
WL	= Wafer Lot
YY, Y	= Year
WW	= Work Week
G	= Pb−Free Indicator

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: “D/DW” Packages: –7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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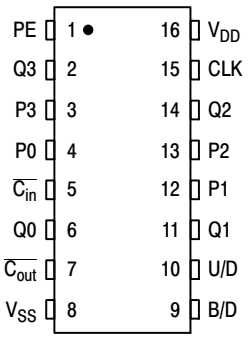
PIN ASSIGNMENT



TRUTH TABLE

$\overline{\text{Carry In}}$	Up/Down	Preset Enable	Action
1	X	0	No Count
0	1	0	Count Up
0	0	0	Count Down
X	X	1	Preset

X = Don’t Care

ORDERING INFORMATION

Device	Package	Shipping†
MC14029BDR2G	SOIC−16 (Pb−Free)	2500 Units / Tape & Reel
NLV14029BDR2G*	SOIC−16 (Pb−Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ (Note 2)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage	"0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0			10	–	0.05	–	0	0.05	–	0.05	
			15	–	0.05	–	0	0.05	–	0.05	
	"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}			10	9.95	–	9.95	10	–	9.95	–	
			15	14.95	–	14.95	15	–	14.95	–	
Input Voltage	"0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)			5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)			10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)			15	–	4.0	–	6.75	4.0	–	4.0	
	"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)			5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)			10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)			15	11	–	11	8.25	–	11	–	
Output Drive Current		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	
(V_{OH} = 4.6 Vdc)			5.0	–0.64	–	–0.51	–0.88	–	–0.36	–	
(V_{OH} = 9.5 Vdc)			10	–1.6	–	–1.3	–2.25	–	–0.9	–	
(V_{OH} = 13.5 Vdc)			15	–4.2	–	–3.4	–8.8	–	–2.4	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)			15	4.2	–	3.4	8.8	–	2.4	–	
Input Current		I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Capacitance, (V_{in} = 0)		C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current		I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)			10	–	10	–	0.010	10	–	300	
			15	–	20	–	0.015	20	–	600	
Total Supply Current (Notes 3 & 4)		I_T	5.0	I_T = (0.58 μA/kHz) f + I_{DD}							μAdc
(Dynamic plus Quiescent, Per Package)			10	I_T = (1.20 μA/kHz) f + I_{DD}							
(C_L = 50 pF on all outputs, all buffers switching)			15	I_T = (1.70 μA/kHz) f + I_{DD}							

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS (Note 5) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types			Unit
			Min	Typ (Note 6)	Max	
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clk to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	–	200	400	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	100	200	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	90	180	
Clk to $\overline{C_{out}}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	–	250	500	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	85	190	
$\overline{C_{in}}$ to $\overline{C_{out}}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 95 ns		5.0	–	175	360	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 47 ns		10	–	50	120	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns		15	–	50	100	
PE to Q	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	–	235	470	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	100	200	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	80	160	
PE to $\overline{C_{out}}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1. 7 ns/pF) C_L + 465 ns		5.0	–	320	640	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 192 ns		10	–	145	290	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns		15	–	105	210	
Clock Pulse Width	$t_{W(cl)}$	5.0	180	90	–	ns
		10	80	40	–	
		15	60	30	–	
Clock Pulse Frequency	f_{cl}	5.0	–	4.0	2.0	MHz
		10	–	8.0	4.0	
		15	–	10	5.0	
Preset Removal Time The Preset Signal must be low prior to a positive−going transition of the clock.	t_{rem}	5.0	160	80	–	ns
		10	80	40	–	
		15	60	30	–	
Clock Rise and Fall Time	$t_{r(cl)}$	5.0	–	–	15	μs
	$t_{f(cl)}$	10	–	–	5	
		1 5	–	–	4	
$\overline{Carry}$ In Setup Time	t_{su}	5.0	150	75	–	ns
		10	60	30	–	
		15	40	20	–	
Up/Down Setup Time		5.0	340	170	–	ns
		10	140	70	–	
		15	100	50	–	
Binary/Decade Setup Time		5.0	320	160	–	ns
		10	140	70	–	
		15	100	50	–	
Preset Enable Pulse Width	t_W	5.0	130	65	–	ns
		10	70	35	–	
		15	50	25	–	

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

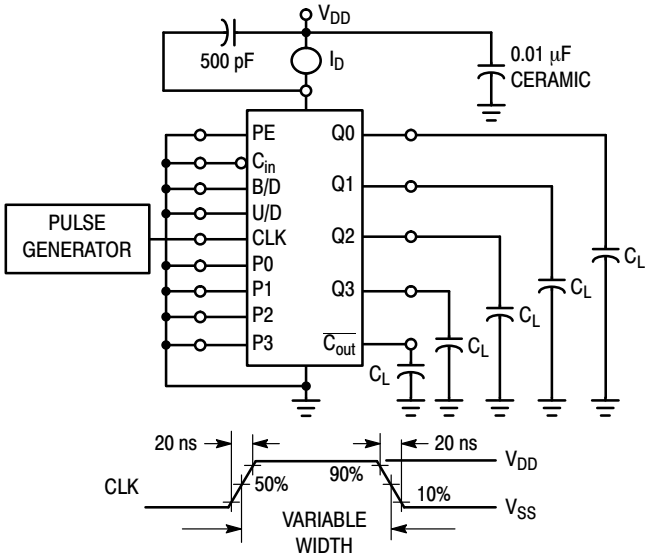


Figure 1. Power Dissipation Test Circuit and Waveform

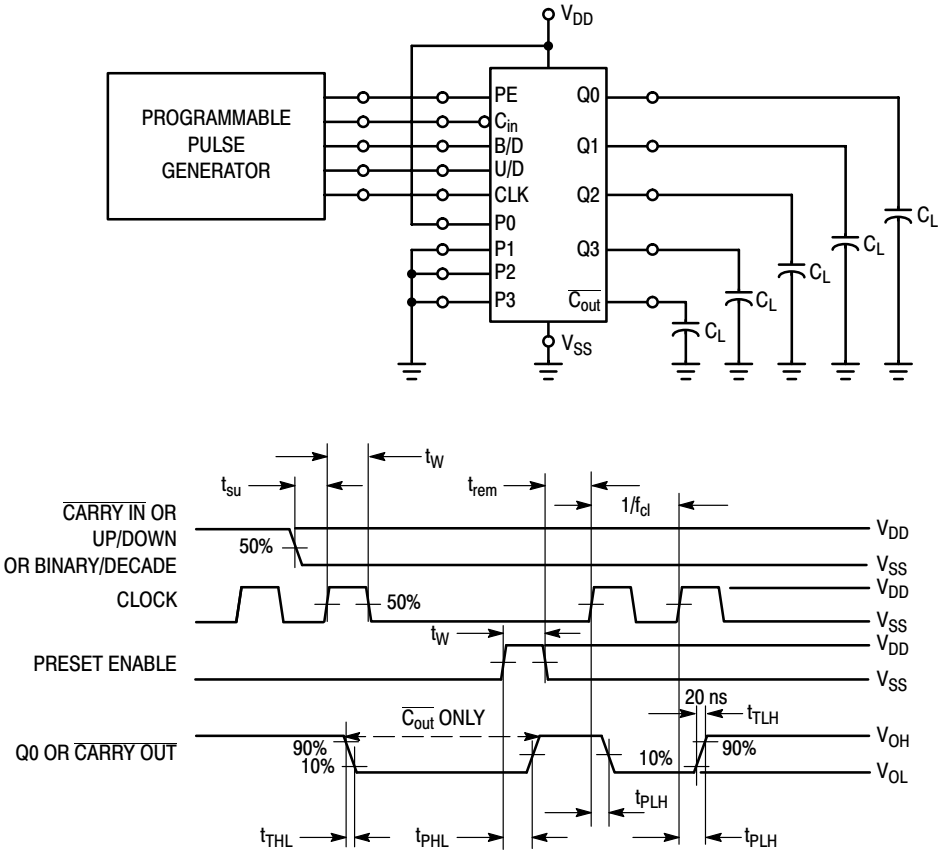
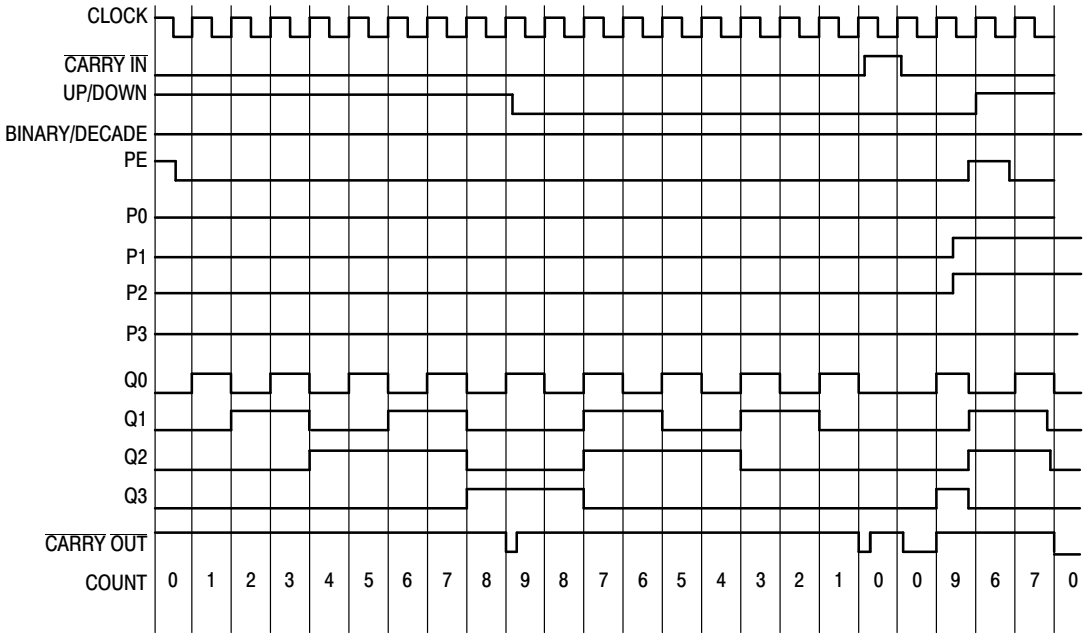
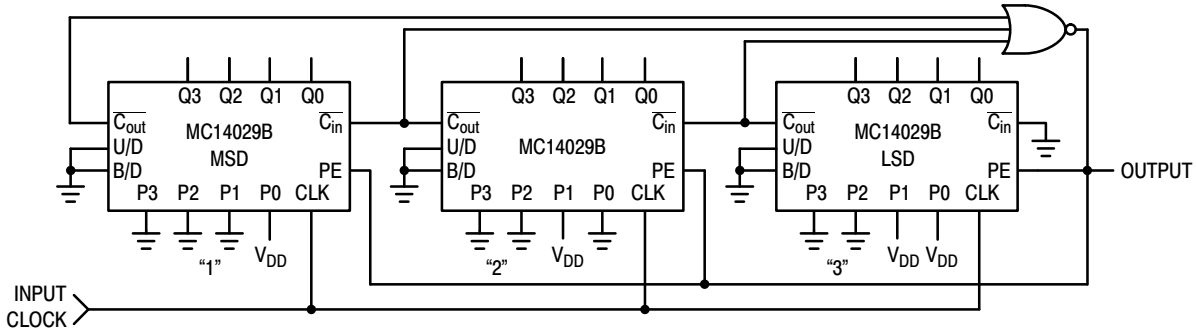
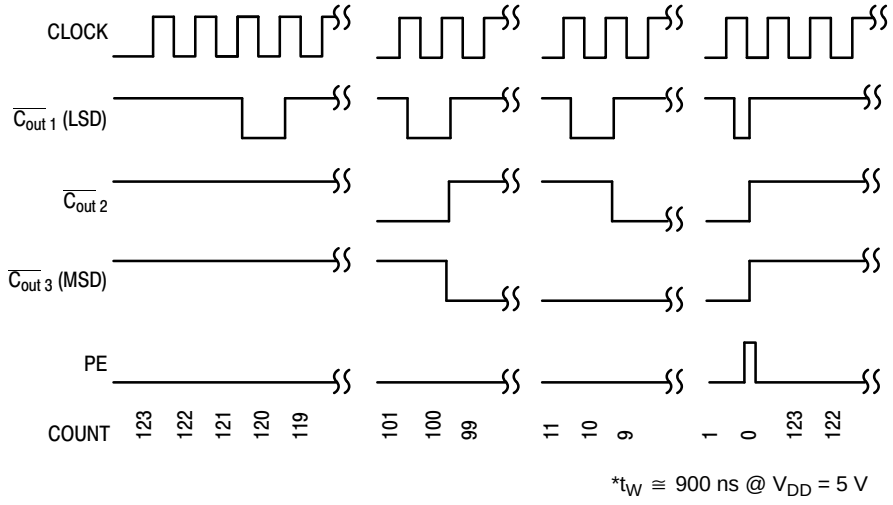


Figure 2. Switching Time Test Circuit and Waveforms

TIMING DIAGRAM



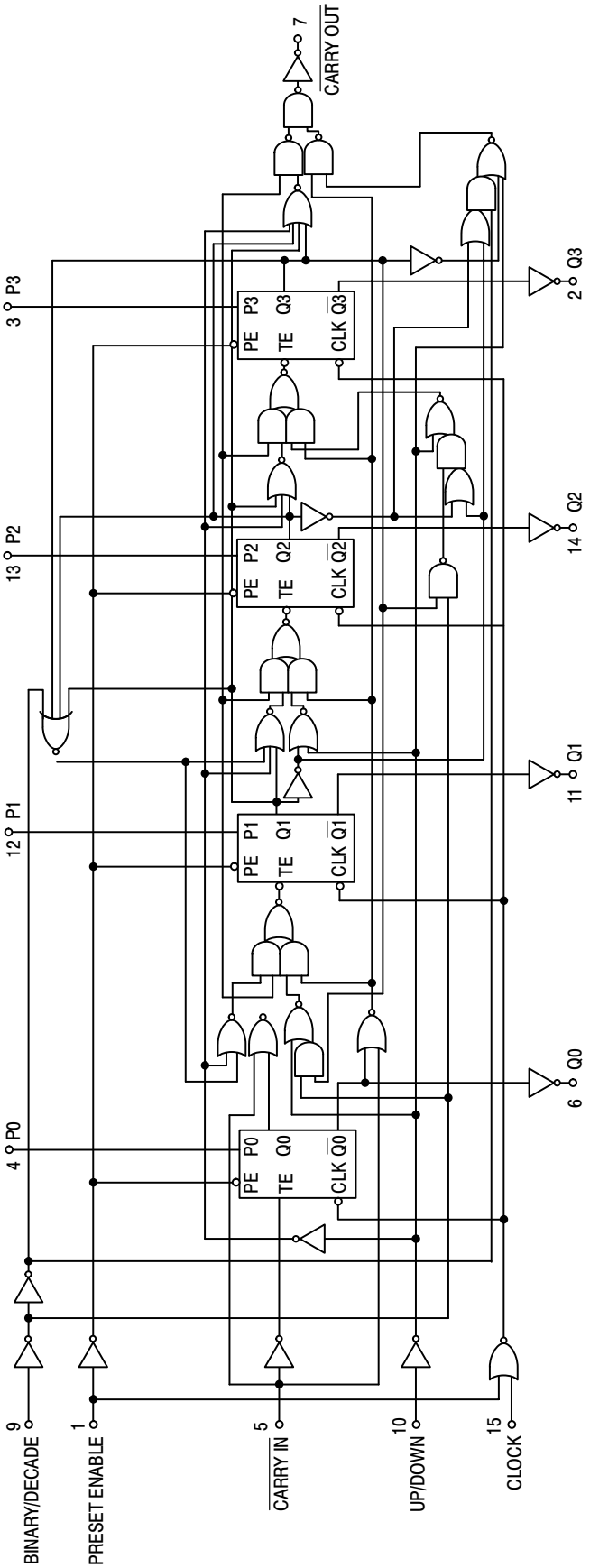


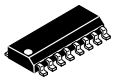


*t_W ≅ 900 ns @ V_{DD} = 5 V

Figure 3. Divide by N BCD Down Counter and Timing Diagram (Shown for N = 123)

LOGIC DIAGRAM





SCALE 1:1

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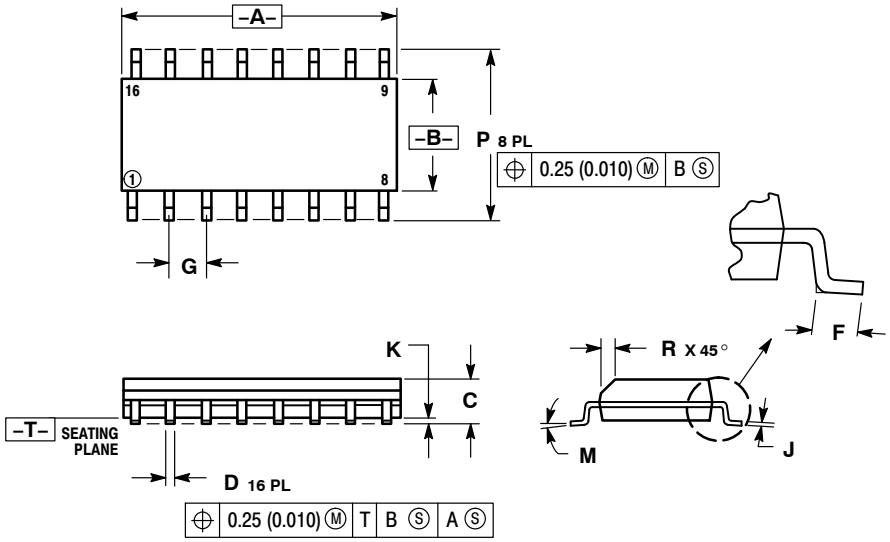
ISSUE K

DATE 29 DEC 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

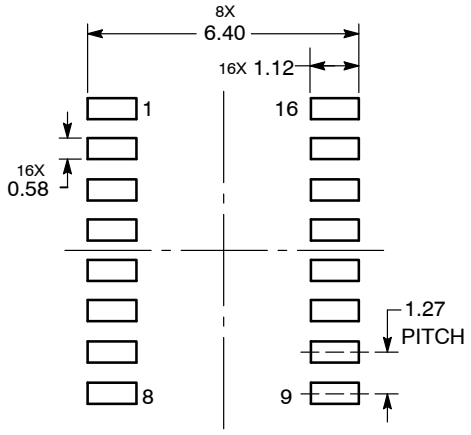
STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

SOLDERING FOOTPRINT



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