

# MC100LVEL13

## 3.3 V ECL Dual 1:3 Fanout Buffer

### Description

The MC100LVEL13 is a dual, fully differential 1:3 fanout buffer. The Low Output-Output Skew of the device makes it ideal for distributing two different frequency synchronous signals.

The differential inputs have special circuitry which ensures device stability under open input conditions. When both differential inputs are left open the D input will pull down to  $V_{EE}$ , The  $\bar{D}$  input will bias around  $V_{CC}/2$  and the Q output will go LOW.

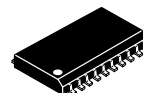
### Features

- 500 ps Typical Propagation Delays
- 50 ps Output-Output Skews
- ESD Protection: > 2 kV Human Body Model
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range:  $V_{CC} = 3.0\text{ V}$  to  $3.8\text{ V}$  with  $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range:  $V_{CC} = 0\text{ V}$  with  $V_{EE} = -3.0\text{ V}$  to  $-3.8\text{ V}$
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at  $V_{EE}$
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity: Level 3 (Pb-Free)
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 143 Devices
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



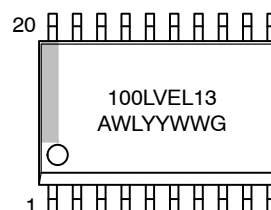
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SOIC-20 WB  
DW SUFFIX  
CASE 751D

### MARKING DIAGRAM\*



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

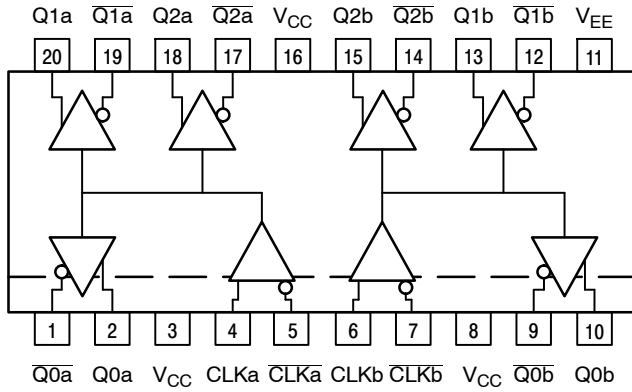
\*For additional marking information, refer to Application Note [AND8002/D](#).

### ORDERING INFORMATION

Device	Package	Shipping†
MC100LVEL13DWG	SOIC-20 WB (Pb-Free)	38 Units / Tube
MC100LVEL13DWR2G	SOIC-20 WB (Pb-Free)	1000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# MC100LVEL13



Warning: All  $V_{CC}$  and  $V_{EE}$  pins must be externally connected to Power Supply to guarantee proper operation.

**Figure 1. Logic Diagram and Pinout: 20-Lead SOIC**  
(Top View)

**Table 1. PIN DESCRIPTION**

PIN	FUNCTION
$Q_{na}, \overline{Q}_{na}$	ECL Differential Clock Outputs
$Q_{nb}, \overline{Q}_{nb}$	ECL Differential Clock Outputs
$CLK_n, \overline{CLK}_n$	ECL Differential Clock Inputs
$V_{CC}$	Positive Supply
$V_{EE}$	Negative Supply

**Table 2. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
$V_{CC}$	PECL Mode Power Supply	$V_{EE} = 0\text{ V}$		8 to 0	V
$V_{EE}$	NECL Mode Power Supply	$V_{CC} = 0\text{ V}$		-8 to 0	V
$V_I$	PECL Mode Input Voltage NECL Mode Input Voltage	$V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 -6 to 0	V V
$I_{out}$	Output Current	Continuous Surge		50 100	mA
$T_A$	Operating Temperature Range			-40 to +85	°C
$T_{stg}$	Storage Temperature Range			-65 to +150	°C
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-20 WB SOIC-20 WB	90 60	°C/W
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-20 WB	30 to 35	°C/W
$T_{sol}$	Wave Solder (Pb-Free)	< 2 to 3 sec @ 260°C		265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 3. LVPECL DC CHARACTERISTICS** ( $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		30	38		30	38		32	40	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
$V_{OL}$	Output LOW Voltage (Note 2)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	2135		2420	2135		2420	2135		2420	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	1490		1825	1490		1825	1490		1825	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 3) $V_{PP} < 500\text{ mV}$ $V_{PP} \geq 500\text{ mV}$										V
		1.3		2.9	1.2		2.9	1.2		2.9	
		1.5		2.9	1.4		2.9	1.4		2.9	
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current $\overline{\text{CLKn}}$ $\overline{\text{CLKn}}$										$\mu\text{A}$
		0.5			0.5			0.5			
		-300			-300			-300			

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
2. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{PPmin}$  and  $1\text{ V}$ .

**Table 4. LVNECL DC CHARACTERISTICS** ( $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -3.3\text{ V}$  (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		30	38		30	38		32	40	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
$V_{OL}$	Output LOW Voltage (Note 2)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	-1165		-880	-1165		-880	-1165		-880	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	-1810		-1475	-1810		-1475	-1810		-1475	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 3) $V_{PP} < 500\text{ mV}$ $V_{PP} \geq 500\text{ mV}$										V
		-2.0		-0.4	-2.1		-0.4	-2.1		-0.4	
		-1.8		-0.4	-1.9		-0.4	-1.9		-0.4	
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current $\overline{\text{CLKn}}$ $\overline{\text{CLKn}}$										$\mu\text{A}$
		0.5			0.5			0.5			
		-300			-300			-300			

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

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3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{PPmin}$  and  $1\text{ V}$ .

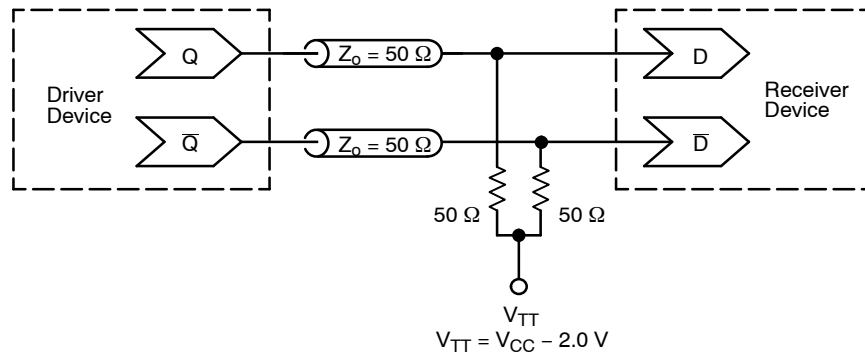
# MC100LVEL13

**Table 5. AC CHARACTERISTICS** ( $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  or  $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -3.3\text{ V}$  (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay CLK to Q/ $\bar{Q}$	410		600	430	500	620	450		640	ps
$t_{sk(O)}$	Output-Output Skew Any Qa to Qa, Any Qb to Qb Any Qa to Any Qb			50 75			50 75			50 75	ps
$t_{skew}$	Duty Cycle Skew $ t_{PLH} - t_{PHL} $			50			50			50	ps
$t_{JITTER}$	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
$V_{PP}$	Input Swing (Note 2)	150		1000	150		1000	150		1000	mV
$t_r$ $t_f$	Output Rise/Fall Times Q (20%–80%)	230		500	230		500	230		500	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
- $V_{PP}(\text{min})$  is minimum input swing for which AC parameters guaranteed. The device has a DC gain of  $\approx 40$ .



**Figure 2. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices)

### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-20 WB  
CASE 751D-05  
ISSUE H

DATE 22 APR 2015



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

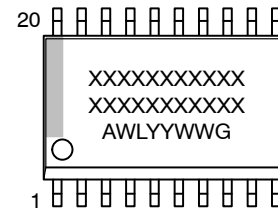
RECOMMENDED  
SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC  
MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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