

3.3 V ECL 2:8 Differential Fanout Buffer

MC100LVE310

Description

The MC100LVE310 is a low voltage, low skew 2:8 differential ECL fanout buffer designed with clock distribution in mind. The device features fully differential clock paths to minimize both device and system skew. The LVE310 offers two selectable clock inputs to allow for redundant or test clocks to be incorporated into the system clock trees.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50 Ω, even if only one side is being used. In most applications all eight differential pairs will be used and therefore terminated. In the case where fewer than eight pairs are used it is necessary to terminate at least the output pairs adjacent to the output pair being used in order to maintain minimum skew. Failure to follow this guideline will result in small degradations of propagation delay (on the order of 10–20 ps) of the outputs being used, while not catastrophic to most designs this will result in an increase in skew. Note that the package corners isolate outputs from one another such that the guideline expressed above holds only for outputs on the same side of the package.

The MC100LVE310, as with most ECL devices, can be operated from a positive V_{CC} supply in LVPECL mode. This allows the LVE310 to be used for high performance clock distribution in +3.3 V systems. Designers can take advantage of the LVE310's performance to distribute low skew clocks across the backplane or the board. In a PECL environment series or Thevenin line terminations are typically used as they require no additional power supplies, if parallel termination is desired a terminating voltage of $V_{CC} - 2.0$ V will need to be provided. For more information on using PECL, designers should refer to Application Note [AN1406/D](#).

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

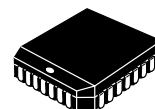
Features

- 200 ps Part-to-Part Skew
- 50 ps Output-to-Output Skew
- PECL Mode Operating Range:
 $V_{CC} = 3.0$ V to 3.8 V with $V_{EE} = 0$ V
- NECL Mode Operating Range:
 $V_{CC} = 0$ V with $V_{EE} = -3.0$ V to -3.8 V
- Q Output will Default LOW with All Inputs Open or at V_{EE}
- The 100 Series Contains Temperature Compensation
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



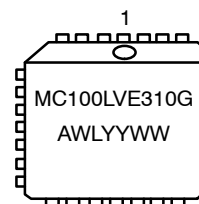
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PLCC-28
FN SUFFIX
CASE 776

MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

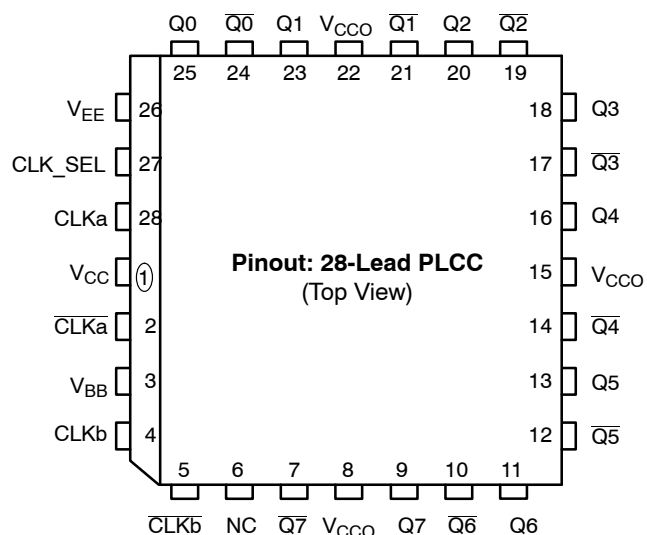
*For additional marking information, refer to Application Note [AND8002/D](#).

ORDERING INFORMATION

| Device | Package | Shipping† |
|------------------|-------------------|-----------------|
| MC100LVE310FNR2G | PLCC-28 (Pb-Free) | 500 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. Logic Diagram and Pinout Assignment

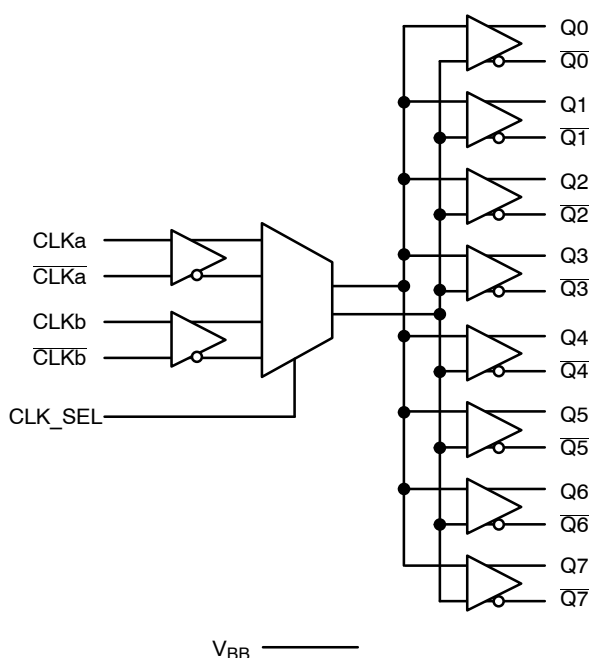


Figure 2. Logic Symbol

Table 1. PIN DESCRIPTION

| PIN | FUNCTION |
|-----------------------------------------------------------------|-------------------------------|
| CLKa, $\overline{\text{CLKa}}$, CLKb, $\overline{\text{CLKb}}$ | ECL Differential Input Clocks |
| Q0:7, $\overline{\text{Q0:7}}$ | ECL Differential Outputs |
| CLK_SEL | ECL Input Clock Select |
| V _{BB} | Reference Voltage Output |
| V _{CC} , V _{CCO} | Positive Supply |
| V _{EE} | Negative Supply |
| NC | No Connect |

Table 2. TRUTH TABLE

| CLK_SEL | Input Clock |
|---------|---------------|
| L | CLKa Selected |
| H | CLKb Selected |

Table 3. ATTRIBUTES

| Characteristics | Value |
|--------------------------------------------------------------------------|------------------------|
| Internal Input Pulldown Resistor | YES |
| Internal Input Pullup Resistor | N/A |
| ESD Protection Human Body Model Machine Model | > 2 kV > 200 V |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) PLCC-28 | Pb-Free Pkg Level 3 |
| Flammability Rating Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in |
| Transistor Count | 212 Devices |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | |

1. For additional information, see Application Note [AND8003/D](#).

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Table 4. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---------------|----------------------------------------------------|------------------------------------------------|----------------------------------------|--------------------|-----------------------------|
| V_{CC} | PECL Mode Power Supply | $V_{EE} = 0\text{ V}$ | | 8 to 0 | V |
| V_{EE} | NECL Mode Power Supply | $V_{CC} = 0\text{ V}$ | | -8 to 0 | V |
| V_I | PECL Mode Input Voltage NECL Mode Input Voltage | $V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$ | $V_I \leq V_{CC}$ $V_I \geq V_{EE}$ | 6 to 0 -6 to 0 | V |
| I_{out} | Output Current | Continuous Surge | | 50 100 | mA |
| I_{BB} | V_{BB} Sink/Source | | | ± 0.5 | mA |
| T_A | Operating Temperature Range | | | -40 to +85 | $^{\circ}\text{C}$ |
| T_{stg} | Storage Temperature Range | | | -65 to +150 | $^{\circ}\text{C}$ |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm 500 lfpm | PLCC-28 PLCC-28 | 63.5 43.5 | $^{\circ}\text{C}/\text{W}$ |
| θ_{JC} | Thermal Resistance (Junction-to-Case) | Standard Board | PLCC-28 | 22 to 26 $\pm 5\%$ | $^{\circ}\text{C}/\text{W}$ |
| T_{sol} | Wave Solder (Pb-Free) | | | 265 | $^{\circ}\text{C}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 5. LVPECL DC CHARACTERISTICS ($V_{CC} = 3.3\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 1))

| Symbol | Characteristic | -40 $^{\circ}\text{C}$ | | | 25 $^{\circ}\text{C}$ | | | 85 $^{\circ}\text{C}$ | | | Unit |
|-------------|----------------------------------------------------------------------------|------------------------|------|------|-----------------------|------|------|-----------------------|------|------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | 55 | 60 | | 55 | 60 | | 65 | 70 | mA |
| V_{OH} | Output HIGH Voltage (Note 2) | 2215 | 2295 | 2420 | 2275 | 2345 | 2420 | 2275 | 2345 | 2420 | mV |
| V_{OL} | Output LOW Voltage (Note 2) | 1470 | 1605 | 1745 | 1490 | 1595 | 1680 | 1490 | 1595 | 1680 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | 2135 | | 2420 | 2135 | | 2420 | 2135 | | 2420 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | 1490 | | 1825 | 1490 | | 1825 | 1490 | | 1825 | mV |
| V_{BB} | Output Voltage Reference | 1.92 | | 2.04 | 1.92 | | 2.04 | 1.92 | | 2.04 | V |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | 1.8 | | 2.9 | 1.8 | | 2.9 | 1.8 | | 2.9 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $\pm 0.3\text{ V}$.
2. Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2\text{ V}$.
3. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} . V_{IHCMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to $V_{PP}(\text{min})$.

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Table 6. LVNECL DC CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$, $V_{EE} = -3.3\text{ V}$ (Note 1))

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|----------------------------------------------------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | 55 | 60 | | 55 | 60 | | 65 | 70 | mA |
| V_{OH} | Output HIGH Voltage (Note 2) | -1085 | -1005 | -880 | -1025 | -955 | -880 | -1025 | -955 | -880 | mV |
| V_{OL} | Output LOW Voltage (Note 2) | -1830 | -1695 | -1555 | -1810 | -1705 | -1620 | -1810 | -1705 | -1620 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | -1165 | | -880 | -1165 | | -880 | -1165 | | -880 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | -1810 | | -1475 | -1810 | | -1475 | -1810 | | -1475 | mV |
| V_{BB} | Output Voltage Reference | -1.38 | | -1.26 | -1.38 | | -1.26 | -1.38 | | -1.26 | V |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | -1.5 | | -0.4 | -1.5 | | -0.4 | -1.5 | | -0.4 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $\pm 0.3\text{ V}$.
2. Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2\text{ V}$.
3. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} . V_{IHCMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to $V_{PP}(\text{min})$.

Table 7. AC CHARACTERISTICS ($V_{CC} = 3.3\text{ V}$; $V_{EE} = 0.0\text{ V}$ or $V_{CC} = 0.0\text{ V}$; $V_{EE} = -3.3\text{ V}$ (Note 1))

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|--------------------------------------|-------------------------------------------------------------------------------------------------------|------------|-----|------------|------------|-----|------------|------------|-----|------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f_{max} | Maximum Toggle Frequency @ $V_{\text{out}} > 500\text{ mV}_{\text{pp}}$ | 0.5 | 1.0 | | 0.5 | 1.0 | | 0.5 | 1.0 | | GHz |
| t_{PLH} t_{PHL} | Propagation Delay to Output IN (Differential Configuration) (Note 2) IN (Single-Ended) (Note 3) | 525 500 | | 725 750 | 550 550 | | 750 800 | 575 600 | | 775 850 | ps |
| t_{skew} | Within-Device Skew (Note 4) Part-to-Part Skew (Differential Configuration) | | | 75 250 | | | 50 200 | | | 50 200 | ps |
| t_{JITTER} | Additive CLOCK Jitter (RMS) < 0.5 GHz | | 1.5 | 2.0 | | 1.5 | 2.0 | | 1.5 | 2.0 | ps |
| V_{PP} | Input Swing (Note 5) | 500 | | 1000 | 500 | | 1000 | 500 | | 1000 | mV |
| t_r/t_f | Output Rise/Fall Time (20%–80%) | 200 | | 600 | 200 | | 600 | 200 | | 600 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

1. V_{EE} can vary $\pm 0.3\text{ V}$.
2. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
3. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
4. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
5. $V_{\text{PP}}(\text{min})$ is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The $V_{\text{PP}}(\text{min})$ is AC limited for the LVE310 as a differential input as low as 50 mV will still produce full ECL levels at the output.

MC100LVE310

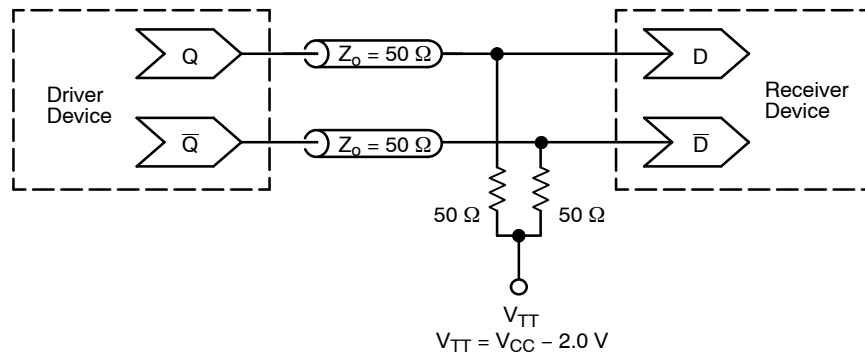


Figure 3. Typical Termination for Output Driver and Device Evaluation
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices)

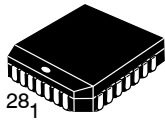
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

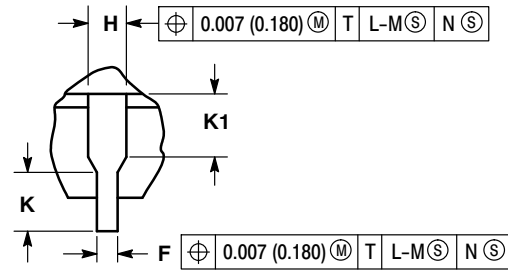
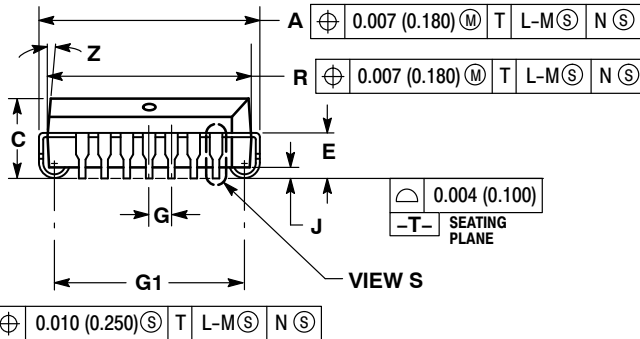
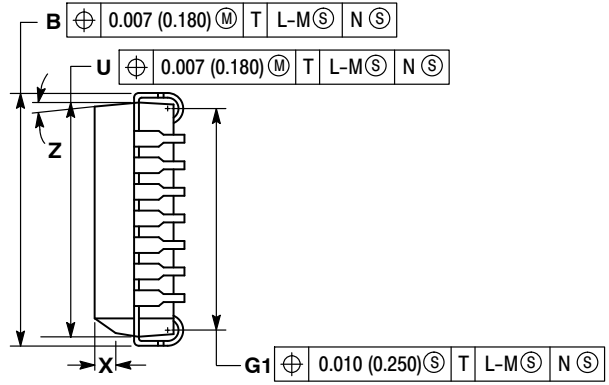
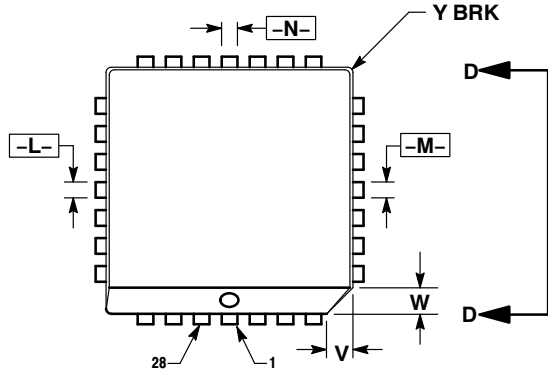
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SCALE 1:1

28 LEAD PLCC
CASE 776-02
ISSUE G

DATE 06 APR 2021

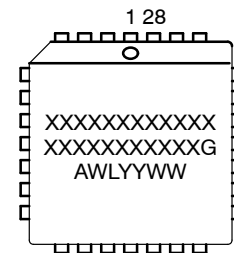


NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.485 | 0.495 | 12.32 | 12.57 |
| B | 0.485 | 0.495 | 12.32 | 12.57 |
| C | 0.165 | 0.180 | 4.20 | 4.57 |
| E | 0.090 | 0.110 | 2.29 | 2.79 |
| F | 0.013 | 0.021 | 0.33 | 0.53 |
| G | 0.050 BSC | | 1.27 BSC | |
| H | 0.026 | 0.032 | 0.66 | 0.81 |
| J | 0.020 | --- | 0.51 | --- |
| K | 0.025 | --- | 0.64 | --- |
| R | 0.450 | 0.456 | 11.43 | 11.58 |
| U | 0.450 | 0.456 | 11.43 | 11.58 |
| V | 0.042 | 0.048 | 1.07 | 1.21 |
| W | 0.042 | 0.048 | 1.07 | 1.21 |
| X | 0.042 | 0.056 | 1.07 | 1.42 |
| Y | --- | 0.020 | --- | 0.50 |
| Z | 2° 10° | | 2° 10° | |
| G1 | 0.410 | 0.430 | 10.42 | 10.92 |
| K1 | 0.040 | --- | 1.02 | --- |

GENERIC MARKING DIAGRAM*



- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

| | | |
|-------------------------|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
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