MAX1720

Switched Capacitor Voltage Inverter with Shutdown

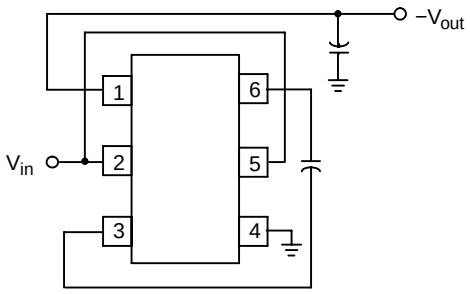
The MAX1720 is a CMOS charge pump voltage inverter that is designed for operation over an input voltage range of 1.15 V to 5.5 V with an output current capability in excess of 50 mA. The operating current consumption is only 67 μA, and a power saving shutdown input is provided to further reduce the current to a mere 0.4 μA. The device contains a 12 kHz oscillator that drives four low resistance MOSFET switches, yielding a low output resistance of 26 Ω and a voltage conversion efficiency of 99%. This device requires only two external 10 μF capacitors for a complete inverter making it an ideal solution for numerous battery powered and board level applications. The MAX1720 is available in the space saving TSOP−6 package.

Features

- Operating Voltage Range of 1.15 V to 5.5 V
- Output Current Capability in Excess of 50 mA
- Low Current Consumption of 67 μA
- Power Saving Shutdown Input for a Reduced Current of 0.4 μA
- Operation at 12 kHz
- Low Output Resistance of 26 Ω
- Space Saving TSOP−6 Package
- Pb−Free Package is Available

Typical Applications

- LCD Panel Bias
- Cellular Telephones
- Pagers
- Personal Digital Assistants
- Electronic Games
- Digital Cameras
- Camcorders
- Hand Held Instruments



This device contains 77 active transistors.

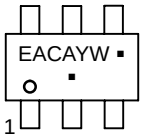
Figure 1. Typical Application

ON Semiconductor®

http://onsemi.com

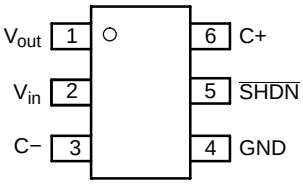
TSOP−6
SN SUFFIX
CASE 318G

MARKING DIAGRAM



EAC = Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
MAX1720EUT	TSOP−6	3000 Tape & Reel
MAX1720EUTG	TSOP−6 (Pb−Free)	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MAXIMUM RATINGS*

Rating	Symbol	Value	Unit
Input Voltage Range (V_{in} to GND)	V_{in}	−0.3 to 6.0	V
Output Voltage Range (V_{out} to GND)	V_{out}	−6.0 to 0.3	V
Output Current (Note 1)	I_{out}	100	mA
Output Short Circuit Duration (V_{out} to GND, Note 1)	t_{SC}	Indefinite	sec
Operating Junction Temperature	T_J	150	°C
Power Dissipation and Thermal Characteristics Thermal Resistance, Junction−to−Air Maximum Power Dissipation @ T_A = 70°C	 $R_{\theta JA}$ P_D	 256 313	 °C/W mW
Storage Temperature	T_{stg}	−55 to 150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

*ESD Ratings

ESD Machine Model Protection up to 200 V, Class B

ESD Human Body Model Protection up to 2000 V, Class 2

ELECTRICAL CHARACTERISTICS (V_{in} = 5.0 V, C_1 = 10 μF, C_2 = 10 μF, T_A = −40°C to 85°C, typical values shown are for T_A = 25°C unless otherwise noted. See Figure 14 for Test Setup.)

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Supply Voltage Range ($\overline{SHDN}$ = V_{in}, R_L = 10 k)	V_{in}	1.5 to 5.5	1.15 to 6.0	−	V
Supply Current Device Operating ($\overline{SHDN}$ = 5.0 V, R_L = ∞) T_A = 25°C T_A = 85°C	I_{in}	 − −	 67 72	 90 100	μA
Supply Current Device Shutdown ($\overline{SHDN}$ = 0 V) T_A = 25°C T_A = 85°C	I_{SHDN}	 − −	 0.4 1.6	 − −	μA
Oscillator Frequency T_A = 25°C T_A = −40°C to 85°C	f_{OSC}	 8.4 6.0	 12 −	 15.6 21	kHz
Output Resistance (I_{out} = 25 mA, Note 2)	R_{out}	−	26	50	Ω
Voltage Conversion Efficiency (R_L = ∞)	V_{EFF}	99	99.9	−	%
Power Conversion Efficiency (R_L = 1.0 k)	P_{EFF}	−	96	−	%
Shutdown Input Threshold Voltage (V_{in} = 1.5 V to 5.5 V) High State, Device Operating Low State, Device Shutdown	$V_{th(\overline{SHDN})}$	 − −	 0.6 V_{in} 0.5 V_{in}	 − −	V
Shutdown Input Bias Current High State, Device Operating, $\overline{SHDN}$ = 5.0 V T_A = 2 T_A = 85°C5°C Low State, Device Shutdown, $\overline{SHDN}$ = 0 V T_A = 25°C T_A = 85°C	 I_{IH} I_{IL} 	 − − − −	 5.0 100 5.0 100	 − − − −	pA
Wake−Up Time from Shutdown (R_L = 1.0 k)	t_{WKUP}	−	1.2	−	ms

1. Maximum Package power dissipation limits must be observed to ensure that the maximum junction temperature is not exceeded.
   $T_J = T_A + (P_D R_{\theta JA})$
2. Capacitors C_1 and C_2 contribution is approximately 20% of the total output resistance.

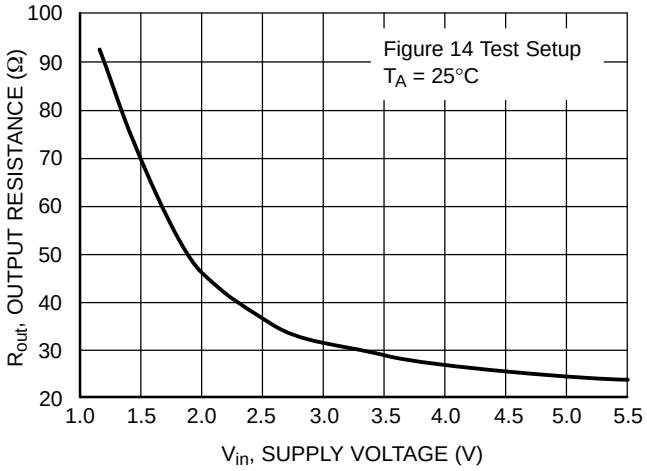


Figure 2. Output Resistance vs. Supply Voltage

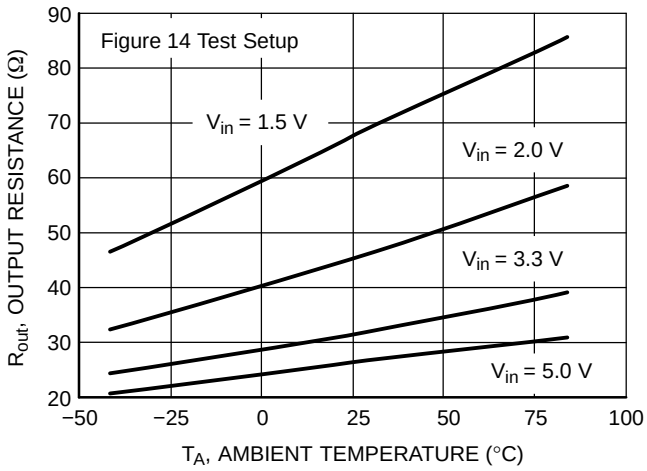


Figure 3. Output Resistance vs. Ambient Temperature

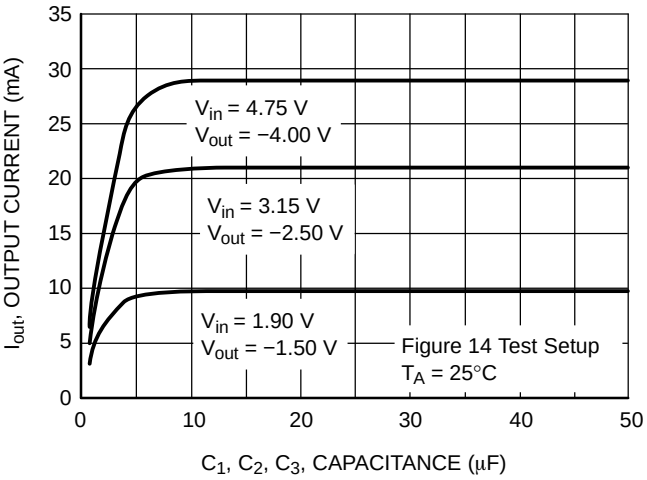


Figure 4. Output Current vs. Capacitance

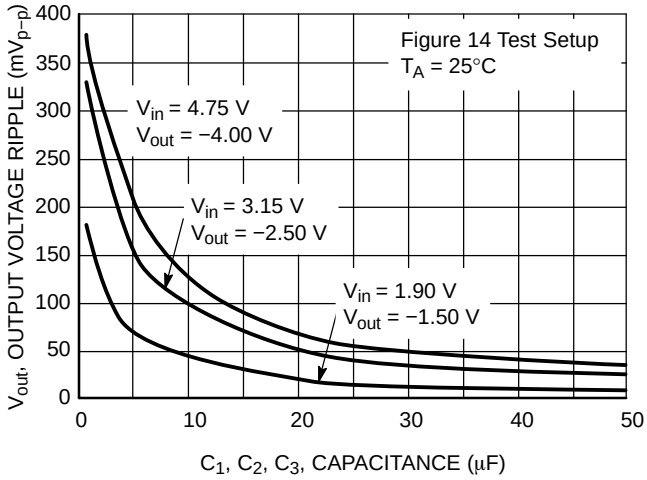


Figure 5. Output Voltage Ripple vs. Capacitance

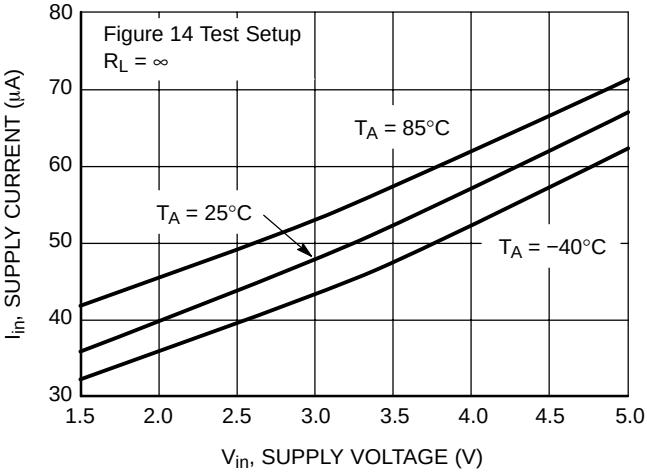


Figure 6. Supply Current vs. Supply Voltage

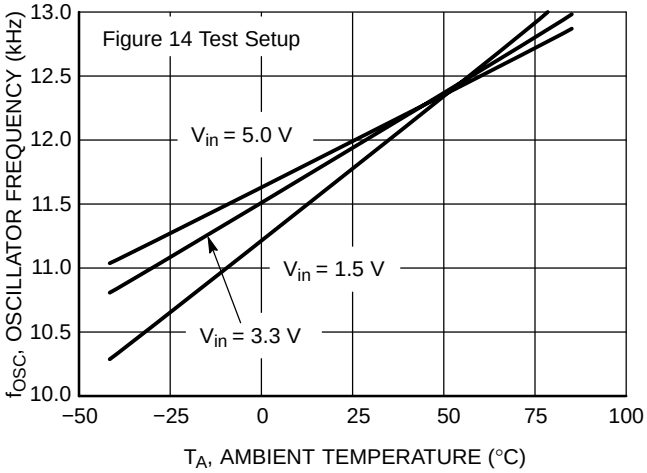


Figure 7. Oscillator Frequency vs. Ambient Temperature

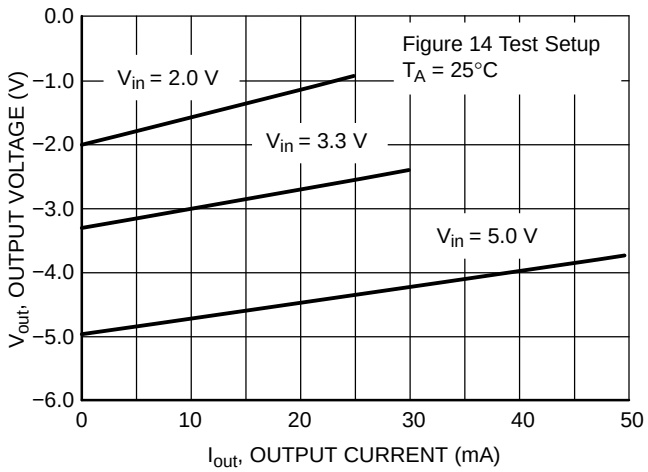


Figure 8. Output Voltage vs. Output Current

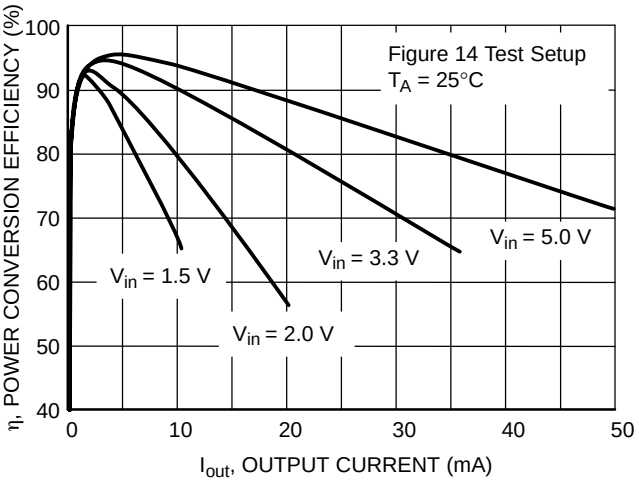


Figure 9. Power Conversion Efficiency vs. Output Current

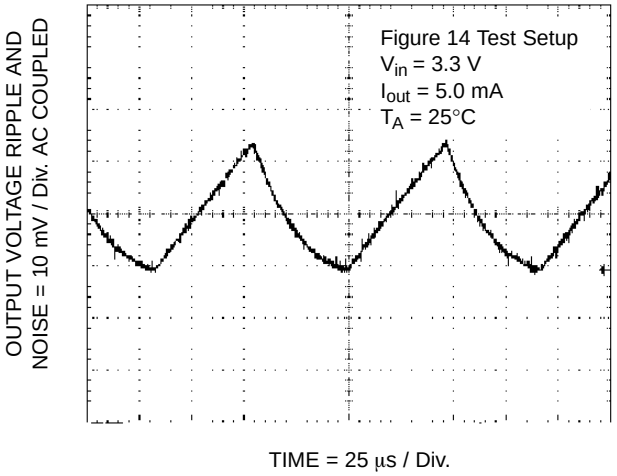


Figure 10. Output Voltage Ripple and Noise

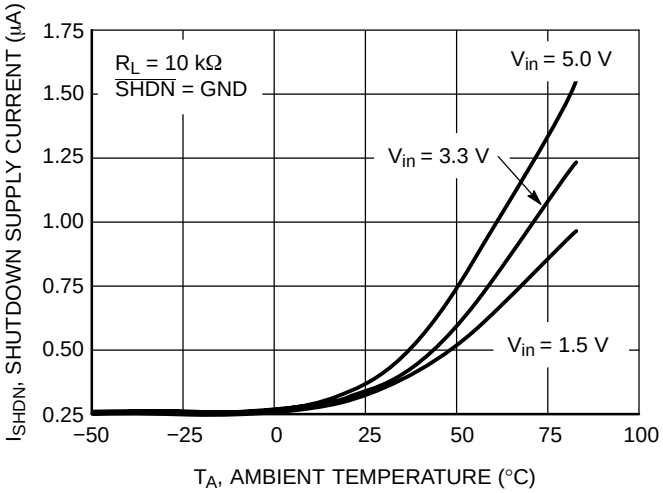


Figure 11. Shutdown Supply Current vs. Ambient Temperature

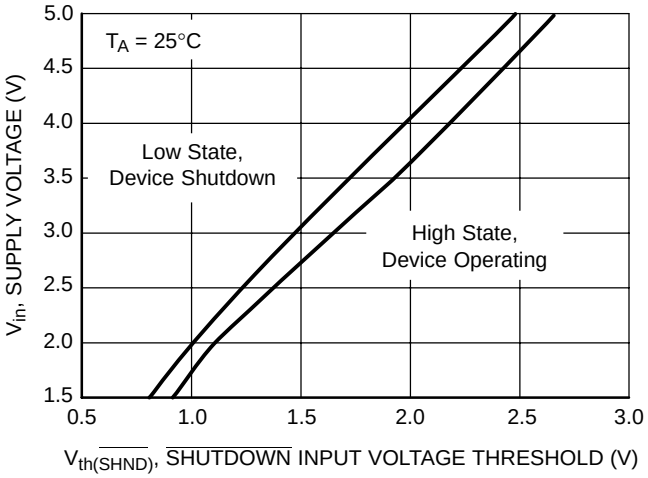


Figure 12. Supply Voltage vs. $\overline{\text{Shutdown}}$ Input Voltage Threshold

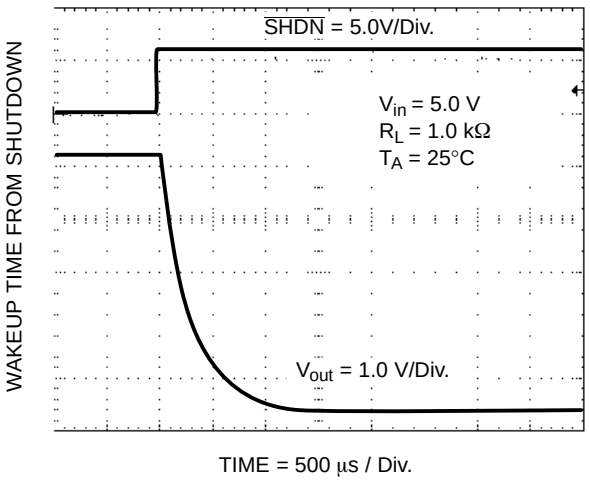


Figure 13. Wakeup Time From Shutdown

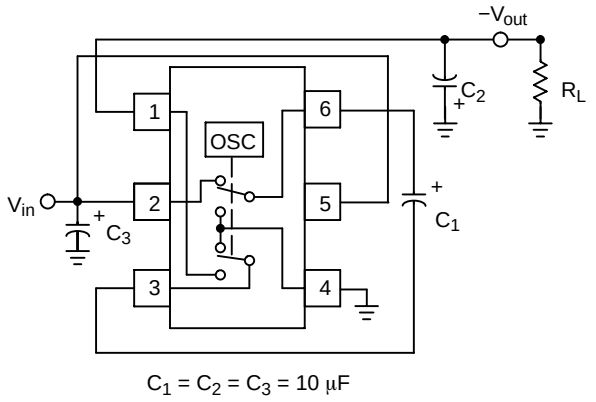


Figure 14. Test Setup/Voltage Inverter

DETAILED OPERATING DESCRIPTION

The MAX1720 charge pump converter inverts the voltage applied to the V_{in} pin. Conversion consists of a two−phase operation (Figure 15). During the first phase, switches S_2 and S_4 are open and S_1 and S_3 are closed. During this time, C_1 charges to the voltage on V_{in} and load current is supplied from C_2. During the second phase, S_2 and S_4 are closed, and S_1 and S_3 are open. This action connects C_1 across C_2, restoring charge to C_2.

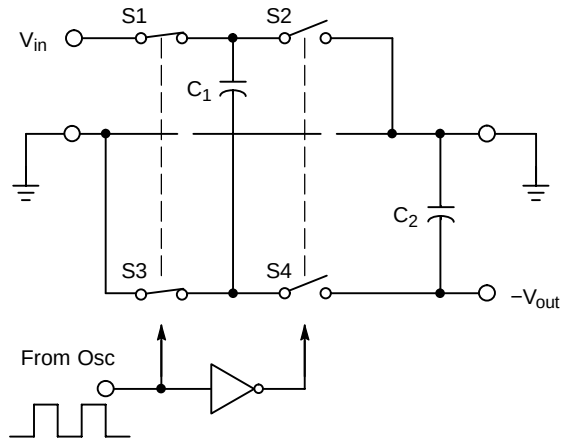


Figure 15. Ideal Switched Capacitor Charge Pump

APPLICATIONS INFORMATION

Output Voltage Considerations

The MAX1720 performs voltage conversion but does not provide regulation. The output voltage will drop in a linear manner with respect to load current. The value of this equivalent output resistance is approximately 26 Ω nominal at 25°C with V_{in} = 5.0 V. V_{out} is approximately −5.0 V at light loads, and drops according to the equation below:

$$V_{DROP} = I_{out} \times R_{out}$$

$$V_{out} = -(V_{in} - V_{DROP})$$

Charge Pump Efficiency

The overall power conversion efficiency of the charge pump is affected by four factors:

1. Losses from power consumed by the internal oscillator, switch drive, etc. (which vary with input voltage, temperature and oscillator frequency).
2. I^2R losses due to the on−resistance of the MOSFET switches on−board the charge pump.
3. Charge pump capacitor losses due to Equivalent Series Resistance (ESR).
4. Losses that occur during charge transfer from the commutation capacitor to the output capacitor when a voltage difference between the two capacitors exists.

Most of the conversion losses are due to factors 2, 3 and 4. These losses are given by Equation 1.

$$P_{LOSS(2,3,4)} = I_{out}^2 \times R_{out} \cong I_{out}^2 \times \left[\frac{1}{(f_{OSC})C_1} + 8R_{SWITCH} + 4ESR_{C_1} + ESR_{C_2}\right] \quad \text{(eq. 1)}$$

The $1/(f_{OSC})(C_1)$ term in Equation 1 is the effective output resistance of an ideal switched capacitor circuit (Figures 16 and 17).

The losses due to charge transfer above are also shown in Equation 2. The output voltage ripple is given by Equation 3.

$$P_{LOSS} = [0.5C_1(V_{in}^2 - V_{out}^2) + 0.5C_2(V_{RIPPLE}^2 - 2V_{out}V_{RIPPLE})] \times f_{OSC} \quad \text{(eq. 2)}$$

$$V_{RIPPLE} = \frac{I_{out}}{(f_{OSC})(C_2)} + 2(I_{out})(ESR_{C_2}) \quad \text{(eq. 3)}$$

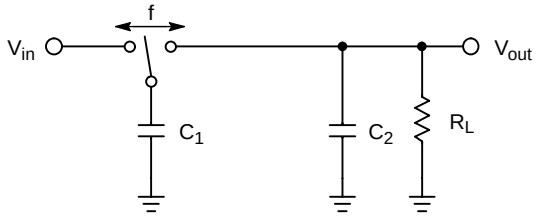


Figure 16. Ideal Switched Capacitor Model

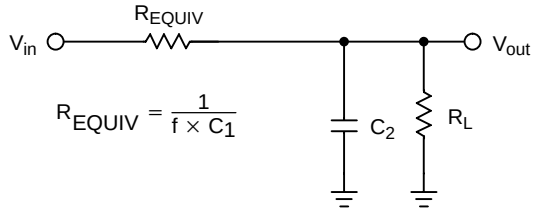


Figure 17. Equivalent Output Resistance

Capacitor Selection

In order to maintain the lowest output resistance and output ripple voltage, it is recommended that low ESR capacitors be used. Additionally, larger values of C_1 will lower the output resistance and larger values of C_2 will reduce output voltage ripple. (See Equation 3).

Table 1 shows various values of C_1, C_2 and C_3 with the corresponding output resistance values at 25°C. Table 2 shows the output voltage ripple for various values of C_1, C_2 and C_3. The data in Tables 1 and 2 was measured not calculated.

Table 1. Output Resistance vs. Capacitance ($C_1 = C_2 = C_3$), V_{in} = 4.75 V and V_{out} = −4.0 V

$C_1 = C_2 = C_3$ (μF)	R_{out} (Ω)
0.7	129.1
1.4	69.5
3.3	37.0
7.3	26.5
10	25.9
24	24.1
50	24

Table 2. Output Voltage Ripple vs. Capacitance ($C_1 = C_2 = C_3$), V_{in} = 4.75 V and V_{out} = −4.0 V

$C_1 = C_2 = C_3$ (μF)	Output Voltage Ripple (mV)
0.7	382
1.4	342
3.3	255
7.3	164
10	132
24	59
50	38

Input Supply Bypassing

The input voltage, V_{in} should be capacitively bypassed to reduce AC impedance and minimize noise effects due to the switching internals in the device. If the device is loaded from V_{out} to GND, it is recommended that a large value capacitor (at least equal to C_1) be connected from V_{in} to GND. If the device is loaded from V_{in} to V_{out}, a small (0.7 μF) capacitor between the pins is sufficient.

Voltage Inverter

The most common application for a charge pump is the voltage inverter (Figure 14). This application uses two or three external capacitors. The C_1 (pump capacitor) and C_2 (output capacitor) are required. The input bypass capacitor, C_3, may be necessary depending on the application. The output is equal to $-V_{in}$ plus any voltage drops due to loading. Refer to Tables 1 and 2 for capacitor selection. The test setup used for the majority of the characterization is shown in Figure 14.

Layout Considerations

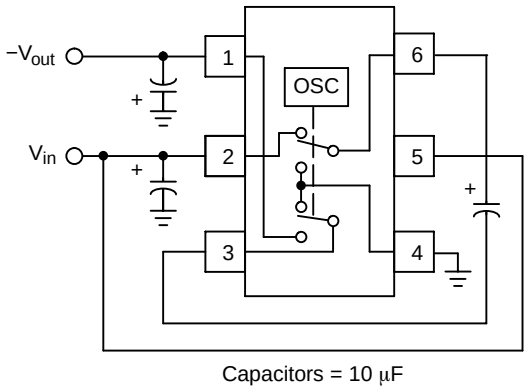
As with any switching power supply circuit, good layout practice is recommended. Mount components as close together as possible to minimize stray inductance and capacitance. Also, use a large ground plane to minimize noise leakage into other circuitry.

Capacitor Resources

Selecting the proper type of capacitor can reduce switching loss. Low ESR capacitors are recommended. The MAX1720 was characterized using the capacitors listed in Table 3. This list identifies low ESR capacitors for the voltage inverter application.

Table 3. Capacitor Types

Manufacturer/Contact	Part Types/Series
AVX 843−448−9411 www.avxcorp.com	TPS
Cornell Dubilier 508−996−8561 www.cornell−dubilier.com	ESRD
Sanyo/Os−con 619−661−6835 www.sanyovideo.com/oscon.htm	SN SVP
Vishay 603−224−1961 www.vishay.com	593D 594



Capacitors = 10 μF

Figure 18. Voltage Inverter

The MAX1720 primary function is a voltage inverter. The device will convert 5.0 V into −5.0 V with light loads. Two capacitors are required for the inverter to function. A third capacitor, the input bypass capacitor, may be required depending on the power source for the inverter. The performance for this device is illustrated below.

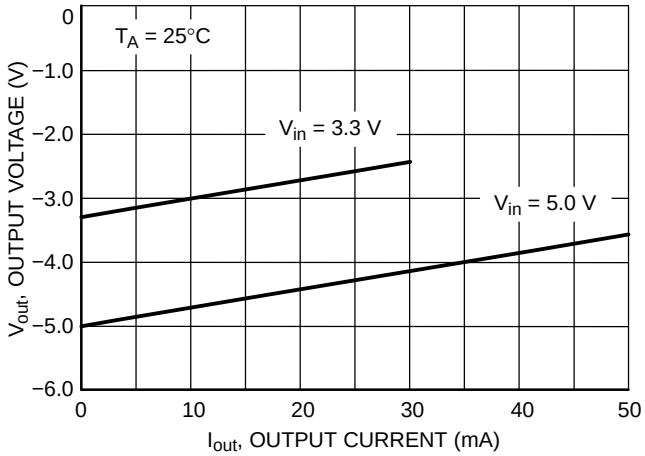


Figure 19. Inverter Load Regulation, Output Voltage vs. Output Current

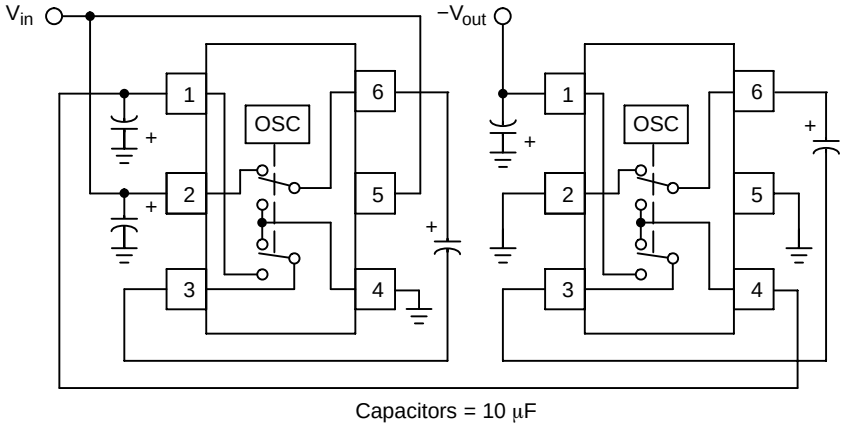
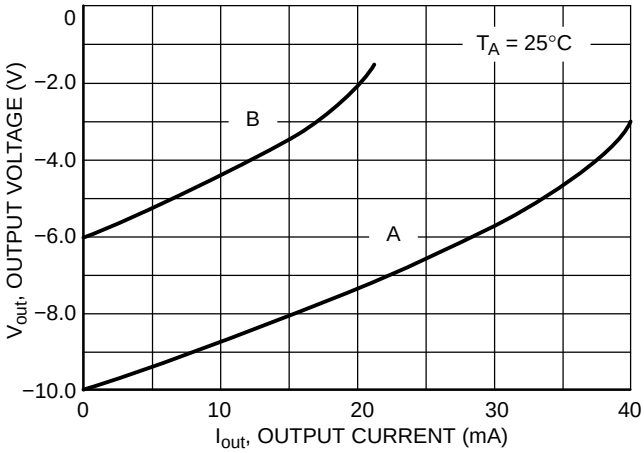


Figure 20. Cascaded Devices for Increased Negative Output Voltage

Two or more devices can be cascaded for increased output voltage. Under light load conditions, the output voltage is approximately equal to $-V_{in}$ times the number of stages. The converter output resistance increases dramatically with each additional stage. This is due to a reduction of input voltage to each successive stage as the converter output is loaded. Note that the ground connection for each successive stage must connect to the negative output of the previous stage. The performance characteristics for a converter consisting of two cascaded devices are shown below.



Curve	V_{in} (V)	R_{out} (Ω)
A	5.0	140
B	3.0	174

Figure 21. Cascade Load Regulation, Output Voltage vs. Output Current

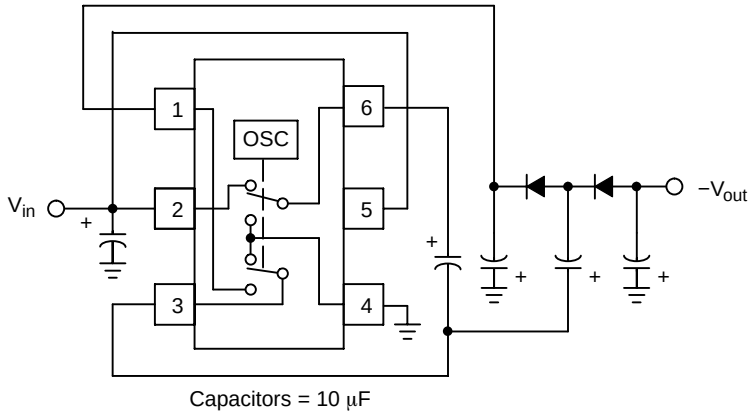
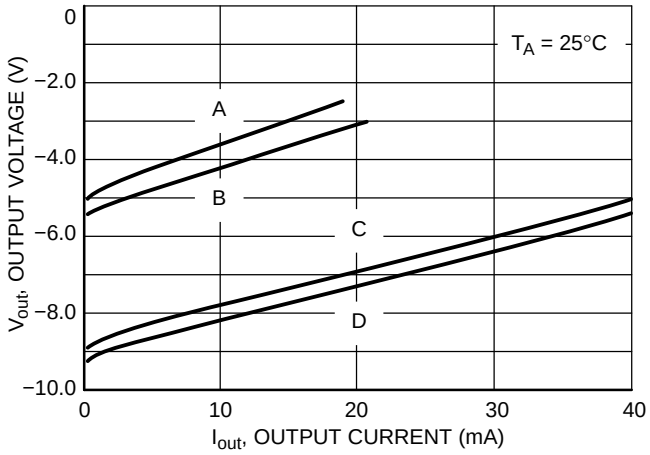


Figure 22. Negative Output Voltage Doubler

A single device can be used to construct a negative voltage doubler. The output voltage is approximately equal to $-2V_{in}$ minus the forward voltage drop of each external diode. The performance characteristics for the above converter are shown below. Note that curves A and C show the circuit performance with economical 1N4148 diodes, while curves B and D are with lower loss MBRA120E Schottky diodes.



Curve	V_{in} (V)	All Diodes	R_{out} (Ω)
A	3.0	1N4148	124
B	3.0	MBRA120E	115
C	5.0	1N4148	96
D	5.0	MBRA120E	94

Figure 23. Doubler Load Regulation, Output Voltage vs. Output Current

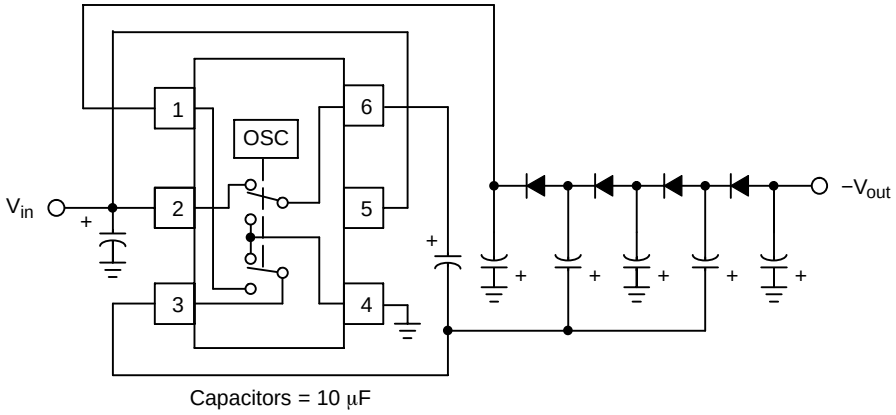
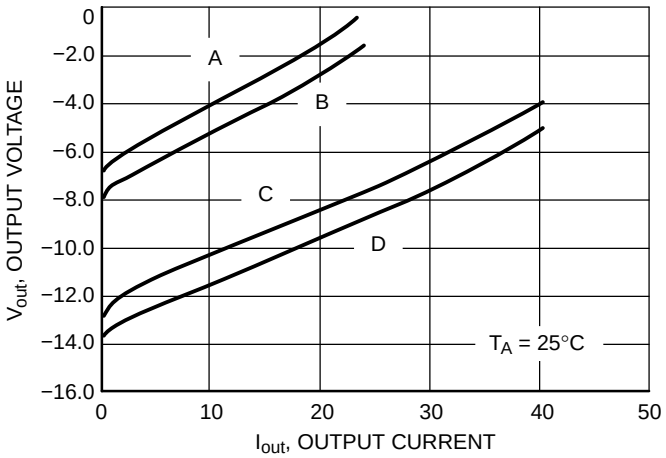


Figure 24. Negative Output Voltage Tripler

A single device can be used to construct a negative voltage tripler. The output voltage is approximately equal to $-3V_{in}$ minus the forward voltage drop of each external diode. The performance characteristics for the above converter are shown below. Note that curves A and C show the circuit performance with economical 1N4148 diodes, while curves B and D are with lower loss MBRA120E Schottky diodes.



Curve	V_{in} (V)	All Diodes	R_{out} (Ω)
A	3.0	1N4148	267
B	3.0	MBRA120E	250
C	5.0	1N4148	205
D	5.0	MBRA120E	195

Figure 25. Tripler Load Regulation, Output Voltage vs. Output Current

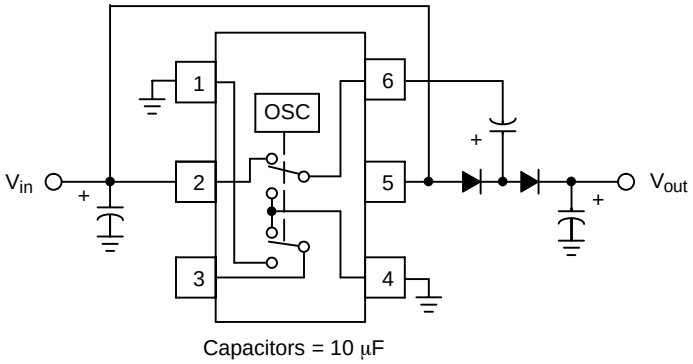
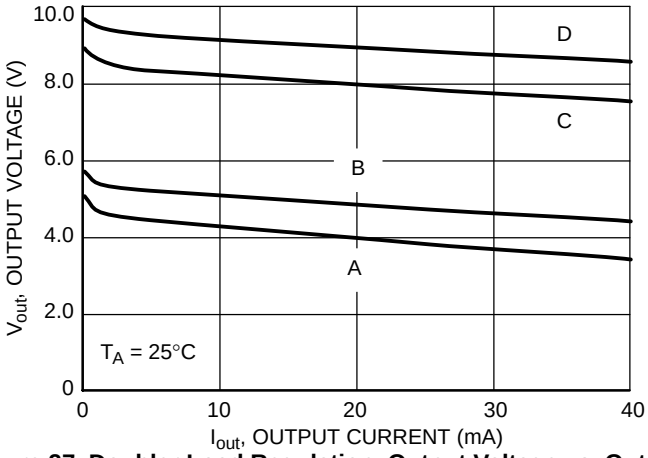


Figure 26. Positive Output Voltage Doubler

A single device can be used to construct a positive voltage doubler. The output voltage is approximately equal to $2V_{in}$ minus the forward voltage drop of each external diode. The performance characteristics for the above converter are shown below. Note that curves A and C show the circuit performance with economical 1N4148 diodes, while curves B and D are with lower loss MBRA120E Schottky diodes.



Curve	V_{in} (V)	All Diodes	R_{out} (Ω)
A	3.0	1N4148	32
B	3.0	MBRA120E	26
C	5.0	1N4148	26
D	5.0	MBRA120E	21

Figure 27. Doubler Load Regulation, Output Voltage vs. Output Current

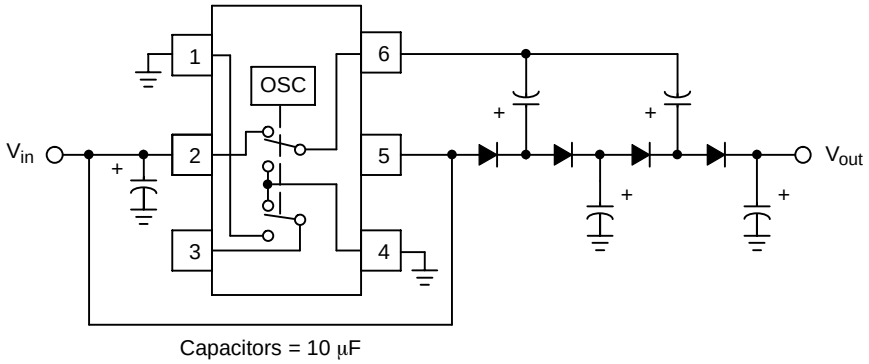
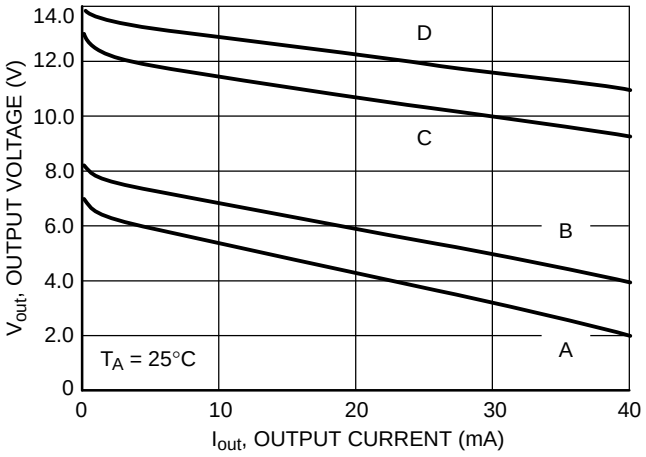


Figure 28. Positive Output Voltage Tripler

A single device can be used to construct a positive voltage tripler. The output voltage is approximately equal to $3V_{in}$ minus the forward voltage drop of each external diode. The performance characteristics for the above converter are shown below. Note that curves A and C show the circuit performance with economical 1N4148 diodes, while curves B and D are with lower loss MBRA120E Schottky diodes.



Curve	V_{in} (V)	All Diodes	R_{out} (Ω)
A	3.0	1N4148	111
B	3.0	MBRA120E	97
C	5.0	1N4148	85
D	5.0	MBRA120E	75

Figure 29. Tripler Load Regulation, Output Voltage vs. Output Current

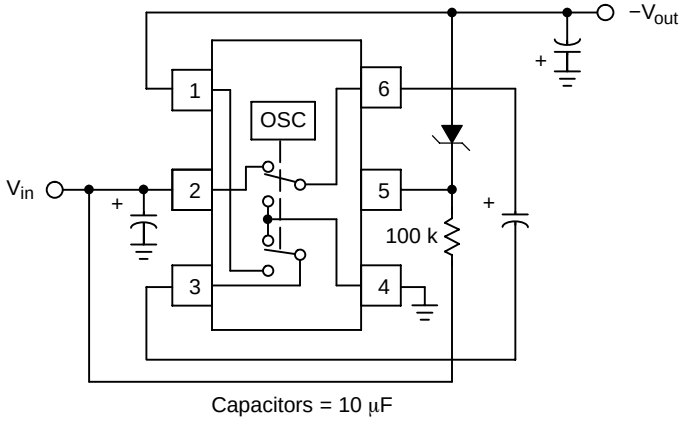


Figure 30. Load Regulated Negative Output Voltage

A zener diode can be used with the shutdown input to provide closed loop regulation performance. This significantly reduces the converter's output resistance and dramatically enhances the load regulation. For closed loop operation, the desired regulated output voltage must be lower in magnitude than $-V_{in}$. The output will regulate at a level of $-V_Z + V_{th(\overline{SHDN})}$. Note that the shutdown input voltage threshold is typically 0.5 V_{in} and therefore, the regulated output voltage will change proportional to the converter's input. This characteristic will not present a problem when used in applications with constant input voltage. In this case the zener breakdown was measured at 25 μA. The performance characteristics for the above converter are shown below. Note that the dashed curve sections represent the converter's open loop performance.

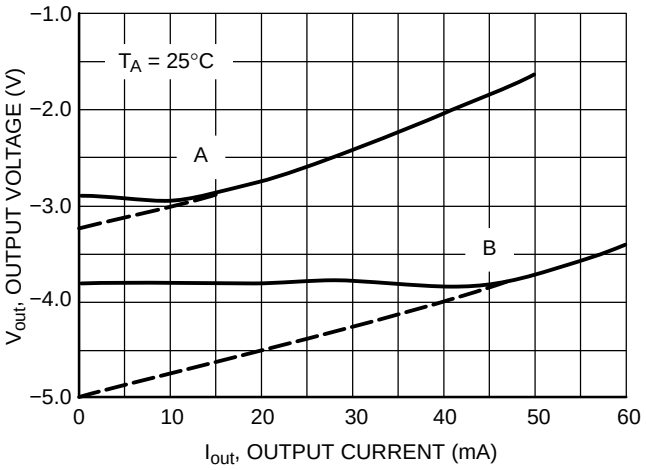


Figure 31. Load Regulation, Output Voltage vs. Output Current

Curve	V_{in} (V)	V_z (V)	V_{out} (V)
A	3.3 V	4.5	−2.8
B	5.0 V	6.5	−3.8

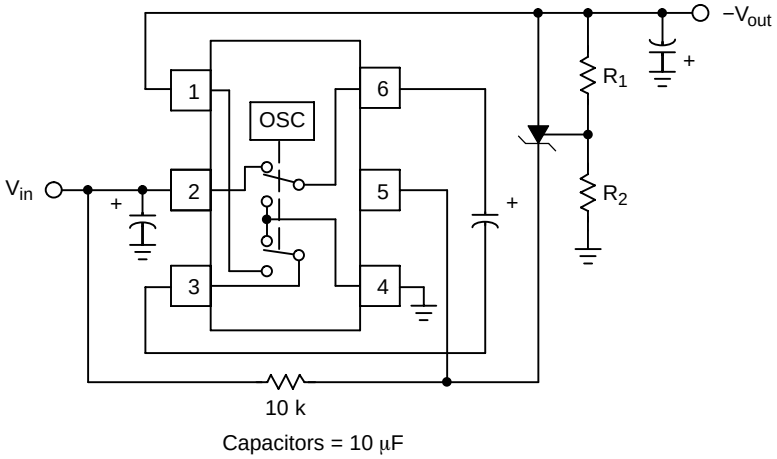


Figure 32. Line and Load Regulated Negative Output Voltage

An adjustable shunt regulator can be used with the shutdown input to give excellent closed loop regulation performance. The shunt regulator acts as a comparator with a precise input offset voltage which significantly reduces the converter's output resistance and dramatically enhances the line and load regulation. For closed loop operation, the desired regulated output voltage must be lower in magnitude than $-V_{in}$. The output will regulate at a level of $-V_{ref}$ (R_2/R_1 + 1). The adjustable shunt regulator can be from either the TLV431 or TL431 families. The comparator offset or reference voltage is 1.25 V or 2.5 V respectively. The performance characteristics for the converter are shown below. Note that the dashed curve sections represent the converter's open loop performance.

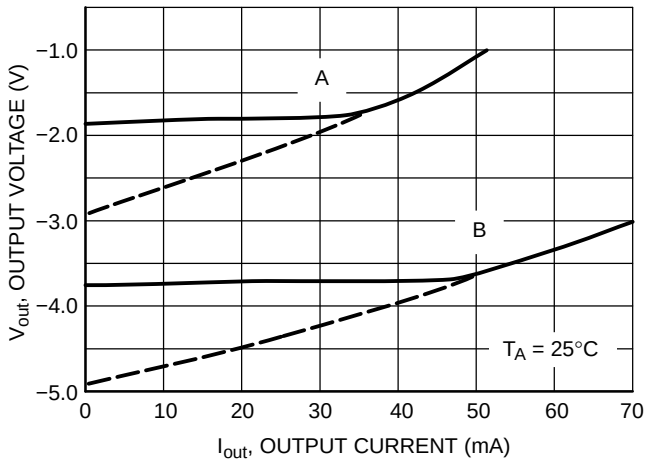


Figure 33. Load Regulation, Output Voltage vs. Output Current

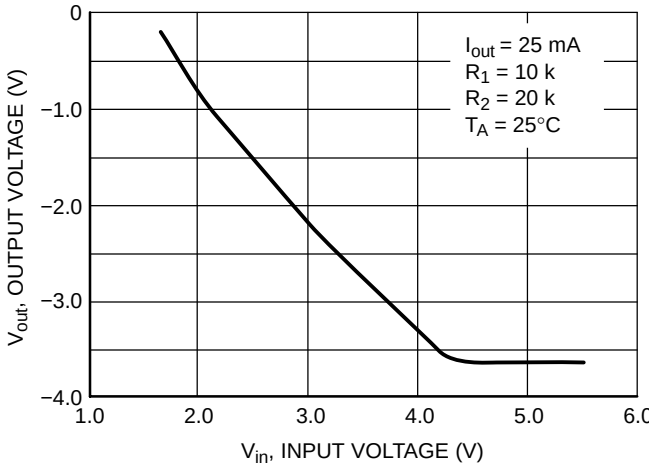
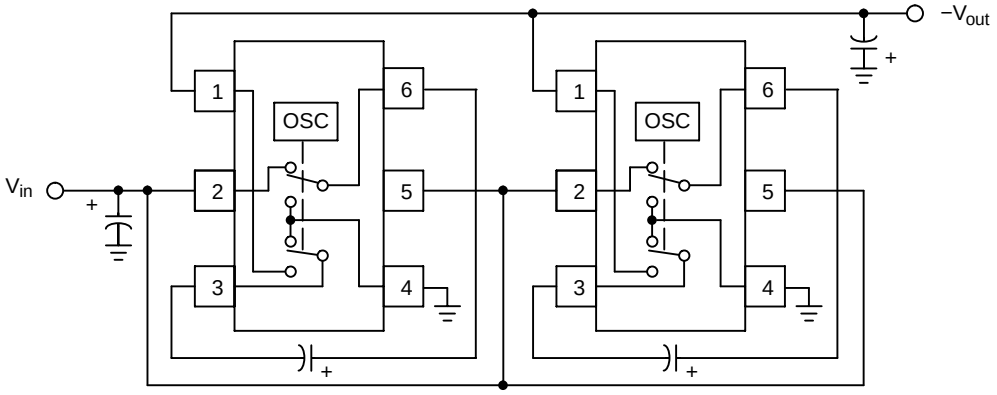


Figure 34. Line Regulation, Output Voltage vs. Input Current

Curve	V_{in} (V)	R_1 (Ω)	R_2 (Ω)	V_{out} (V)
A	3.0	10 k	5.0 k	−1.8
B	5.0	10 k	20 k	−3.6



Capacitors = 10 μF

Figure 35. Paralleling Devices for Increased Negative Output Current

An increase in converter output current capability with a reduction in output resistance can be obtained by paralleling two or more devices. The output current capability is approximately equal to the number of devices paralleled. A single shared output capacitor is sufficient for proper operation but each device does require it's own pump capacitor. Note that the output ripple frequency will be complex since the oscillators are not synchronized. The performance characteristics for a converter consisting of two paralleled devices is shown below.

Curve	V_{in} (V)	R_{out} (Ω)
A	5.0	14.5
B	3.0	17

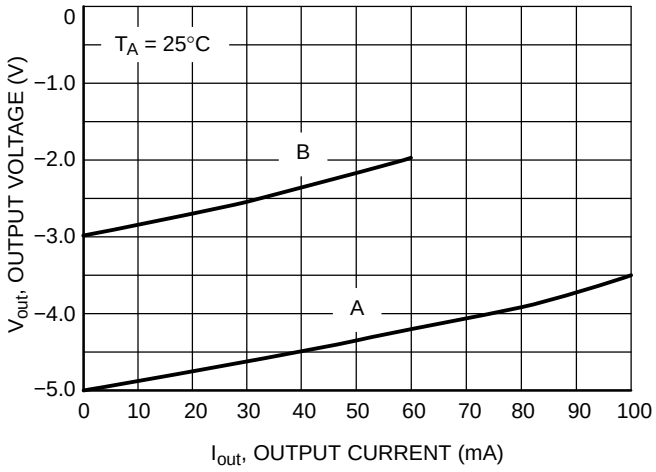


Figure 36. Parallel Load Regulation, Output Voltage vs. Output Current

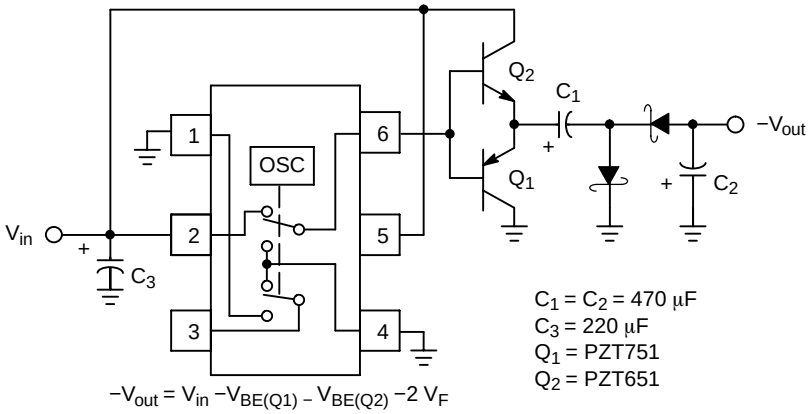


Figure 37. External Switch for Increased Negative Output Current

The output current capability of the MAX1720 can be extended beyond 600 mA with the addition of two external switch transistors and two Schottky diodes. The output voltage is approximately equal to $-V_{in}$ minus the sum of the base emitter drops of both transistors and the forward voltage of both diodes. The performance characteristics for the converter are shown below. Note that the output resistance is reduced to 0.9 Ω.

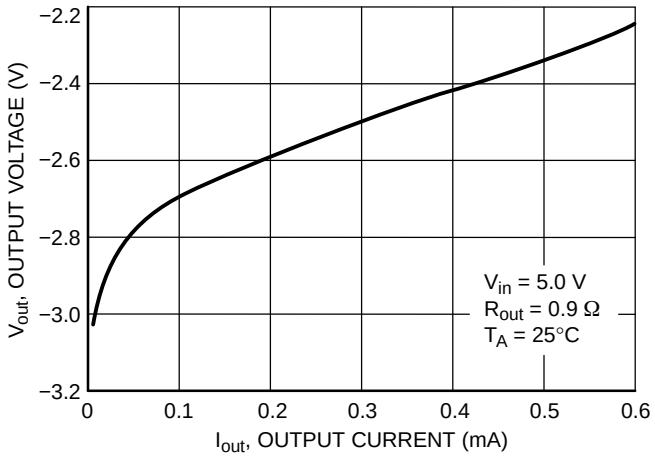


Figure 38. Current Boosted Load Regulation, Output Voltage vs. Output Current

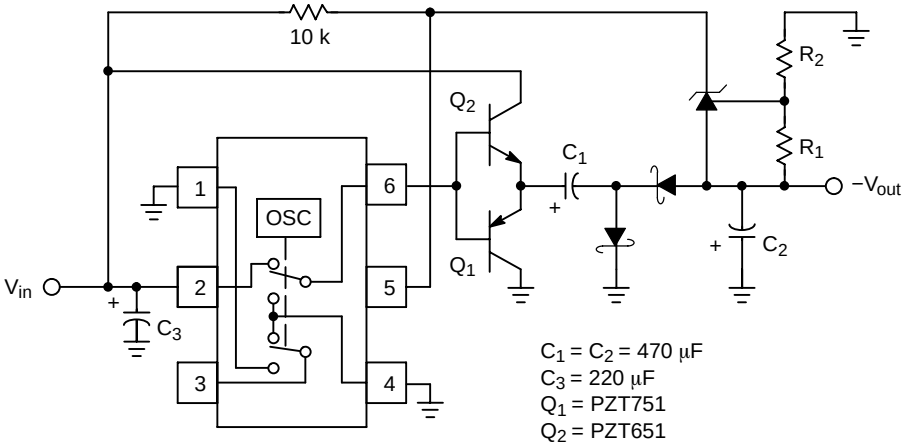


Figure 39. Line and Load Regulated Negative Output Voltage with High Current Capability

This converter is a combination of Figures 37 and 32. It provides a line and load regulated output of −2.36 V at up to 450 mA with an input voltage of 5.0 V. The output will regulate at a level of $-V_{ref}\,(R_2/R_1 + 1)$. The performance characteristics are shown below. Note, the dashed line is the open loop and the solid line is the closed loop performance.

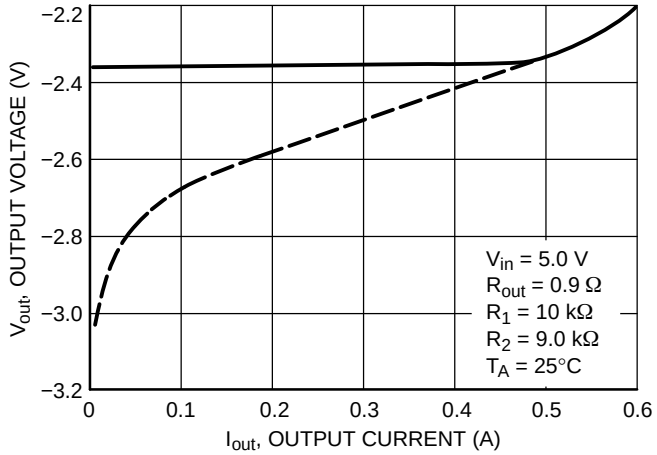


Figure 40. Current Boosted Load Regulation, Output Voltage vs. Output Current

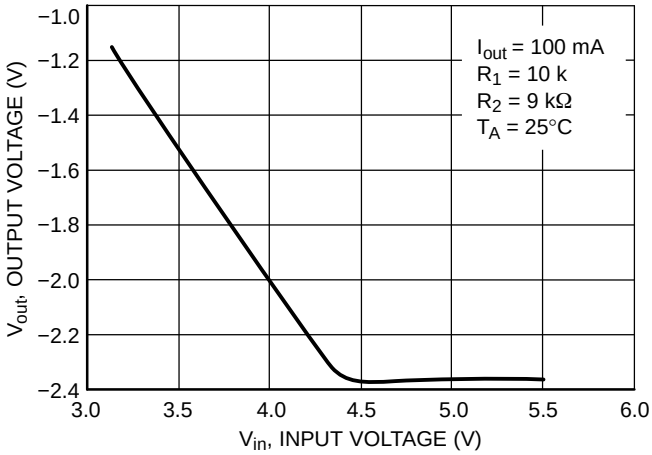


Figure 41. Current Boosted Line Regulation, Output Voltage vs. Input Voltage

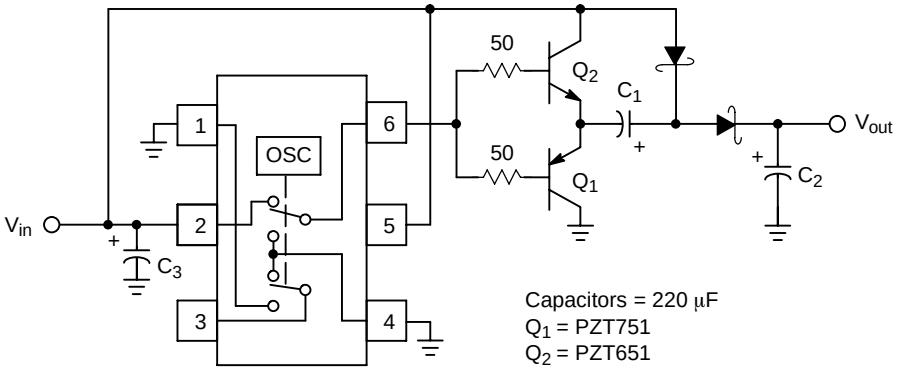


Figure 42. Positive Output Voltage Doubler with High Current Capability

The MAX1720 can be configured to produce a positive output voltage doubler with current capability in excess of 500 mA. This is accomplished with the addition of two external switch transistors and two Schottky diodes. The output voltage is approximately equal to $2V_{in}$ minus the sum of the base emitter drops of both transistors and the forward voltage of both diodes. The performance characteristics for the converter is shown below. Note that the output resistance is reduced to 1.9 Ω.

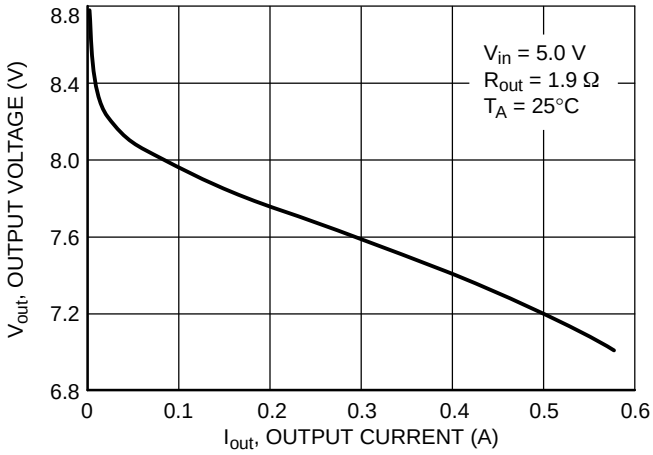


Figure 43. Positive Doubler with Current Boosted Load Regulation, Output Voltage vs. Output Current

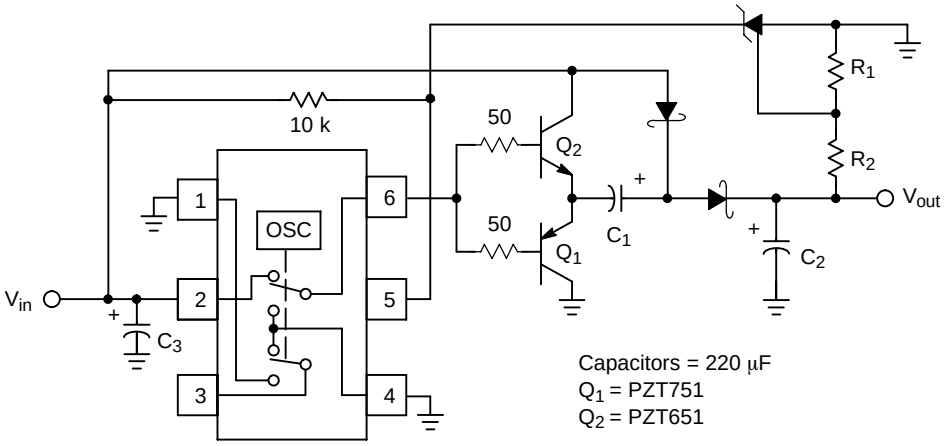


Figure 44. Line and Load Regulated Positive Output Voltage Doubler with High Current Capability

This converter is a combination of Figures 42 and the shunt regulator to close the loop. In this case the anode of the regulator is connected to ground. This convert provides a line and load regulated output of 7.6 V at up to 300 mA with an input voltage of 5.0 V. The output will regulate at a level of V_{ref} (R_2/R_1 + 1). The open loop configuration is the dashed line and the closed loop is the solid line. The performance characteristics are shown below.

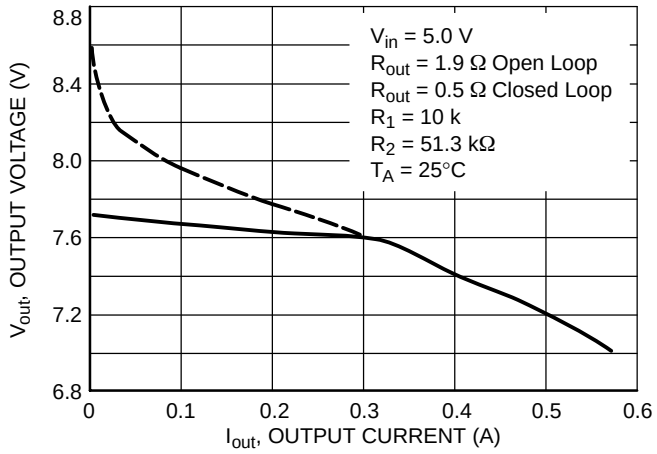


Figure 45. Current Boosted Close Loop Load Regulation, Output Voltage vs. Output Current

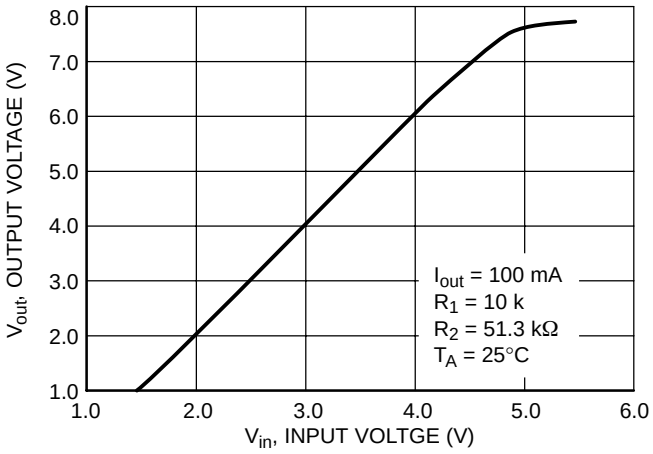


Figure 46. Current Boosted Close Loop Line Regulation, Output Voltage vs. Input Voltage

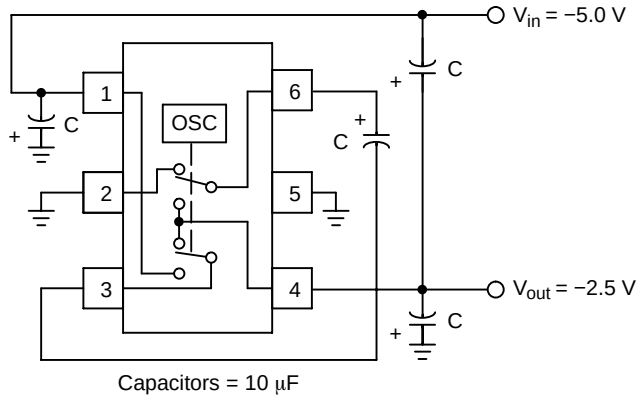


Figure 47. Negative Input Voltage Splitter

A single device can be used to split a negative input voltage. The output voltage is approximately equal to $-V_{in}/2$. The performance characteristics are shown below. Note that the converter has an output resistance of 10 Ω.

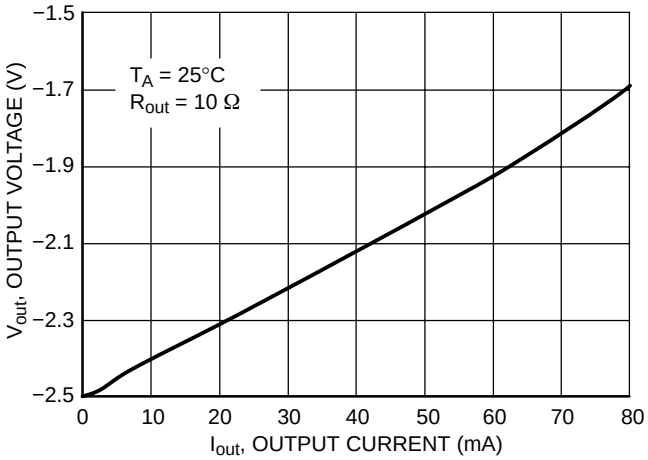


Figure 48. Negative Voltage Splitter Load Regulation, Output Voltage vs. Output Current

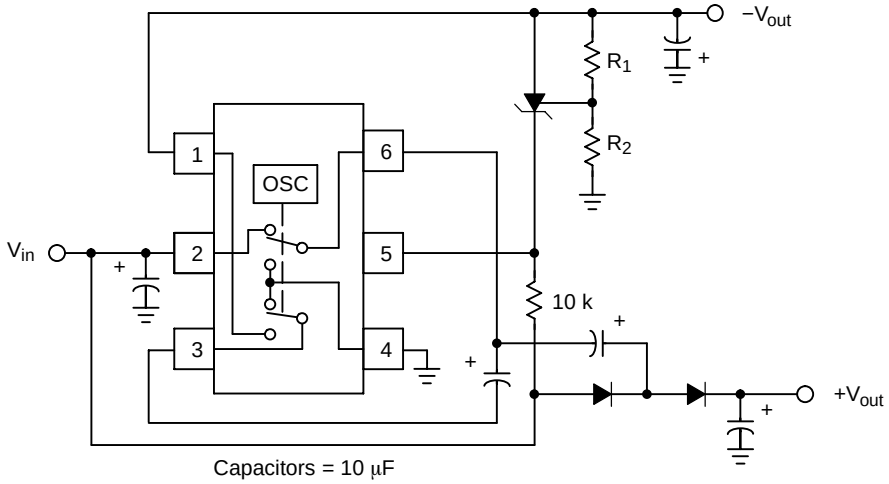


Figure 49. Combination of a Closed Loop Negative Inverter with a Positive Output Voltage Doubler

All of the previously shown converter circuits have only single outputs. Applications requiring multiple outputs can be constructed by incorporating combinations of the former circuits. The converter shown above combines Figures 26 and 32 to form a regulated negative output inverter with a non−regulated positive output doubler. The magnitude of $-V_{out}$ is controlled by the resistor values and follows the relationship $-V_{ref}$ (R_2/R_1 + 1). Since the positive output is not within the feedback loop, its output voltage will increase as the negative output load increases. This cross regulation characteristic is shown in the upper portion of Figure 50. The dashed line is the open loop and the solid line is the closed loop configuration for the load regulation. The load regulation for the positive doubler with a constant load on the $-V_{out}$ is shown in Figure 51.

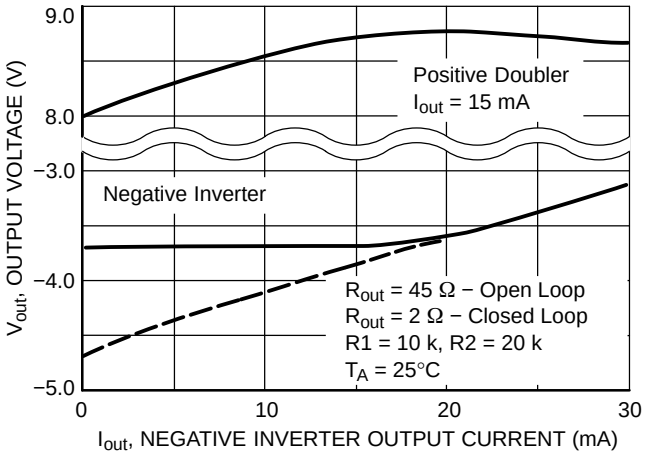


Figure 50. Load Regulation, Output Voltage vs. Output Current

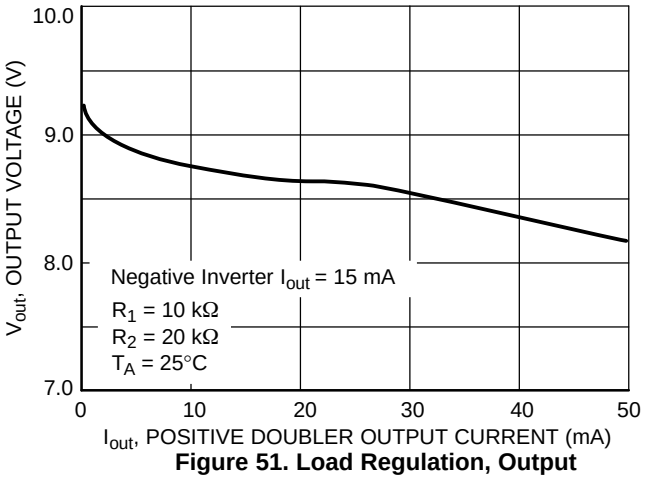


Figure 51. Load Regulation, Output Voltage vs. Output Current

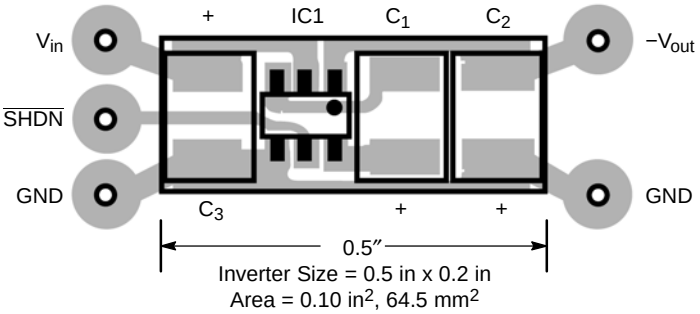
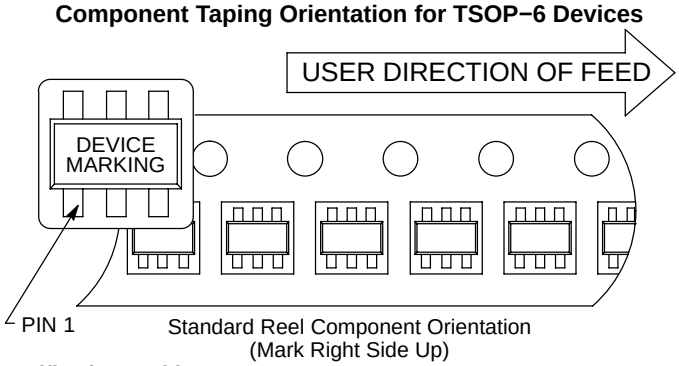


Figure 52. Inverter Circuit Board Layout, Top View Copper Side

TAPING FORM

Component Taping Orientation for TSOP−6 Devices



Tape & Reel Specifications Table

Package	Tape Width (W)	Pitch (P)	Part Per Full Reel	Diameter
TSOP−6	8 mm	4 mm	3000	7 inches

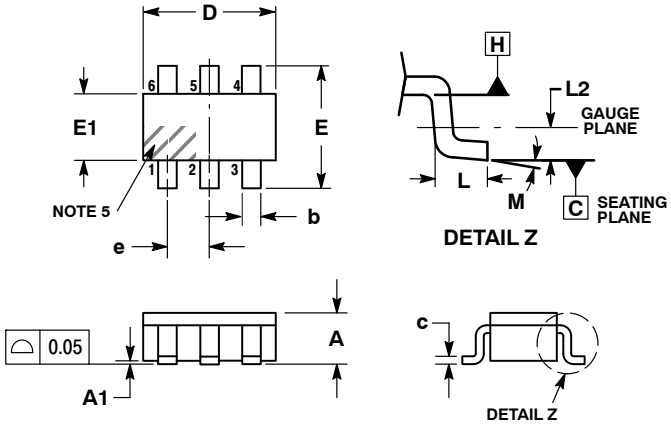
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 2:1

TSOP−6
CASE 318G−02
ISSUE V

DATE 12 JUN 2012



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	–	10°

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

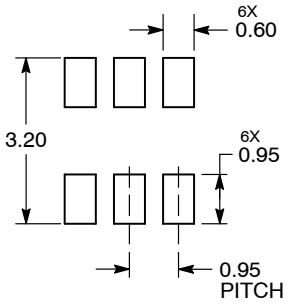
STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

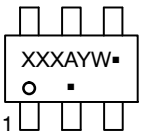
RECOMMENDED SOLDERING FOOTPRINT*



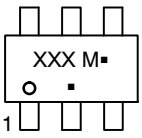
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC



STANDARD

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present.

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