Single Supply Quad Comparators


These comparators are designed for use in level detection, low-level sensing and memory applications in consumer, automotive, and industrial electronic applications.

**Features**
- Single Supply Operation: 3.0 V to 36 V
- Split Supply Operation: ±1.5 V to ±18 V
- Low Input Bias Current: 25 nA (Typ)
- Low Input Offset Current: ±5.0 nA (Typ)
- Low Input Offset Voltage
- Input Common Mode Voltage Range to GND
- Low Output Saturation Voltage: 130 mV (Typ) @ 4.0 mA
- TTL and CMOS Compatible
- ESD Clamps on the Inputs Increase Reliability without Affecting Device Operation
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

**Ordering Information**
See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

**Device Marking Information**
See general marking information in the device marking section on page 8 of this data sheet.
### MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Voltage</td>
<td>$V_{CC}$</td>
<td>$+36$ or $±18$</td>
<td>Vdc</td>
</tr>
<tr>
<td>Input Differential Voltage Range</td>
<td>$V_{IDR}$</td>
<td>$36$</td>
<td>Vdc</td>
</tr>
<tr>
<td>Input Common Mode Voltage Range</td>
<td>$V_{ICMR}$</td>
<td>$−0.3$ to $36$</td>
<td>Vdc</td>
</tr>
<tr>
<td>Output Short Circuit to Ground (Note 1)</td>
<td>$I_{SC}$</td>
<td>Continuous</td>
<td></td>
</tr>
<tr>
<td>Power Dissipation @ $T_A = 25°C$</td>
<td>$P_D$</td>
<td>$1.0$</td>
<td>W</td>
</tr>
<tr>
<td>Plastic Package</td>
<td>$1/R_{JUA}$</td>
<td>$8.0$</td>
<td>mW/°C</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>$T_J$</td>
<td>$150$</td>
<td>°C</td>
</tr>
<tr>
<td>Operating Ambient Temperature Range</td>
<td>$T_A$</td>
<td>$−25$ to $+85$</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$−40$ to $+85$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$−40$ to $+105$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$0$ to $+70$</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$T_{stg}$</td>
<td>$−65$ to $+150$</td>
<td>°C</td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.  
1. The maximum output current may be as high as 20 mA, independent of the magnitude of $V_{CC}$. Output short circuits to $V_{CC}$ can cause excessive heating and eventual destruction.

### ESD RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>HBM</th>
<th>MM</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD Protection at any Pin (Human Body Model – HBM, Machine Model – MM)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NCV2901</td>
<td>2000</td>
<td>200</td>
<td>V</td>
</tr>
<tr>
<td>LM339E, LM2901E</td>
<td>1500</td>
<td>200</td>
<td>V</td>
</tr>
<tr>
<td>LM339DG/DR2G, LM2901DG/DR2G</td>
<td>250</td>
<td>100</td>
<td>V</td>
</tr>
<tr>
<td>All Other Devices</td>
<td>1500</td>
<td>200</td>
<td>V</td>
</tr>
</tbody>
</table>

NOTE: Diagram shown is for 1 comparator.

Figure 1. Circuit Schematic
ELECTRICAL CHARACTERISTICS (\(V_{CC} = +5.0\) Vdc, \(T_A = +25^\circ\)C, unless otherwise noted)

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Offset Voltage (Note 3)</td>
<td>(V_{IO})</td>
<td>–</td>
<td>±2.0</td>
<td>±5.0</td>
<td>–</td>
</tr>
<tr>
<td>Input Bias Current (Notes 3, 4) (Output in Analog Range)</td>
<td>(I_{IB})</td>
<td>–</td>
<td>25</td>
<td>250</td>
<td>–</td>
</tr>
<tr>
<td>Input Offset Current (Note 3)</td>
<td>(I_{IO})</td>
<td>–</td>
<td>±5.0</td>
<td>±50</td>
<td>–</td>
</tr>
<tr>
<td>Input Common Mode Voltage Range (Note 5)</td>
<td>(V_{ICMR})</td>
<td>0</td>
<td>–</td>
<td>-1.5</td>
<td>0</td>
</tr>
<tr>
<td>Supply Current</td>
<td>(I_{CC})</td>
<td>–</td>
<td>0.8</td>
<td>2.0</td>
<td>–</td>
</tr>
<tr>
<td>(R_L = \infty) (For All Comparators)</td>
<td></td>
<td>–</td>
<td>1.0</td>
<td>2.5</td>
<td>–</td>
</tr>
<tr>
<td>Voltage Gain</td>
<td>(A_{VOL})</td>
<td>50</td>
<td>200</td>
<td>–</td>
<td>25</td>
</tr>
<tr>
<td>Large Signal Response Time</td>
<td></td>
<td>–</td>
<td>–</td>
<td>300</td>
<td>–</td>
</tr>
<tr>
<td>Response Time (Note 6)</td>
<td></td>
<td>–</td>
<td>1.3</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Output Sink Current</td>
<td>(I_{Sink})</td>
<td>6.0</td>
<td>16</td>
<td>–</td>
<td>6.0</td>
</tr>
<tr>
<td>Saturation Voltage</td>
<td>(V_{sat})</td>
<td>–</td>
<td>130</td>
<td>400</td>
<td>–</td>
</tr>
<tr>
<td>Output Leakage Current</td>
<td>(I_{OL})</td>
<td>–</td>
<td>0.1</td>
<td>–</td>
<td>–</td>
</tr>
</tbody>
</table>

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. (LM239) \(T_{low} = -25^\circ\)C, \(T_{high} = +85^\circ\)C
   (LM339, LM339E) \(T_{low} = 0^\circ\)C, \(T_{high} = +70^\circ\)C
   (MC3302) \(T_{low} = -40^\circ\)C, \(T_{high} = +85^\circ\)C
   (LM2901), LM2901E \(T_{low} = -40^\circ\)C, \(T_{high} = +105^\circ\)C
   (LM2901V & NCV2901) \(T_{low} = -40^\circ\)C, \(T_{high} = +125^\circ\)C
   NCV2901 is qualified for automotive use.

3. At the output switch point, \(V_O \geq 1.4\) Vdc, \(R_S \leq 100\) Ω, 5.0 Vdc ≤ \(V_{CC}\) ≤ 30 Vdc, with the inputs over the full common mode range (0 Vdc to \(V_{CC} - 1.5\) Vdc).

4. The bias current flows out of the inputs due to the PNP input stage. This current is virtually constant, independent of the output state.

5. Positive excursions of input voltage may exceed the power supply level. As long as one input voltage remains within the common mode range, the comparator will provide a proper output state. Refer to the Maximum Ratings table for safe operating area.

6. The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals, 300 ns is typical.
**PERFORMANCE CHARACTERISTICS**  \((V_{\text{CC}} = +5.0 \text{ Vdc}, T_A = T_{\text{low}} \text{ to } T_{\text{high}} \text{ [Note 7]})\)

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Offset Voltage (Note 8)</td>
<td>(V_{IO})</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Input Bias Current (Notes 8, 9)</td>
<td>(I_{IB})</td>
<td>-</td>
<td>400</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>(Output in Analog Range)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Offset Current (Note 8)</td>
<td>(I_{IO})</td>
<td>-</td>
<td>±150</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Input Common Mode Voltage Range</td>
<td>(V_{ICMR})</td>
<td>0</td>
<td>(-2.0)</td>
<td>0</td>
<td>-</td>
</tr>
<tr>
<td>Saturation Voltage</td>
<td>(V_{sat})</td>
<td>-</td>
<td>700</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>(V_{I(+)} \geq +1.0 \text{ Vdc, } V_{I(-)} = 0, I_{sink} \leq 4.0 \text{ mA})</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Leakage Current</td>
<td>(I_{OL})</td>
<td>-</td>
<td>1.0</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>(V_{I(+)} \geq +1.0 \text{ Vdc, } V_{I(-)} = 0, V_O = 30 \text{ Vdc})</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>(V_{ID})</td>
<td>-</td>
<td>(V_{CC})</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>All (V_I \geq 0 \text{ Vdc})</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

7. (LM239) \(T_{\text{low}} = -25^\circ \text{C, } T_{\text{high}} = +85^\circ \text{C}\)
   (LM339, LM339E) \(T_{\text{low}} = 0^\circ \text{C, } T_{\text{high}} = +70^\circ \text{C}\)
   (MC3302) \(T_{\text{low}} = -40^\circ \text{C, } T_{\text{high}} = +85^\circ \text{C}\)
   (LM2901, LM2901E) \(T_{\text{low}} = -40^\circ \text{C, } T_{\text{high}} = +105^\circ \text{C}\)
   (LM2901V & NCV2901) \(T_{\text{low}} = -40^\circ \text{C, } T_{\text{high}} = +125^\circ \text{C}\)
   NCV2901 is qualified for automotive use.

8. At the output switch point, \(V_O \approx 1.4 \text{ Vdc, } R_S \leq 100 \Omega \text{ Vdc} \leq V_{\text{CC}} \leq 30 \text{ Vdc}\), with the inputs over the full common mode range \((0 \text{ Vdc to } V_{\text{CC}} - 1.5 \text{ Vdc})\).

9. The bias current flows out of the inputs due to the PNP input stage. This current is virtually constant, independent of the output state.

---

**Figure 2. Inverting Comparator with Hysteresis**

\[
\begin{align*}
R_3 &= 10k \\
V_{R1} &= \frac{V_{CC}R_1}{R_{\text{ref}} + R_1} \\
V_{R2} &= \frac{R_1}{R_{\text{ref}} + R_2} \\
V_H &= \frac{R_1}{R_{\text{ref}} + R_2} [V_{O(\text{max})} - V_{O(\text{min})}] \\
V_O &= \frac{R_1}{R_{\text{ref}} + R_2} + V_{\text{ref}} \\
V_{\text{ref}} &= \frac{V_{CC}R_1}{R_{\text{ref}} + R_1}
\end{align*}
\]

**Figure 3. Noninverting Comparator with Hysteresis**

\[
\begin{align*}
R_2 &= \frac{R_1}{R_{\text{ref}}} \\
R_3 &= \frac{1}{R_1} \\
V_H &= \frac{V_{CC}R_1}{R_{\text{ref}} + R_1} \\
V_{\text{ref}} &= \frac{V_{CC}R_1}{R_{\text{ref}} + R_1} \\
V_O &= \frac{R_1}{R_{\text{ref}} + R_2} + V_{\text{ref}} \\
V_{\text{ref}} &= \frac{V_{CC}R_1}{R_{\text{ref}} + R_1}
\end{align*}
\]
Typical Characteristics

\( V_{CC} = 15 \text{ Vdc}, T_A = +25^\circ \text{C} \) (each comparator) unless otherwise noted.

<table>
<thead>
<tr>
<th>Logic</th>
<th>Device</th>
<th>( V_{CC} ) (V)</th>
<th>( R_L ) kΩ</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS</td>
<td>1/4 MC14001</td>
<td>+15</td>
<td>100</td>
</tr>
<tr>
<td>TTL</td>
<td>1/4 MC7400</td>
<td>+5.0</td>
<td>10</td>
</tr>
</tbody>
</table>

Figure 4. Normalized Input Offset Voltage

Figure 5. Input Bias Current

Figure 6. Output Sink Current versus Output Saturation Voltage

Figure 7. Driving Logic

Figure 8. Squarewave Oscillator
These quad comparators feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (VOL to VOH). To alleviate this situation input resistors < 10 kΩ should be used. The addition of positive feedback (< 10 mV) is also recommended. It is good design practice to ground all unused input pins.

Differential input voltages may be larger than supply voltages without damaging the comparator’s inputs. Voltages more negative than −300 mV should not be used.

**Figure 9. Zero Crossing Detector (Single Supply)**

D1 prevents input from going negative by more than 0.6 V.

$$R_1 + R_2 = R_3$$

$$R_3 \leq \frac{R_5}{10}$$ for small error in zero crossing

**Figure 10. Zero Crossing Detector (Split Supplies)**

$$V_{\text{in(min)}} = 0.4 \text{ V peak for 1% phase distortion (Δθ).}$$
## ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package</th>
<th>Shipping</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM239DR2G</td>
<td>SOIC–14 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td>LM239DTBR2G</td>
<td>TSSOP–14 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td>LM339DR2G</td>
<td>SOIC–14 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td>LM339EDR2G</td>
<td>SOIC–14 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td>LM339DTBR2G</td>
<td>TSSOP–14 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td>LM2901DR2G</td>
<td>SOIC–14 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td>LM2901EDR2G</td>
<td>SOIC–14 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td>LM2901DTBR2G</td>
<td>TSSOP–14 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td>LM2901VDR2G</td>
<td>SOIC–14 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td>LM2901VDTBR2G</td>
<td>TSSOP–14 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td>NCV2901DR2G*</td>
<td>SOIC–14 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td>NCV2901DTBR2G*</td>
<td>TSSOP–14 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td>NCV2901CTR*</td>
<td>Bare Die</td>
<td>6000 / Tape &amp; Reel</td>
</tr>
<tr>
<td>MC3302DR2G</td>
<td>SOIC–14 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
</tbody>
</table>

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable.
MARKING DIAGRAMS

SOIC–14
D SUFFIX
CASE 751A

TSSOP–14
DTB SUFFIX
CASE 948G

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or • = Pb−Free Package
(Note: Microdot may be in either location)
*This marking diagram also applies to NCV2901.
**NOTES:**

2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACK-
   AGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH
   OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE
   NOT TO EXCEED 0.10 INCH.
5. DIMENSION C IS MEASURED AT A POINT 0.015 BELOW DATUM
   PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR
   TO DATUM C.
6. DIMENSION b2 IS MEASURED AT THE LEAD TIPS WITH THE
   LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE
   LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE
   CORNERS).

**GENERAL MARKING DIAGRAM**

X...X = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to
device data sheet for actual part marking.
Pb-Free indicator, “G” or microdot “*”,
may or may not be present.
<table>
<thead>
<tr>
<th>STYLE 1</th>
<th>STYLE 2</th>
<th>STYLE 3</th>
<th>STYLE 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIN 1: Collector</td>
<td>PIN 2: Cancelled</td>
<td>PIN 3: Cancelled</td>
<td>PIN 1: Drain</td>
</tr>
<tr>
<td>2. Base</td>
<td>2. Source</td>
<td>2. Gate</td>
<td>3. Gate</td>
</tr>
<tr>
<td>5. Emitter</td>
<td>5. Gate</td>
<td>5. Gate</td>
<td>6. Gate</td>
</tr>
</tbody>
</table>

**STYLE 5:**

| PIN 1: Gate | PIN 2: Drain | PIN 3: Source | PIN 4: No Connection |
| PIN 5: Source | PIN 6: Drain | PIN 7: Gate | PIN 8: Gate |
| PIN 9: Drain | PIN 10: Gate | PIN 11: Source | PIN 12: Source |
| PIN 13: Drain | PIN 14: Gate | PIN 15: No Connection | PIN 16: No Connection |

**STYLE 6:**

| PIN 1: No Connection | PIN 2: Gate | PIN 3: Source | PIN 4: No Connection |
| PIN 5: Gate | PIN 6: Source | PIN 7: Drain | PIN 8: Drain |
| PIN 9: Drain | PIN 10: Gate | PIN 11: Source | PIN 12: Source |
| PIN 13: Drain | PIN 14: Gate | PIN 15: No Connection | PIN 16: No Connection |

**STYLE 7:**

| PIN 1: No Connection | PIN 2: Gate | PIN 3: Source | PIN 4: No Connection |
| PIN 5: Gate | PIN 6: Source | PIN 7: Drain | PIN 8: Drain |
| PIN 9: Drain | PIN 10: Gate | PIN 11: Source | PIN 12: Source |
| PIN 13: Drain | PIN 14: Gate | PIN 15: No Connection | PIN 16: No Connection |

**STYLE 8:**

| PIN 1: Gate | PIN 2: No Connection | PIN 3: Gate | PIN 4: No Connection |
| PIN 5: Gate | PIN 6: No Connection | PIN 7: Gate | PIN 8: Gate |
| PIN 9: Gate | PIN 10: Gate | PIN 11: Gate | PIN 12: Gate |
| PIN 13: Gate | PIN 14: Gate | PIN 15: Gate | PIN 16: Gate |

**STYLE 9:**

| PIN 1: No Connection | PIN 2: Gate | PIN 3: Source | PIN 4: No Connection |
| PIN 5: Gate | PIN 6: Source | PIN 7: Drain | PIN 8: Drain |
| PIN 9: Drain | PIN 10: Gate | PIN 11: Source | PIN 12: Source |
| PIN 13: Drain | PIN 14: Gate | PIN 15: No Connection | PIN 16: No Connection |

**STYLE 10:**

| PIN 1: No Connection | PIN 2: Gate | PIN 3: Source | PIN 4: No Connection |
| PIN 5: Gate | PIN 6: Source | PIN 7: Drain | PIN 8: Drain |
| PIN 9: Drain | PIN 10: Gate | PIN 11: Source | PIN 12: Source |
| PIN 13: Drain | PIN 14: Gate | PIN 15: No Connection | PIN 16: No Connection |

**STYLE 11:**

| PIN 1: Gate | PIN 2: No Connection | PIN 3: Gate | PIN 4: No Connection |
| PIN 5: Gate | PIN 6: No Connection | PIN 7: Gate | PIN 8: Gate |
| PIN 9: Gate | PIN 10: Gate | PIN 11: Gate | PIN 12: Gate |
| PIN 13: Gate | PIN 14: Gate | PIN 15: Gate | PIN 16: Gate |

**STYLE 12:**

| PIN 1: Gate | PIN 2: No Connection | PIN 3: Gate | PIN 4: No Connection |
| PIN 5: Gate | PIN 6: No Connection | PIN 7: Gate | PIN 8: Gate |
| PIN 9: Gate | PIN 10: Gate | PIN 11: Gate | PIN 12: Gate |
| PIN 13: Gate | PIN 14: Gate | PIN 15: Gate | PIN 16: Gate |
NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “/C0071”, may or may not be present. Some products may not follow the Generic Marking.
STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. CATHODE
10. CATHODE
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. COMMON ANODE
10. COMMON CATHODE
11. ANODE/CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. COMMON CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. NO CONNECTION
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON CATHODE
NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE − W − W.

SOLDERING FOOTPRINT

DIMENSIONS: MILLIMETERS

14X 0.36

14X 1.26

0.65 PITCH

GENERIC MARKING DIAGRAM*

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
• = Pb–Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb–Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.