**Voltage Regulator – Adjustable Output, Positive 1.5 A**

**LM317, NCV317**

The LM317 is an adjustable 3-terminal positive voltage regulator capable of supplying in excess of 1.5 A over an output voltage range of 1.2 V to 37 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow-out proof.

The LM317 serves a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317 can be used as a precision current regulator.

**Features**
- Output Current in Excess of 1.5 A
- Output Adjustable between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting Constant with Temperature
- Output Transistor Safe Area Compensation
- Floating Operation for High Voltage Applications
- Eliminates Stocking many Fixed Voltages
- Available in Surface Mount D²PAK–3, and Standard 3–Lead Transistor Package
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

**Figure 1. Standard Application**

\[ V_{\text{out}} = 1.25 V \left( 1 + \frac{R_2}{R_1} \right) + \frac{I_{\text{Adj}} R_2}{R_2} \]

Since \( I_{\text{Adj}} \) is controlled to less than 100 μA, the error associated with this term is negligible in most applications.
MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input–Output Voltage Differential</td>
<td>$V_{I-V_O}$</td>
<td>−0.3 to 40</td>
<td>Vdc</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Case 221A</td>
<td>$P_D$</td>
<td>Internally Limited</td>
<td>W</td>
</tr>
<tr>
<td>Thermal Resistance, Junction–to–Ambient</td>
<td>$\theta_{JA}$</td>
<td>65</td>
<td>°C/W</td>
</tr>
<tr>
<td>Thermal Resistance, Junction–to–Case</td>
<td>$\theta_{JC}$</td>
<td>5.0</td>
<td>°C/W</td>
</tr>
<tr>
<td>Case 936 (D²PAK–3)</td>
<td>$P_D$</td>
<td>Internally Limited</td>
<td>W</td>
</tr>
<tr>
<td>Thermal Resistance, Junction–to–Ambient</td>
<td>$\theta_{JA}$</td>
<td>70</td>
<td>°C/W</td>
</tr>
<tr>
<td>Thermal Resistance, Junction–to–Case</td>
<td>$\theta_{JC}$</td>
<td>5.0</td>
<td>°C/W</td>
</tr>
<tr>
<td>Operating Junction Temperature Range</td>
<td>$T_J$</td>
<td>−55 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$T_{stg}$</td>
<td>−65 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS

($V_{I-V_O} = 5.0$ V, $I_O = 0.5$ A for D2T and T packages; $T_J = T_{low}$ to $T_{high}$ (Note 1); $I_{max}$ and $P_{max}$ (Note 2); unless otherwise noted.)

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line Regulation (Note 3), $T_A = +25 ^\circ C$, $3.0 , V \leq V_{I-V_O} \leq 40 , V$</td>
<td>$R_{line}$</td>
<td>0.01</td>
<td>0.04</td>
<td>%/V</td>
</tr>
<tr>
<td>Load Regulation (Note 3), $T_A = +25 ^\circ C$, 10 mA $\leq I_O \leq I_{max}$, $V_O = 5.0 , V$</td>
<td>$R_{load}$</td>
<td>5.0</td>
<td>25</td>
<td>mV/V</td>
</tr>
<tr>
<td>Thermal Regulation, $T_A = +25 ^\circ C$ (Note 4), 20 ms Pulse</td>
<td>$R_{therm}$</td>
<td>0.03</td>
<td>0.07</td>
<td>% $V_O$/W</td>
</tr>
<tr>
<td>Adjustment Pin Current</td>
<td>$I_{Adj}$</td>
<td>50</td>
<td>100</td>
<td>µA</td>
</tr>
<tr>
<td>Adjustment Pin Current Change, 2.5 V $\leq V_{I-V_O} \leq 40 , V$, 10 mA $\leq I_O \leq I_{max}$, $P_D \leq P_{max}$</td>
<td>$\Delta I_{Adj}$</td>
<td>0.2</td>
<td>5.0</td>
<td>µA</td>
</tr>
<tr>
<td>Reference Voltage, $3.0 , V \leq V_{I-V_O} \leq 40 , V$, 10 mA $\leq I_O \leq I_{max}$, $P_D \leq P_{max}$</td>
<td>$V_{ref}$</td>
<td>1.2</td>
<td>1.25</td>
<td>1.3 V</td>
</tr>
<tr>
<td>Line Regulation (Note 3), $3.0 , V \leq V_{I-V_O} \leq 40 , V$</td>
<td>$R_{line}$</td>
<td>0.02</td>
<td>0.07</td>
<td>%/V</td>
</tr>
<tr>
<td>Load Regulation (Note 3), 10 mA $\leq I_O \leq I_{max}$</td>
<td>$R_{load}$</td>
<td>20</td>
<td>70</td>
<td>mV/V</td>
</tr>
<tr>
<td>Temperature Stability ($T_{low} \leq T_J \leq T_{high}$)</td>
<td>$T_S$</td>
<td>0.7</td>
<td>–</td>
<td>% $V_O$</td>
</tr>
<tr>
<td>Minimum Load Current to Maintain Regulation ($V_{I-V_O} = 40 , V$)</td>
<td>$I_{min}$</td>
<td>3.5</td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td>Maximum Output Current</td>
<td>$I_{max}$</td>
<td>1.5</td>
<td>2.2</td>
<td>–</td>
</tr>
<tr>
<td>$V_{I-V_O} \leq 15 , V$, $P_O \leq P_{max}$, T Package</td>
<td></td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>$V_{I-V_O} = 40 , V$, $P_O \leq P_{max}$, $T_A = +25 ^\circ C$, T Package</td>
<td>$P_{max}$</td>
<td>0.15</td>
<td>0.4</td>
<td>–</td>
</tr>
<tr>
<td>RMS Noise, % of $V_O$, $T_A = +25 ^\circ C$, 10 Hz $\leq f \leq 10 , kHz$</td>
<td>$N$</td>
<td>0.003</td>
<td>–</td>
<td>% $V_O$</td>
</tr>
<tr>
<td>Ripple Rejection, $V_O = 10 , V$, $f = 120 , Hz$ (Note 5)</td>
<td>$RR$</td>
<td>65</td>
<td>–</td>
<td>dB</td>
</tr>
<tr>
<td>Without $C_{Adj}$, $C_{Adj} = 10$ µF</td>
<td></td>
<td>66</td>
<td>80</td>
<td>–</td>
</tr>
<tr>
<td>Thermal Shutdown (Note 6)</td>
<td></td>
<td>–</td>
<td>180</td>
<td>–</td>
</tr>
<tr>
<td>Long–Term Stability, $T_J = T_{high}$ (Note 7), $T_A = +25 ^\circ C$ for Endpoint Measurements</td>
<td>$S$</td>
<td>0.3</td>
<td>1.0</td>
<td>%/1.0 kHrs.</td>
</tr>
<tr>
<td>Thermal Resistance Junction–to–Case, T Package</td>
<td>$R_{UC}$</td>
<td>5.0</td>
<td>–</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

1. $T_{low}$ to $T_{high}$ = 0° to +125° C, for LM317T, D2T. $T_{low}$ to $T_{high}$ = −40° to +125° C, for LM317BT, BD2T.
2. $I_{max}$ = 1.5 A, $P_{max}$ = 20 W
3. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
4. Power dissipation within an IC voltage regulator produces a temperature gradient on the die, affecting individual IC components on the die. These effects can be minimized by proper integrated circuit design and layout techniques. Thermal Regulation is the effect of these temperature gradients on the output voltage and is expressed in percentage of output change per watt of power change in a specified time.
5. $C_{Adj}$, when used, is connected between the adjustment pin and ground.
6. Thermal characteristics are not subject to production test.
7. Since Long–Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

www.onsemi.com
This device contains 29 active transistors.

Figure 2. Representative Schematic Diagram

Figure 3. Line Regulation and $\Delta I_{\text{Adj}}$/Line Test Circuit

* Pulse testing required. 1% Duty Cycle is suggested.

Line Regulation (%/V) = $\frac{|V_{OH} - V_{OL}|}{|V_{OL}|} \times 100$
Load Regulation (mV) = \text{VO (min Load)} - \text{VO (max Load)}

Load Regulation (% VO) = \frac{\text{VO (min Load)} - \text{VO (max Load)}}{\text{VO (min Load)}} \times 100

* Pulse testing required. 1% Duty Cycle is suggested.

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Figure 4. Load Regulation and \(\Delta I_{\text{Adj}}/\text{Load} \) Test Circuit

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To Calculate \(R_2\): \(V_{\text{out}} = I_{\text{SET}} R_2 + 1.250 \text{ V}\)

Assume \(I_{\text{SET}} = 5.25 \text{ mA}\)

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Figure 5. Standard Test Circuit

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\* D\(_1\) Discharges \(C_{\text{Adj}}\) if output is shorted to Ground.

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Figure 6. Ripple Rejection Test Circuit
Figure 7. Load Regulation

Figure 8. Current Limit

Figure 9. Adjustment Pin Current

Figure 10. Dropout Voltage

Figure 11. Temperature Stability

Figure 12. Minimum Operating Current
Basic Circuit Operation

The LM317 is a 3-terminal floating regulator. In operation, the LM317 develops and maintains a nominal 1.25 V reference (Vref) between its output and adjustment terminals. This reference voltage is converted to a programming current (Iprog) by R1 (see Figure 17), and this constant current flows through R2 to ground.

The regulated output voltage is given by:

\[ V_{\text{out}} = V_{\text{ref}} \left(1 + \frac{R_2}{R_1}\right) + I_{\text{Adj}} R_2 \]

Since the current from the adjustment terminal (I_{\text{Adj}}) represents an error term in the equation, the LM317 was designed to control I_{\text{Adj}} to less than 100 µA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM317 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

Load Regulation

The LM317 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

External Capacitors

A 0.1 µF disc or 1.0 µF tantalum input bypass capacitor (C_in) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{Adj}) prevents ripple from being amplified as the output voltage is increased. A 10 µF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.

Although the LM317 is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1.0 µF tantalum or 25 µF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

Protection Diodes

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM317 with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values (C_O > 25 µF, C_{Adj} > 10 µF). Diode D1 prevents C_O from discharging through the IC during an input short circuit. Diode D2 protects against capacitor C_{Adj} discharging through the IC during an output short circuit. The combination of diodes D1 and D2 prevents C_{Adj} from discharging through the IC during an input short circuit.
Figure 21. D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

Figure 22. “Laboratory” Power Supply with Adjustable Current Limit and Output Voltage

Diodes \(D_1\) and \(D_2\) and transistor \(Q_2\) are added to allow adjustment of output voltage to 0 V.

\* \(D_6\) protects both LM317's during an input short circuit.
* To provide current limiting of $I_O$ to the system ground, the source of the FET must be tied to a negative voltage below $-1.25$ V.

$$R_1 = \frac{V_{ref}}{I_{O_{\text{max}}} + I_{DSS}}$$

$$R_2 \leq \frac{V_{ref}}{I_{DSS}}$$

$V_O < BVDSS + 1.25 \text{ V} + V_{SS}$,

$L_{\text{min}} - I_{DSS} < I_O < 1.5$ A.

As shown $0 < I_O < 1.0$ A.

* $D_1$ protects the device during an input short circuit.

**Figure 23. Adjustable Current Limiter**

**Figure 24. 5.0 V Electronic Shutdown Regulator**

**Figure 25. Slow Turn–On Regulator**

**Figure 26. Current Regulator**
## ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Operating Temperature Range</th>
<th>Package</th>
<th>Shipping†</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM317BD2TG</td>
<td>T&lt;sub&gt;J&lt;/sub&gt; = −40° to +125°C</td>
<td>D&lt;sup&gt;2&lt;/sup&gt;PAK–3 (Pb–Free)</td>
<td>50 Units / Rail</td>
</tr>
<tr>
<td>LM317BD2TR4G</td>
<td></td>
<td>D&lt;sup&gt;2&lt;/sup&gt;PAK–3 (Pb–Free)</td>
<td>800 Tape &amp; Reel</td>
</tr>
<tr>
<td>LM317BTG</td>
<td></td>
<td>TO–220 (Pb–Free)</td>
<td>50 Units / Rail</td>
</tr>
<tr>
<td>LM317D2TG</td>
<td>T&lt;sub&gt;J&lt;/sub&gt; = 0° to +125°C</td>
<td>D&lt;sup&gt;2&lt;/sup&gt;PAK–3 (Pb–Free)</td>
<td>50 Units / Rail</td>
</tr>
<tr>
<td>LM317D2TR4G</td>
<td></td>
<td>D&lt;sup&gt;2&lt;/sup&gt;PAK–3 (Pb–Free)</td>
<td>800 Tape &amp; Reel</td>
</tr>
<tr>
<td>LM317TG</td>
<td></td>
<td>TO–220 (Pb–Free)</td>
<td>50 Units / Rail</td>
</tr>
<tr>
<td>NCV317BD2TG*</td>
<td>T&lt;sub&gt;J&lt;/sub&gt; = −55° to +150°C</td>
<td>D&lt;sup&gt;2&lt;/sup&gt;PAK–3 (Pb–Free)</td>
<td>50 Units / Rail</td>
</tr>
<tr>
<td>NCV317BD2TR4G*</td>
<td></td>
<td>D&lt;sup&gt;2&lt;/sup&gt;PAK–3 (Pb–Free)</td>
<td>800 Tape &amp; Reel</td>
</tr>
<tr>
<td>NCV317BTG*</td>
<td></td>
<td>TO–220 (Pb–Free)</td>
<td>50 Units / Rail</td>
</tr>
</tbody>
</table>

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable.

### MARKING DIAGRAMS

**D<sup>2</sup>PAK–3 D2T SUFFIX CASE 936**

1. **LM 317BD2T AWLYWWG**
2. **LM 317D2T AWLYWWG**
3. **NC V317BD2T AWLYWWG**

**TO–220 T SUFFIX CASE 221A**

1. **LM 317BT AWLYWWG**
2. **LM 317T AWLYWWG**
3. **NC V317BT AWLYWWG**

- **A** = Assembly Location
- **WL** = Wafer Lot
- **Y** = Year
- **WW** = Work Week
- **G** = Pb–Free Package
TO-220, SINGLE GAUGE
CASE 221AB-01
ISSUE A

DATE 16 NOV 2010

NOTES:
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND
LEAD IRREGULARITIES ARE ALLOWED.
4. PRODUCT SHIPPED PRIOR TO 2008 HAD DIMENSIONS
S = 0.045 - 0.055 INCHES (1.143 - 1.397 MM)

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/Delay
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

SCALE 1:1

DIM MIN MAX MIN MAX
MILLIMETERS INCHES
A 0.570 0.620 14.48 15.75
B 0.380 0.405 9.66 10.26
C 0.160 0.190 4.07 4.82
D 0.025 0.035 0.64 0.88
E 0.140 0.147 3.61 3.73
F 0.095 0.105 2.42 2.66
H 0.110 0.155 2.80 3.93
J 0.018 0.025 0.46 0.64
K 0.500 0.562 12.70 14.27
L 0.045 0.060 1.15 1.52
M 0.190 0.210 4.85 5.33
Q 0.100 0.120 2.54 3.04
R 0.080 0.110 2.04 2.79
S 0.020 0.025 0.51 0.64
T 0.235 0.255 5.97 6.47
U 0.000 0.050 0.00 1.27
V 0.045 --- 1.15 ---
Z --- 0.080 --- 2.04 ---
NOTES:
2. CONTROLLING DIMENSION: INCHES.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.
6. SINGLE GAUGE DESIGN WILL BE SHIPPED AFTER FPCN EXPIRATION IN OCTOBER 2011.

DIMENSIONS: MILLIMETERS

SOLDERING FOOTPRINT*

DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “/C0071”, may or may not be present.